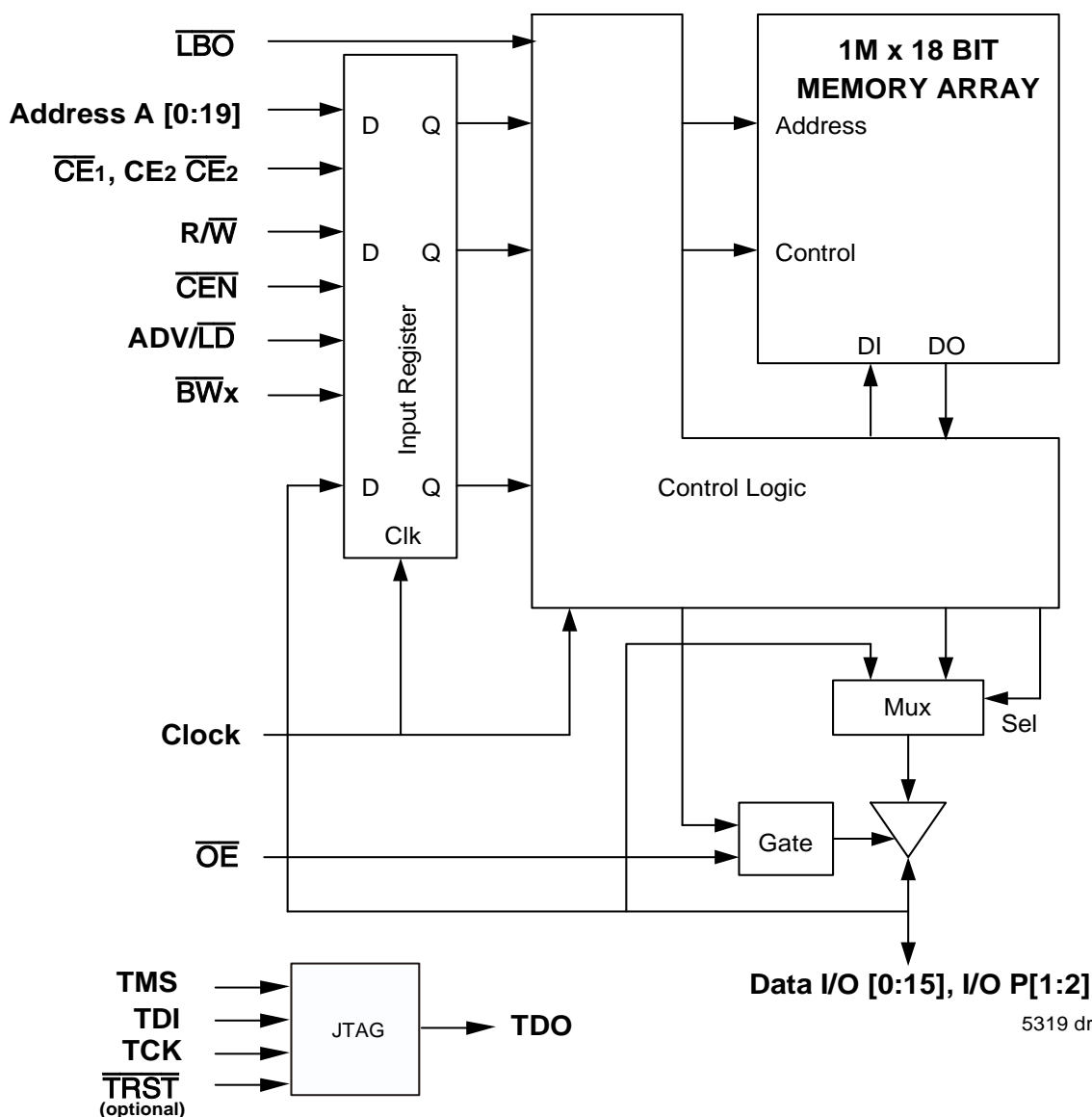# 1M x 18
2.5V Synchronous ZBT™ SRAM
2.5V I/O, Burst Counter
Flow-Through Outputs

IDT71T75902

Features

- 1M x 18 memory configuration
- Supports high performance system speed - 100 MHz (7.5 ns Clock-to-Data Access)
- ZBT™ Feature - No dead cycles between write and read cycles
- Internally synchronized output buffer enable eliminates the need to control $\overline{OE}$
- Single R/$\overline{W}$ (READ/WRITE) control pin
- 4-word burst capability (Interleaved or linear)
- Individual byte write ($\overline{BW}_1$ - $\overline{BW}_2$ control (May tie active)

- Three chip enables for simple depth expansion
- 2.5V power supply (±5%)
- 2.5V (±5%) I/O Supply (V$_{DDQ}$)
- Power down controlled by ZZ input
- Boundary Scan JTAG Interface (IEEE 1149.1 Compliant)
- Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA)
- Green parts available, see Ordering Information

Functional Block Diagram — 1M x 18

5319 drw 01a

DSC-5319/10

Description

The IDT71T75902 is a 2.5V high-speed 18,874,368-bit (18 Megabit) synchronous SRAM organized as 1M x 18. It is designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus it has been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and on the next clock cycle the associated data cycle occurs, be it read or write.

The IDT71T75902 contain address, data-in and control signal registers. The outputs are flow-through (no output data register). Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable ($\overline{CEN}$) pin allows operation of the IDT71T75902 to be suspended as long as necessary. All synchronous inputs are ignored when $\overline{CEN}$ is high and the internal device registers will hold their previous values.

There are three chip enable pins ($\overline{CE}_1$, CE_2, $\overline{CE}_2$) that allow the user to deselect the device when desired. If any one of these three is not asserted when ADV/$\overline{LD}$ is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state one cycle after the chip is deselected or a write is initiated.

The IDT71T75902 has an on-chip burst counter. In the burst mode, the IDT71T75902 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the $\overline{LBO}$ input pin. The $\overline{LBO}$ pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH).

The IDT71T75902 SRAM utilize IDT's high-performance CMOS process, and are packaged in a JEDEC Standard 14mm x 20mm 100-pin plastic thin quad flatpack (TQFP) as well as a 119 ball grid array (BGA).

Pin Description Summary

A_0-A_{19}	Address Inputs	Input	Synchronous
$\overline{CE}_1$, CE_2, $\overline{CE}_2$	Chip Enables	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
R/$\overline{W}$	Read/Write Signal	Input	Synchronous
$\overline{CEN}$	Clock Enable	Input	Synchronous
$\overline{BW}_1$, $\overline{BW}_2$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
ADV/$\overline{LD}$	Advance Burst Address/Load New Address	Input	Synchronous
$\overline{LBO}$	Linear/Interleaved Burst Order	Input	Static
TMS	Test Mode Select	Input	N/A
TDI	Test Data Input	Input	N/A
TCK	Test Clock	Input	N/A
TDO	Test Data Output	Output	N/A
$\overline{TRST}$	JTAG Reset (Optional)	Input	Asynchronous
ZZ	Sleep Mode	Input	Synchronous
I/O$_0$-I/O$_{31}$, I/O$_{P1}$-I/O$_{P2}$	Data Input/Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	Static
V_{SS}	Ground	Supply	Static

5319 tbl 01a

Pin Definitions[1]

Symbol	Pin Function	I/O	Active	Description
A_0-A_{19}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/$\overline{LD}$ low, $\overline{CEN}$ low, and true chip enables.
ADV/$\overline{LD}$	Advance / Load	I	N/A	ADV/$\overline{LD}$ is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/$\overline{LD}$ is low with the chip deselected, any burst in progress is terminated. When ADV/$\overline{LD}$ is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/$\overline{LD}$ is sampled high.
R/$\overline{W}$	Read / Write	I	N/A	R/$\overline{W}$ signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place one clock cycle later.
$\overline{CEN}$	Clock Enable	I	LOW	Synchronous Clock Enable Input. When $\overline{CEN}$ is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{CEN}$ sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, $\overline{CEN}$ must be sampled low at rising edge of clock.
$\overline{BW}_1$-$\overline{BW}_2$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (When R/$\overline{W}$ and ADV/$\overline{LD}$ are sampled low) the appropriate byte write signal ($\overline{BW}_1$-$\overline{BW}_2$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/$\overline{W}$ is sampled high. The appropriate byte(s) of data are written into the device one cycle later. $\overline{BW}_1$-$\overline{B}_2$ can all be tied low if always doing write to the entire 18-bit word.
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enables	I	LOW	Synchronous active low chip enable. $\overline{CE}_1$ and $\overline{CE}_2$ are used with CE_2 to enable the IDT71T75902 ($\overline{CE}_1$ or $\overline{CE}_2$ sampled high or CE_2 sampled low) and ADV/$\overline{LD}$ low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a one cycle deselect, i.e., the data bus will tri-state one clock cycle after deselect is initiated.
CE_2	Chip Enable	I	HIGH	Synchronous active high chip enable. CE_2 is used with $\overline{CE}_1$ and $\overline{CE}_2$ to enable the chip. CE_2 has inverted polarity but otherwise identical to $\overline{CE}_1$ and $\overline{CE}_2$.
CLK	Clock	I	N/A	This is the clock input to the IDT71T75902. Except for $\overline{OE}$, all timing references for the device are made with respect to the rising edge of CLK.
I/O$_0$-I/O$_{31}$ I/O$_{P1}$-I/O$_{P2}$	Data Input/Output	I/O	N/A	Data input/output (I/O) pins. The data input path is registered, triggered by the rising edge of CLK. The data output path is flow-through (no output register).
$\overline{LBO}$	Linear Burst Order	I	LOW	Burst order selection input. When $\overline{LBO}$ is high the Interleaved burst sequence is selected. When $\overline{LBO}$ is low the Linear burst sequence is selected. $\overline{LBO}$ is a static input, and it must not change during device operation.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. $\overline{OE}$ must be low to read data from the IDT71T75902. When $\overline{OE}$ is HIGH the I/O pins are in a high-impedance state. $\overline{OE}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{OE}$ can be tied low.
TMS	Test Mode Select	I	N/A	Gives input command for TAP controller; sampled on rising edge of TCK. This pin has an internal pullup.
TDI	Test Data Input	I	N/A	Serial input of registers placed between TDI and TDO. Sampled on rising edge of TCK. This pin has an internal pullup.
TCK	Test Clock	I	N/A	Clock input of TAP controller. Each TAP event is clocked. Test inputs are captured on rising edge of TCK, while test outputs are driven from falling edge of TCK. This pin has an internal pullup.
TDO	Test Data Output	O	N/A	Serial output of registers placed between TDI and TDO. This output is active depending on the state of the TAP controller.
$\overline{TRST}$	JTAG Reset (Optional)	I	LOW	Optional asynchronous JTAG reset. Can be used to reset the TAP controller, but not required. JTAG reset occurs automatically at power up and also resets using TMS and TCK per IEEE 1149.1. If not used $\overline{TRST}$ can be left floating. This pin has an internal pullup. Only available in BGA package.
ZZ	Sleep Mode	I	HIGH	Synchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71T75902 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. This pin has an internal pulldown.
V_{DD}	Power Supply	N/A	N/A	2.5V core power supply.
V_{DDQ}	Power Supply	N/A	N/A	2.5V I/O Supply.
V_{SS}	Ground	N/A	N/A	Ground.

5319 tbl 02a

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial	Industrial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +3.6	-0.5 to +3.6	V
V_{TERM}[3,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	-0.5 to V_{DD}	V
V_{TERM}[4,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.5	-0.5 to V_{DD} +0.5	V
V_{TERM}[5,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DDQ} +0.5	-0.5 to V_{DDQ} +0.5	V
T_A[7]	Operating Ambient Temperature	0 to +70	-40 to +85	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	°C
P_T	Power Dissipation	2.0	2.0	W
I_{OUT}	DC Output Current	50	50	mA

5319 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
7. During production testing, the case temperature equals T_A.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	2.375	2.5	2.625	V
V_{DDQ}	I/O Supply Voltage	2.375	2.5	2.625	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage — Inputs	1.7	—	V_{DD} +0.3	V
V_{IH}	Input High Voltage — I/O	1.7	—	V_{DDQ} +0.3[2]	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.7	V

5319 tbl 03

NOTE:
1. V_{IL} (min.) = –0.8V for pulse width less than $t_{CYC}/2$, once per cycle.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature[1]	V_{SS}	V_{DD}	V_{DDQ}
Commerical	0 °C to +70 °C	OV	2.5V ± 5%	2.5V ± 5%
Industrial	-40 °C to +85 °C	OV	2.5V ± 5%	2.5V ± 5%

5319 tbl 05

NOTE:
1. During production testing, the case temperature equals the ambient temperature.

TQFP Capacitance
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5319 tbl 07

BGA Capacitance
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5319 tbl 07a

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

Pin Configuration — 1M x 18, 100 TQFP

Top pins (100–81): A6, A7, $\overline{CE}_1$, CE2, NC, NC, $\overline{BW}_2$, $\overline{BW}_1$, $\overline{CE}_2$, VDD, VSS, CLK, R/$\overline{W}$, $\overline{CEN}$, $\overline{OE}$, ADV/$\overline{D}$, A19, A18, A8, A9

Pin	Left		Right	Pin
1	NC		A10	80
2	NC		NC	79
3	NC		NC	78
4	VDDQ		VDDQ	77
5	VSS		VSS	76
6	NC		NC	75
7	NC		I/OP1	74
8	I/O8		I/O7	73
9	I/O9		I/O6	72
10	VSS		VSS	71
11	VDDQ		VDDQ	70
12	I/O10		I/O5	69
13	I/O11		I/O4	68
14	VSS(1)		VSS	67
15	VDD		VSS(1)	66
16	VDD(2)		VDD	65
17	VSS		ZZ	64
18	I/O12		I/O3	63
19	I/O13		I/O2	62
20	VDDQ		VDDQ	61
21	VSS		VSS	60
22	I/O14		I/O1	59
23	I/O15		I/O0	58
24	I/OP2		NC	57
25	NC		NC	56
26	VSS		VSS	55
27	VDDQ		VDDQ	54
28	NC		NC	53
29	NC		NC	52
30	NC		NC	51

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Bottom pins (31–50): $\overline{LBO}$, A5, A4, A3, A2, A1, A0, NC/TMS(3), NC/TDI(3), VSS, VDD, NC/TDO(3), NC/TCK(3,4), A11, A12, A13, A14, A15, A16, A17

5319 drw 02a

Top View
100 TQFP

NOTES:
1. Pins 14 and 66 do not have to be connected directly to VSS as long as the input voltage is ≤ VIL.
2. Pin 16 does not have to be connected directly to VDD as long as the input voltage is ≥ VIH.
3. Pins 38, 39 and 43 will be pulled internally to VDD if not actively driven. To disable the TAP controller without interfering with normal operation, several settings are possible. Pins 38, 39 and 43 could be tied to VDD or VSS and pin 42 should be left unconnected. Or all JTAG inputs (TMS, TDI and TCK) pins 38, 39 and 43 could be left unconnected "NC" and the JTAG circuit will remain disabled from power up.

Pin Configurations — 1M x 18, 119 BGA[1,2,3]

	1	2	3	4	5	6	7
A	V_{DDQ}	A_6	A_4	A_{19}	A_8	A_{16}	V_{DDQ}
B	NC	CE_2	A_3	$ADV/\overline{LD}$	A_9	$\overline{CE}_2$	NC
C	NC	A_7	A_2	V_{DD}	A_{13}	A_{17}	NC
D	I/O_8	NC	V_{SS}	NC	V_{SS}	I/O_{P1}	NC
E	NC	I/O_9	V_{SS}	$\overline{CE}_1$	V_{SS}	NC	I/O_7
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	I/O_6	V_{DDQ}
G	NC	I/O_{10}	$\overline{BW}_2$	A_{18}	V_{SS}	NC	I/O_5
H	I/O_{11}	NC	V_{SS}	$R/\overline{W}$	V_{SS}	I/O_4	NC
J	V_{DDQ}	V_{DD}	$V_{DD}^{(2)}$	V_{DD}	$V_{SS}^{(1)}$	V_{DD}	V_{DDQ}
K	NC	I/O_{12}	V_{SS}	CLK	V_{SS}	NC	I/O_3
L	I/O_{13}	NC	V_{SS}	NC	$\overline{BW}_1$	I/O_2	NC
M	V_{DDQ}	I/O_{14}	V_{SS}	$\overline{CEN}$	V_{SS}	NC	V_{DDQ}
N	I/O_{15}	NC	V_{SS}	A_1	V_{SS}	I/O_1	NC
P	NC	I/O_{P2}	V_{SS}	A_0	V_{SS}	NC	I/O_0
R	NC	A_5	$\overline{LBO}$	V_{DD}	$V_{SS}^{(1)}$	A_{12}	NC
T	NC	A_{10}	A_{15}	$NC^{(3)}$	A_{14}	A_{11}	ZZ
U	V_{DDQ}	$NC/TMS^{(3)}$	$NC/TDI^{(3)}$	$NC/TCK^{(3)}$	$NC/TDO^{(3)}$	$NC/\overline{TRST}^{(3)}$	V_{DDQ}

5319 tbl 25a

Top View

NOTES:

1. Pins R5 and J5 do not have to be connected directly to V_{SS} as long as the input voltage is $\leq V_{IL}$
2. Pin J3 does not have to be connected directly to V_{DD} as long as the input voltage is $\geq V_{IH}$.
3. U2, U3, U4 and U6 will be pulled internally to V_{DD} if not actively driven. To disable the TAP controller without interfering with normal operation, several settings are possible. U2, U3, U4 and U6 could be tied to VDD or VSS and U5 should be left unconnected. Or all JTAG inputs (TMS, TDI, and TCK and $\overline{TRST}$) U2, U3, U4 and U6 could be left unconnected "NC" and the JTAG circuit will remain disabled from power up.
4. $\overline{TRST}$ is offered as an optional JTAG reset if required in the application. If not needed, can be left floating and will internally be pulled to V_{DD}.

Synchronous Truth Table[1]

$\overline{CEN}$	R/$\overline{W}$	$\overline{CE}_1$, $\overline{CE}_2$[6]	ADV/$\overline{LD}$	$\overline{BW}$x	ADDRESS USED	PREVIOUS CYCLE	CURRENT CYCLE	I/O (One cycle later)
L	L	L	L	Valid	External	X	LOAD WRITE	D[7]
L	H	L	L	X	External	X	LOAD READ	Q[7]
L	X	X	H	Valid	Internal	LOAD WRITE / BURST WRITE	BURST WRITE (Advance burst counter)[2]	D[7]
L	X	X	H	X	Internal	LOAD READ / BURST READ	BURST READ (Advance burst counter)[2]	Q[7]
L	X	H	L	X	X	X	DESELECT or STOP[3]	HIZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HIZ
H	X	X	X	X	X	X	SUSPEND[4]	Previous Value

5319 tbl 08

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. When ADV/$\overline{LD}$ signal is sampled high, the internal burst counter is incremented. The R/$\overline{W}$ signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/$\overline{W}$ signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when either ($\overline{CE}_1$, or $\overline{CE}_2$ is sampled high or CE$_2$ is sampled low) and ADV/$\overline{LD}$ is sampled low at rising edge of clock. The data bus will tri-state one cycle after deselect is initiated.
4. When $\overline{CEN}$ is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
5. To select the chip requires $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE$_2$ = H on these chip enable pins. The chip is deselected if any one of the chip enables is false.
6. Device Outputs are ensured to be in High-Z during device power-up.
7. Q - data read from the device, D - data written to the device.

Partial Truth Table for Writes[1]

OPERATION	R/$\overline{W}$	$\overline{BW}_1$	$\overline{BW}_2$
READ	H	X	X
WRITE ALL BYTES	L	L	L
WRITE BYTE 1 (I/O[0:7], I/OP1)[2]	L	L	H
WRITE BYTE 2 (I/O[8:15], I/OP2)[2]	L	H	L
NO WRITE	L	H	H

5319 tbl 09a

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.

Interleaved Burst Sequence Table ($\overline{LBO}$=V$_{DD}$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address[1]	1	1	1	0	0	1	0	0

5319 tbl 10

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

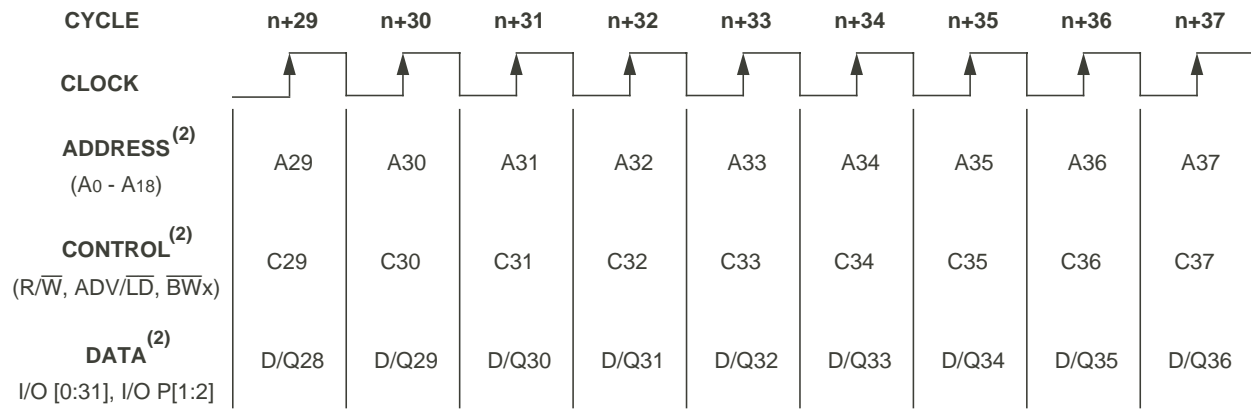## Linear Burst Sequence Table ($\overline{\text{LBO}}$=Vss)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address[1]	1	1	0	0	0	1	1	0

5319 tbl 11

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Functional Timing Diagram[1]

CYCLE	n+29	n+30	n+31	n+32	n+33	n+34	n+35	n+36	n+37
ADDRESS[2] (A_0 - A_{18})	A29	A30	A31	A32	A33	A34	A35	A36	A37
CONTROL[2] (R/$\overline{\text{W}}$, ADV/$\overline{\text{LD}}$, $\overline{\text{BW}}$x)	C29	C30	C31	C32	C33	C34	C35	C36	C37
DATA[2] I/O [0:31], I/O P[1:2]	D/Q28	D/Q29	D/Q30	D/Q31	D/Q32	D/Q33	D/Q34	D/Q35	D/Q36

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NOTES:
1. This assumes $\overline{\text{CEN}}$, $\overline{\text{CE}}_1$, CE_2 and $\overline{\text{CE}}_2$ are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles[2]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}_1$[1]	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	D_1	Load read
n+1	X	X	H	X	L	X	L	Q_0	Burst read
n+2	A_1	H	L	L	L	X	L	Q_{0+1}	Load read
n+3	X	X	L	H	L	X	L	Q_1	Deselect or STOP
n+4	X	X	H	X	L	X	X	Z	NOOP
n+5	A_2	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	L	Q_2	Burst read
n+7	X	X	L	H	L	X	L	Q_{2+1}	Deselect or STOP
n+8	A_3	L	L	L	L	L	X	Z	Load write
n+9	X	X	H	X	L	L	X	D_3	Burst write
n+10	A_4	L	L	L	L	L	X	D_{3+1}	Load write
n+11	X	X	L	H	L	X	X	D_4	Deselect or STOP
n+12	X	X	H	X	L	X	X	Z	NOOP
n+13	A_5	L	L	L	L	L	X	Z	Load write
n+14	A_6	H	L	L	L	X	X	D_5	Load read
n+15	A_7	L	L	L	L	L	L	Q_6	Load write
n+16	X	X	H	X	L	L	X	D_7	Burst write
n+17	A_8	H	L	L	L	X	X	D_{7+1}	Load read
n+18	X	X	H	X	L	X	L	Q_8	Burst read
n+19	A_9	L	L	L	L	L	L	Q_{8+1}	Load write

5319 tbl 12

NOTES:

1. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. CE2 timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.

2. H = High; L = Low; X = Don't Care; Z = High Impedence.

Read Operation[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}_1$[2]	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	X	X	L	Q_0	Contents of Address A_0 Read Out

5319 tbl 13

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. CE_2 timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.

Burst Read Operation[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}_1$[2]	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+2	X	X	H	X	L	X	L	Q_{0+1}	Address A_{0+1} Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q_{0+2}	Address A_{0+2} Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q_{0+3}	Address A_{0+3} Read Out, Load A_1
n+5	A_1	H	L	L	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+6	X	X	H	X	L	X	L	Q_1	Address A_1 Read Out, Inc. Count
n+7	A_2	H	L	L	L	X	L	Q_{1+1}	Address A_{1+1} Read Out, Load A_2

5319 tbl 14

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. CE_2 timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.

Write Operation[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}_1$[2]	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	D_0	Write to Address A_0

5319 tbl 15

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. CE_2 timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.

Burst Write Operation[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}_1$[2]	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	D_0	Address A_0 Write, Inc. Count
n+2	X	X	H	X	L	L	X	D_{0+1}	Address A_{0+1} Write, Inc. Count
n+3	X	X	H	X	L	L	X	D_{0+2}	Address A_{0+2} Write, Inc. Count
n+4	X	X	H	X	L	L	X	D_{0+3}	Address A_{0+3} Write, Load A_1
n+5	A_1	L	L	L	L	L	X	D_0	Address A_0 Write, Inc. Count
n+6	X	X	H	X	L	L	X	D_1	Address A_1 Write, Inc. Count
n+7	A_2	L	L	L	L	L	X	D_{1+1}	Address A_{1+1} Write, Load A_2

5319 tbl 16

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. CE_2 timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.

Read Operation with Clock Enable Used[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}_1$[2]	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address A_0 and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A_1	H	L	L	L	X	L	Q_0	Address A_0 Read out, Load A_1
n+3	X	X	X	X	H	X	L	Q_0	Clock Ignored. Data Q_0 is on the bus.
n+4	X	X	X	X	H	X	L	Q_0	Clock Ignored. Data Q_0 is on the bus.
n+5	A_2	H	L	L	L	X	L	Q_1	Address A_1 Read out, Load A_2
n+6	A_3	H	L	L	L	X	L	Q_2	Address A_2 Read out, Load A_3
n+7	A_4	H	L	L	L	X	L	Q_3	Address A_3 Read out, Load A_4

5319 tbl 17

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. CE2 timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.

Write Operation with Clock Enable Used[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}_1$[2]	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address A_0 and Control meet setup.
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A_1	L	L	L	L	L	X	D_0	Write data D_0, Load A_1.
n+3	X	X	X	X	H	X	X	X	Clock Ignored.
n+4	X	X	X	X	H	X	X	X	Clock Ignored.
n+5	A_2	L	L	L	L	L	X	D_1	Write Data D_1, Load A_2
n+6	A_3	L	L	L	L	L	X	D_2	Write Data D_2, Load A_3
n+7	A_4	L	L	L	L	L	X	D_3	Write Data D_3, Load A_4

5319 tbl 18

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. CE2 timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.

Read Operation with Chip Enable Used[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}_1$[2]	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O[3]	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	Z	Deselected.
n+2	A0	H	L	L	L	X	X	Z	Address A0 and Control meet setup.
n+3	X	X	L	H	L	X	L	Q0	Address A0 read out, Deselected.
n+4	A1	H	L	L	L	X	X	Z	Address A1 and Control meet setup.
n+5	X	X	L	H	L	X	L	Q1	Address A1 read out, Deselected.
n+6	X	X	L	H	L	X	X	Z	Deselected.
n+7	A2	H	L	L	L	X	X	Z	Address A2 and Control meet setup.
n+8	X	X	L	H	L	X	L	Q2	Address A2 read out, Deselected.
n+9	X	X	L	H	L	X	X	Z	Deselected.

5319 tbl 19

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. CE2 timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.
3. Device outputs are ensured to be in High-Z during device power-up.

Write Operation with Chip Enable Used[1]

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$[2]	$\overline{CEN}$	$\overline{BW}x$	$\overline{OE}$	I/O	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	Z	Deselected.
n+2	A0	L	L	L	L	L	X	Z	Address A0 and Control meet setup
n+3	X	X	L	H	L	X	X	D0	Data D0 Write In, Deselected.
n+4	A1	L	L	L	L	L	X	Z	Address A1 and Control meet setup
n+5	X	X	L	H	L	X	X	D1	Data D1 Write In, Deselected.
n+6	X	X	L	H	L	X	X	Z	Deselected.
n+7	A2	L	L	L	L	L	X	Z	Address A2 and Control meet setup
n+8	X	X	L	H	L	X	X	D2	Data D2 Write In, Deselected.
n+9	X	X	L	H	L	X	X	Z	Deselected.

5319 tbl 20

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE2 = L.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (VDD = 2.5V±5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$|I_{LI}|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$|I_{LI}|$	$\overline{LBO}$, JTAG and ZZ Input Leakage Current[1]	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$|I_{LO}|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +6mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -6mA, V_{DD} = Min.	2.0	—	V

5319 tbl 21

NOTE:

1. The $\overline{LBO}$, TMS, TDI, TCK and $\overline{TRST}$ pins will be internally pulled to V_{DD} and the ZZ pin will be internally pulled to V_{SS} if they are not actively driven in the application.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1] (VDD = 2.5V±5%)

Symbol	Parameter	Test Conditions	7.5ns		8.5ns		Unit
			Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, ADV/$\overline{LD}$ = X, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f$_{MAX}$[2]	275	295	225	245	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0[2,3]	40	60	40	60	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f$_{MAX}$[2,3]	105	125	95	115	mA
I_{SB3}	Idle Power Supply Current	Device Selected, Outputs Open, $\overline{CEN} \geq V_{IH}$, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f$_{MAX}$[2,3]	60	80	60	80	mA
I_{ZZ}	Full Sleep Mode Supply Current	Device Selected, Outputs Open, $\overline{CEN} \leq V_{IH}$, V_{DD} = Max., ZZ $\geq V_{HD}$ $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f$_{MAX}$[2,3]	40	60	40	60	mA

5319 tbl 22a

NOTES:

1. All values are maximum guaranteed values.
2. At f = f$_{MAX}$, inputs are cycling at the maximum frequency of read cycles of 1/t$_{CYC}$; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} – 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} – 0.2V, V_{LD} = 0.2V.
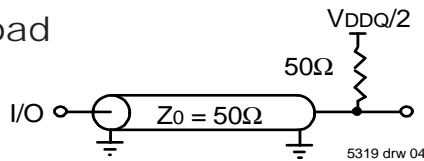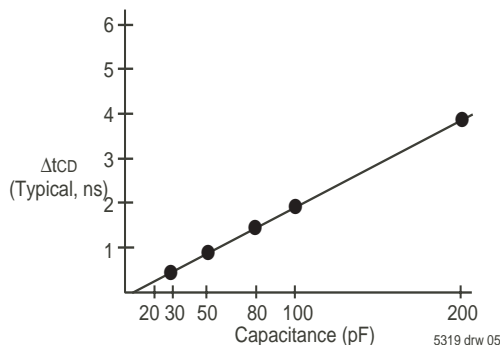
AC Test Load

Figure 1. AC Test Load

5319 drw 04

Figure 2. Lumped Capacitive Load, Typical Derating

5319 drw 05

AC Test Conditions

Input Pulse Levels	0 to 2.5V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	(V_{DDQ}/2)
Output Reference Levels	(V_{DDQ}/2)
Output Load	Figure 1

5319 tbl 23

AC Electrical Characteristics

(V$_{DD}$ = 2.5V±5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	7.5ns Min.	7.5ns Max.	8.5ns Min.	8.5ns Max.	Unit
t$_{CYC}$	Clock Cycle Time	10	—	11	—	ns
t$_{CH}$[1]	Clock High Pulse Width	2.5	—	3.0	—	ns
t$_{CL}$[1]	Clock Low Pulse Width	2.5	—	3.0	—	ns
Output Parameters						
t$_{CD}$	Clock High to Valid Data	—	7.5	—	8.5	ns
t$_{CDC}$	Clock High to Data Change	2	—	2	—	ns
t$_{CLZ}$[2,3,4]	Clock High to Output Active	3	—	3	—	ns
t$_{CHZ}$[2,3,4]	Clock High to Data High-Z	—	5	—	5	ns
t$_{OE}$	Output Enable Access Time	—	5	—	5	ns
t$_{OLZ}$[2,3]	Output Enable Low to Data Active	0	—	0	—	ns
t$_{OHZ}$[2,3]	Output Enable High to Data High-Z	—	5	—	5	ns
Set Up Times						
t$_{SE}$	Clock Enable Setup Time	2.0	—	2.0	—	ns
t$_{SA}$	Address Setup Time	2.0	—	2.0	—	ns
t$_{SD}$	Data In Setup Time	2.0	—	2.0	—	ns
t$_{SW}$	Read/Write (R/$\overline{W}$) Setup Time	2.0	—	2.0	—	ns
t$_{SADV}$	Advance/Load (ADV/$\overline{LD}$) Setup Time	2.0	—	2.0	—	ns
t$_{SC}$	Chip Enable/Select Setup Time	2.0	—	2.0	—	ns
t$_{SB}$	Byte Write Enable ($\overline{BW}$x) Setup Time	2.0	—	2.0	—	ns
Hold Times						
t$_{HE}$	Clock Enable Hold Time	0.5	—	0.5	—	ns
t$_{HA}$	Address Hold Time	0.5	—	0.5	—	ns
t$_{HD}$	Data In Hold Time	0.5	—	0.5	—	ns
t$_{HW}$	Read/Write (R/$\overline{W}$) Hold Time	0.5	—	0.5	—	ns
t$_{HADV}$	Advance/Load (ADV/$\overline{LD}$) Hold Time	0.5	—	0.5	—	ns
t$_{HC}$	Chip Enable/Select Hold Time	0.5	—	0.5	—	ns
t$_{HB}$	Byte Write Enable ($\overline{BW}$x) Hold Time	0.5	—	0.5	—	ns

5319 tbl 24a

NOTES:
1. Measured as HIGH above 0.6V$_{DDQ}$ and LOW below 0.4V$_{DDQ}$.
2. Transition is measured ±200mV from steady-state.
3. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
4. To avoid bus contention, the output buffers are designed such that t$_{CHZ}$ (device turn-off) is about 1ns faster than t$_{CLZ}$ (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t$_{CLZ}$ is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 2.625V) than t$_{CHZ}$, which is a Max. parameter (worse case at 70 deg. C, 2.375V).

Timing Waveform of Read Cycle[1,2,3,4]
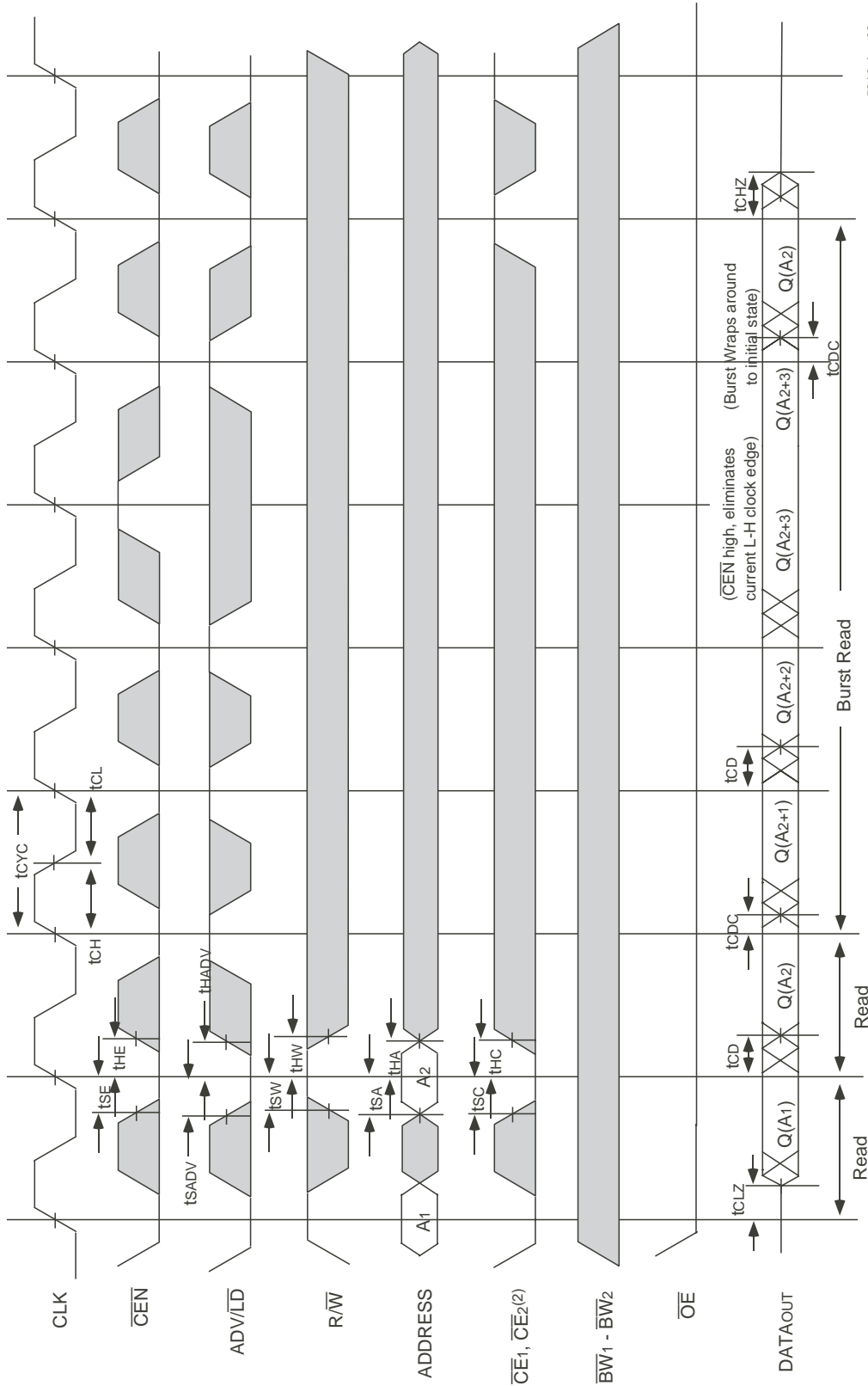
5319 drw 06a

NOTES:
1. Q (A₁) represents the first output from the external address A₁. Q (A₂) represents the first output from the external address A₂; Q (A₂₊₁) represents the next output data in the burst sequence of the base address A₂, etc. where address bits A₀ and A₁ are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. CE₂ timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE₂ is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
4. R/$\overline{W}$ is don't care when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.

Timing Waveform of Write Cycles[1,2,3,4,5]
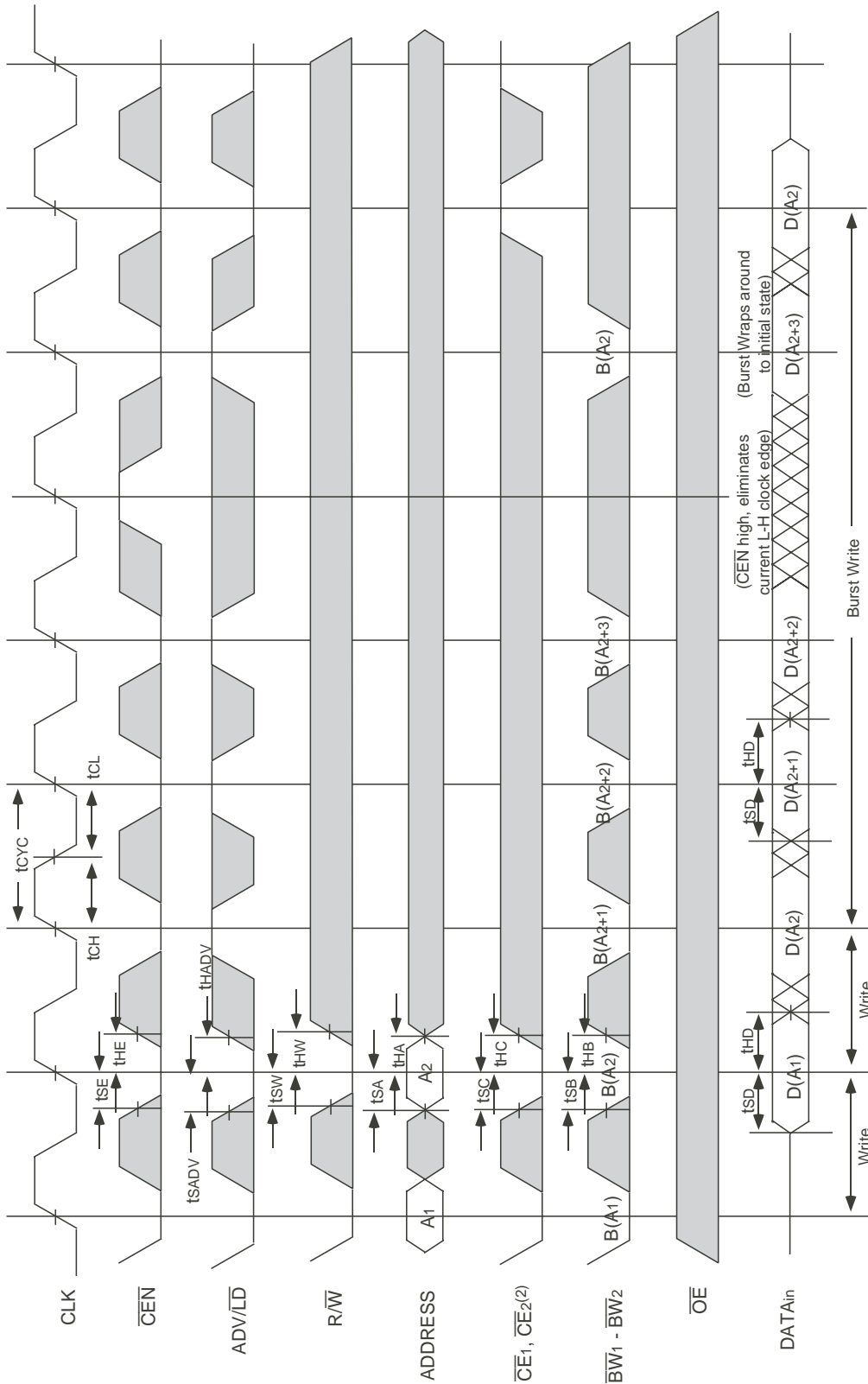
5319 drw 07a

NOTES:
1. D (A1) represents the first input to the external address A1. D (A2) represents the first input to the external address A2; D (A2+1) represents the next input data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. CE2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
4. R/$\overline{W}$ is don't care when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals ($\overline{BW}$x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

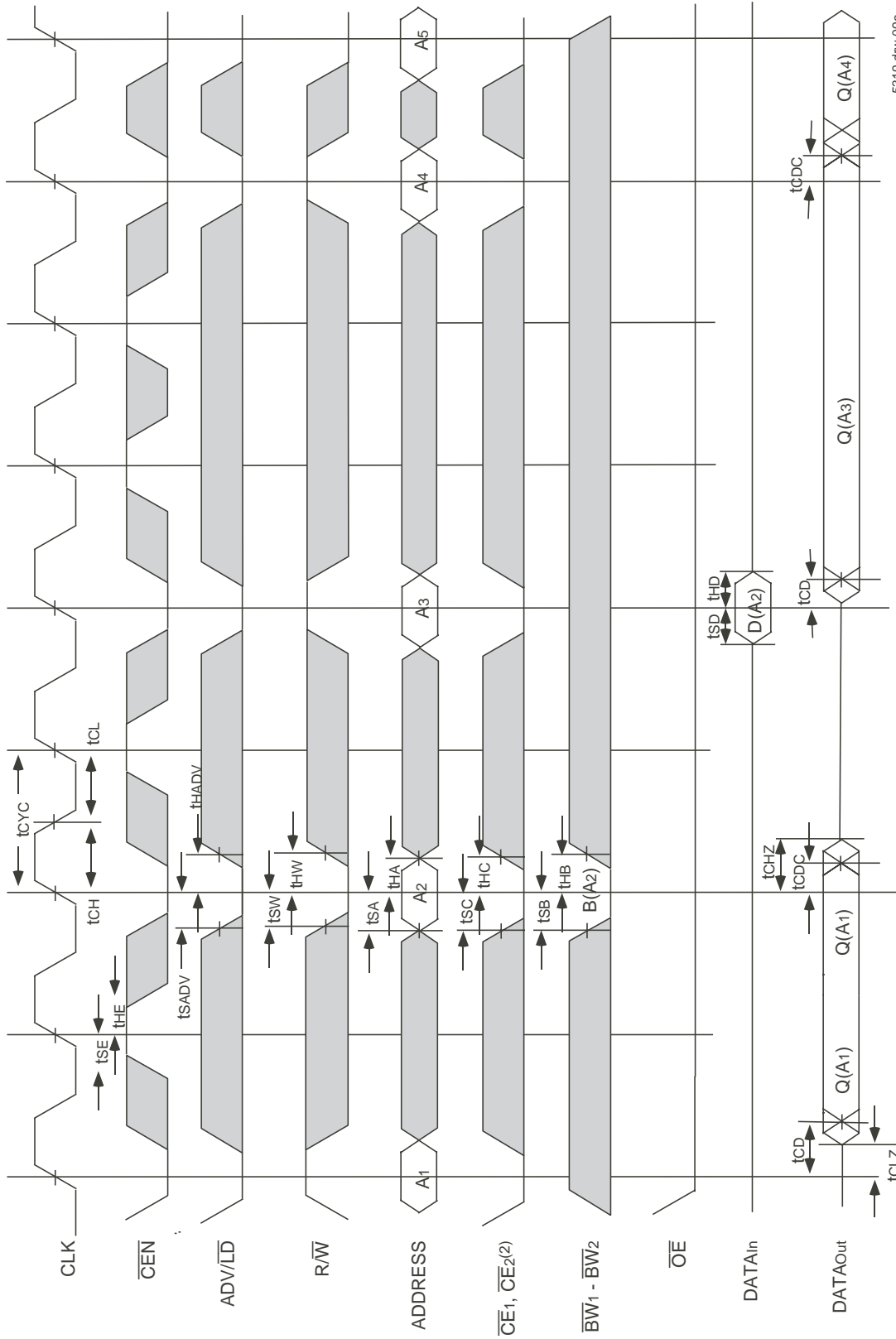# Timing Waveform of Combined Read and Write Cycles[1,2,3]
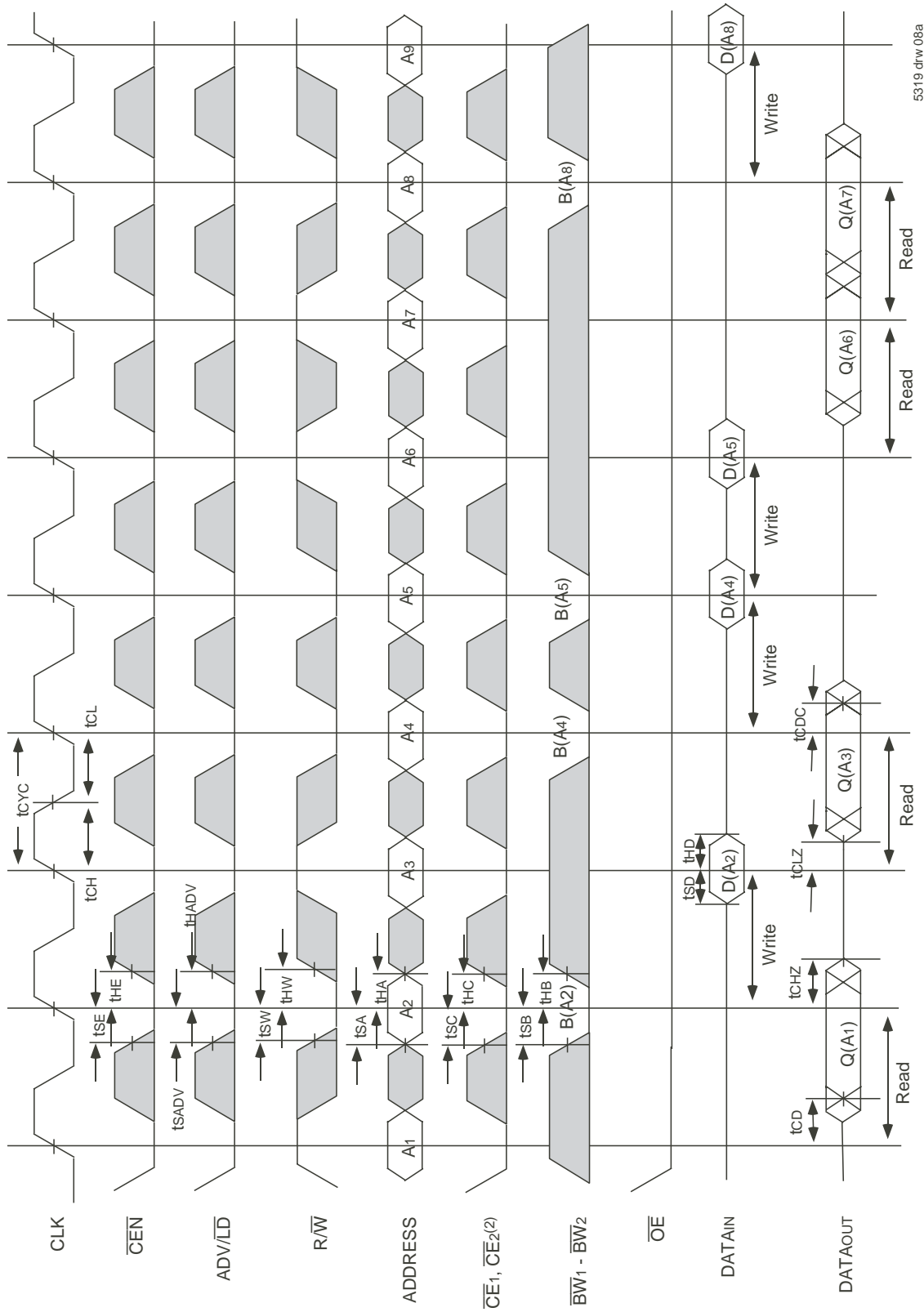
5319 drw 08a

Signals: CLK, $\overline{CEN}$, ADV/$\overline{LD}$, R/$\overline{W}$, ADDRESS, $\overline{CE}_1$, $\overline{CE}_2$[2], $\overline{BW}_1$ - $\overline{BW}_2$, $\overline{OE}$, DATA_IN, DATA_OUT

Timing parameters: tCYC, tCH, tCL, tSE, tHE, tSADV, tHADV, tSW, tHW, tSA, tHA, tSC, tHC, tSB, tHB, tSD, tHD, tCD, tCHZ, tCLZ, tCDC

Address labels: A1, A2, A3, A4, A5, A6, A7, A8, A9
Byte write: B(A2), B(A4), B(A5), B(A8)
Data in: D(A2), D(A4), D(A5), D(A8)
Data out: Q(A1), Q(A3), Q(A6), Q(A7)

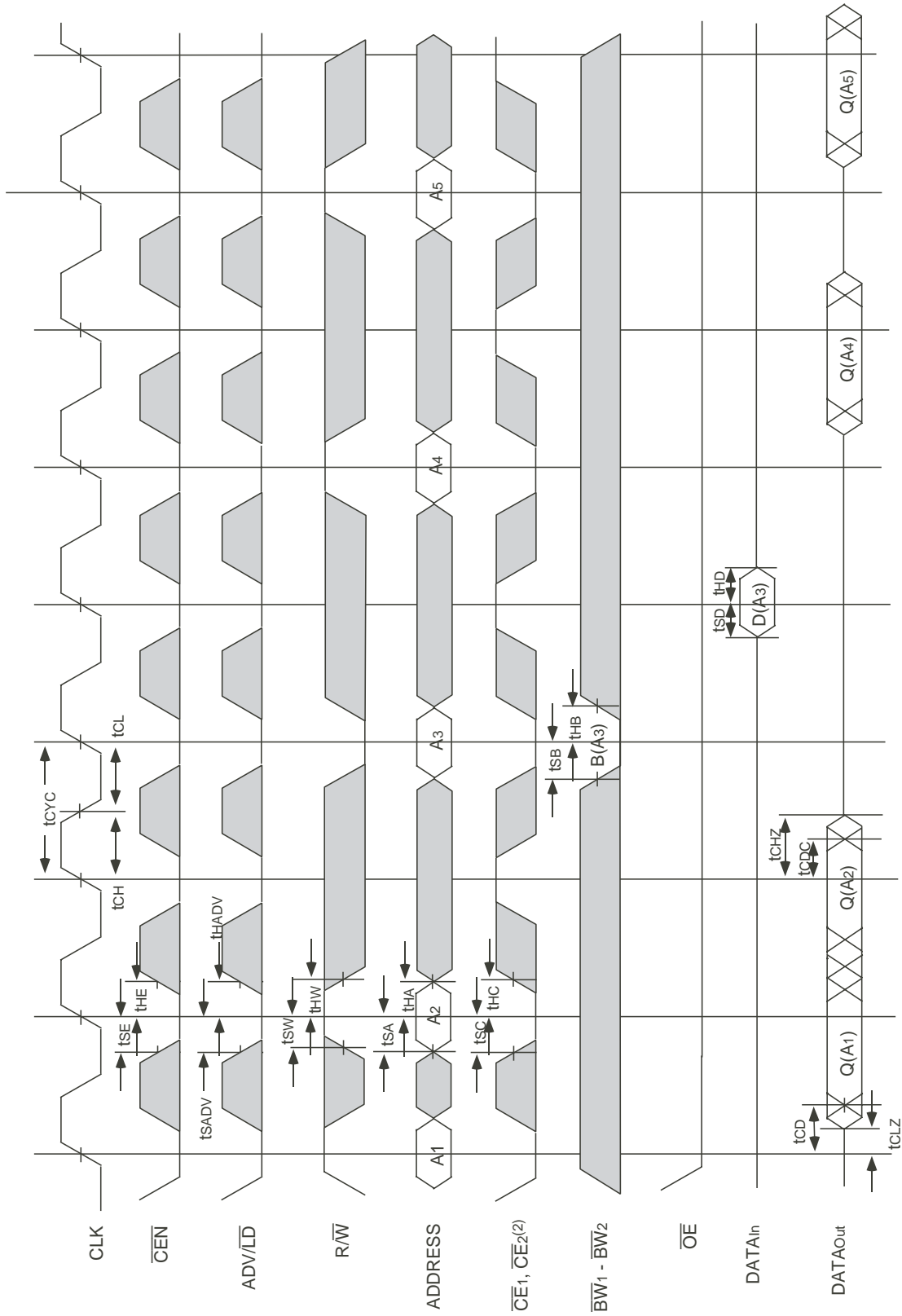Read / Write / Read / Read / Write / Write / Read / Write / Read labels

NOTES:
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. $\overline{CE}_2$ timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

Timing Waveform of $\overline{\text{CEN}}$ Operation[1,2,3,4]

5319 drw 09a

Signals: CLK, $\overline{\text{CEN}}$, ADV/$\overline{\text{LD}}$, R/$\overline{\text{W}}$, ADDRESS, $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$[2], $\overline{\text{BW}}_1$ - $\overline{\text{BW}}_2$, $\overline{\text{OE}}$, DATAin, DATAout

Timing parameters: tCYC, tCL, tCH, tSE, tHE, tSADV, tHADV, tSW, tHW, tSA, tHA, tSC, tHC, tSB, tHB, tSD, tHD, tCD, tCLZ, tCHZ, tCDC

Addresses/data: A1, A2, A3, A4, A5, B(A2), D(A2), Q(A1), Q(A3), Q(A4)

NOTES:
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. $\overline{\text{CE}}_2$ timing transitions are identical but inverted to the $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ signals. For example, when $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ are LOW on this waveform, CE2 is HIGH.
3. $\overline{\text{CEN}}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{\text{BW}}$x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{\text{W}}$ signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

# Timing Waveform of $\overline{CS}$ Operation[1,2,3,4]

5319 drw 10a

NOTES:
1. Q (A1) represents the first output from the external address A1. D (A3) represents the input data to the SRAM corresponding to address A3 etc.
2. CE2 timing transitions are identical but inverted to the $\overline{CE_1}$ and $\overline{CE_2}$ signals.
3. When either one of the Chip enables ($\overline{CE_1}$, CE2, $\overline{CE_2}$) is sampled inactive at the rising clock edge, a deselect cycle is initiated. The data-bus tri-states one cycle after the initiation of the deselect cycle. This allows for any pending data transfers (reads or writes) to be completed.
4. Individual Byte Write signals ($\overline{BW_x}$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

JTAG Interface Specification

M5319 drw 01
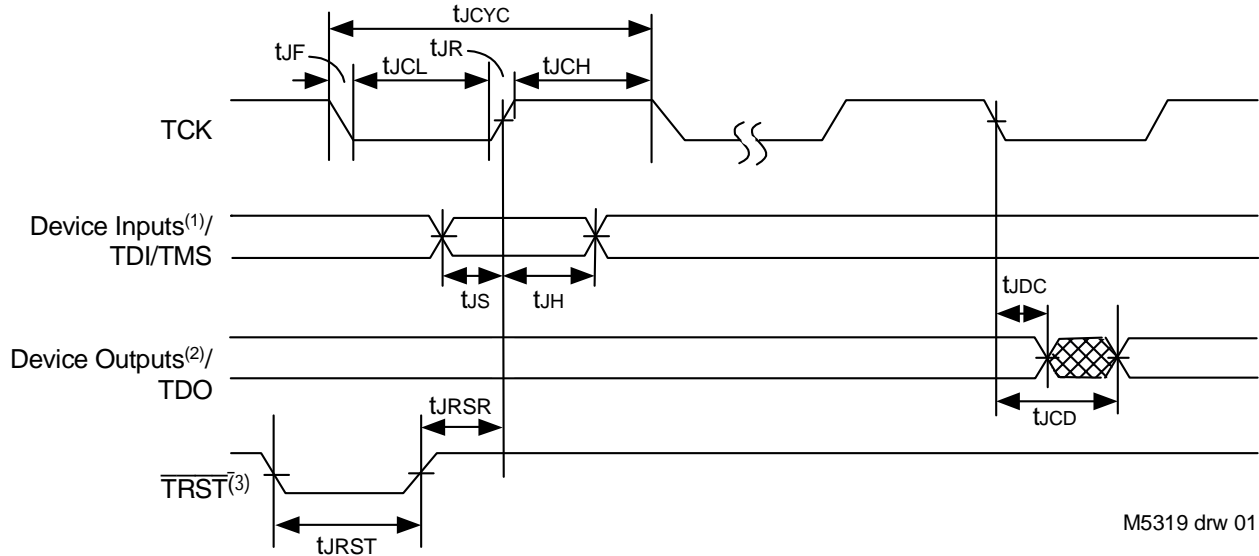
NOTES:
1. Device inputs = All device inputs except TDI, TMS and $\overline{TRST}$.
2. Device outputs = All device outputs except TDO.
3. During power up, $\overline{TRST}$ could be driven low or not be used since the JTAG circuit resets automatically. $\overline{TRST}$ is an optional JTAG reset.

JTAG AC Electrical Characteristics[1,2,3,4]

Symbol	Parameter	Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	5[1]	ns
t_{JF}	JTAG Clock Fall Time	—	5[1]	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	20	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	25	—	ns
t_{JH}	JTAG Hold	25	—	ns

I5319 tbl 01

NOTES:
1. Guaranteed by design.
2. AC Test Load (Fig. 1) on external output signals.
3. Refer to AC Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
JTAG Identification (JIDR)	32
Boundary Scan (BSR)	Note (1)

I5319 tbl 03

NOTE:
1. The Boundary Scan Descriptive Language (BSDL) file for this device is available by contacting your local IDT sales representative.

JTAG Identification Register Definitions

| Instruction Field	Value	Description
Revision Number (31:28)	0x2	Reserved for version number.
IDT Device ID (27:12)	0x223	Defines IDT part number 71T75902
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT.
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register.

I5319 tbl 02a

Available JTAG Instructions

Instruction	Description	OPCODE
EXTEST	Forces contents of the boundary scan cells onto the device outputs[1]. Places the boundary scan register (BSR) between TDI and TDO.	0000
SAMPLE/PRELOAD	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs[2] and outputs[1] to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.	0001
DEVICE_ID	Loads the JTAG ID register (JIDR) with the vendor ID code and places the register between TDI and TDO.	0010
HIGHZ	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.	0011
RESERVED	Several combinations are reserved. Do not use codes other than those identified for EXTEST, SAMPLE/PRELOAD, DEVICE_ID, HIGHZ, CLAMP, VALIDATE and BYPASS instructions.	0100
RESERVED		0101
RESERVED		0110
RESERVED		0111
CLAMP	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.	1000
RESERVED	Same as above.	1001
RESERVED		1010
RESERVED		1011
RESERVED		1100
VALIDATE	Automatically loaded into the instruction register whenever the TAP controller passes through the CAPTURE-IR state. The lower two bits '01' are mandated by the IEEE std. 1149.1 specification.	1101
RESERVED	Same as above.	1110
BYPASS	The BYPASS instruction is used to truncate the boundary scan register as a single bit in length.	1111

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NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{TRST}$.
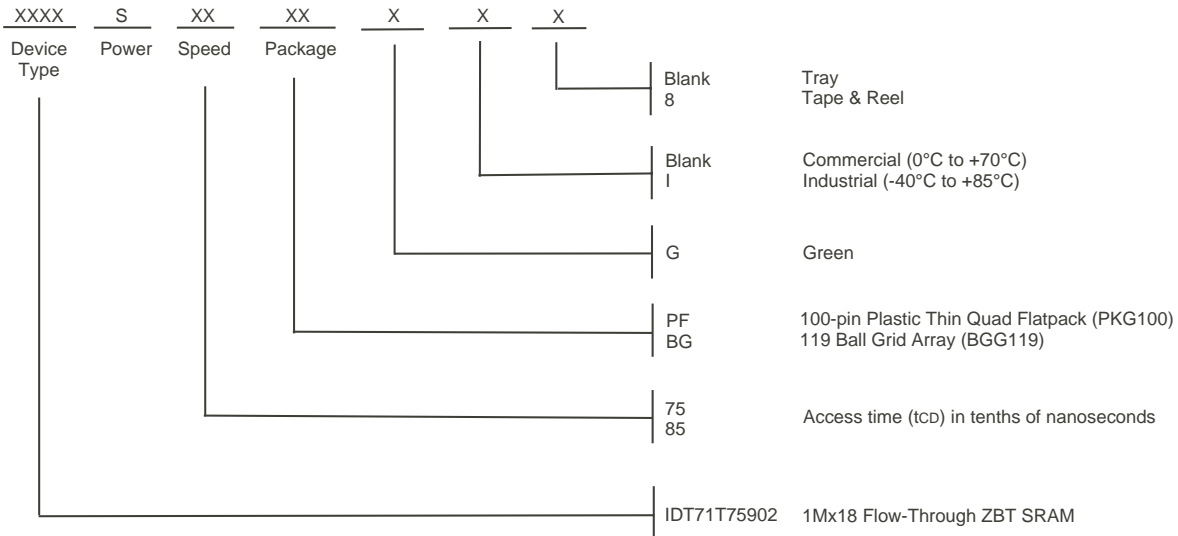
Timing Waveform of $\overline{OE}$ Operation[1]
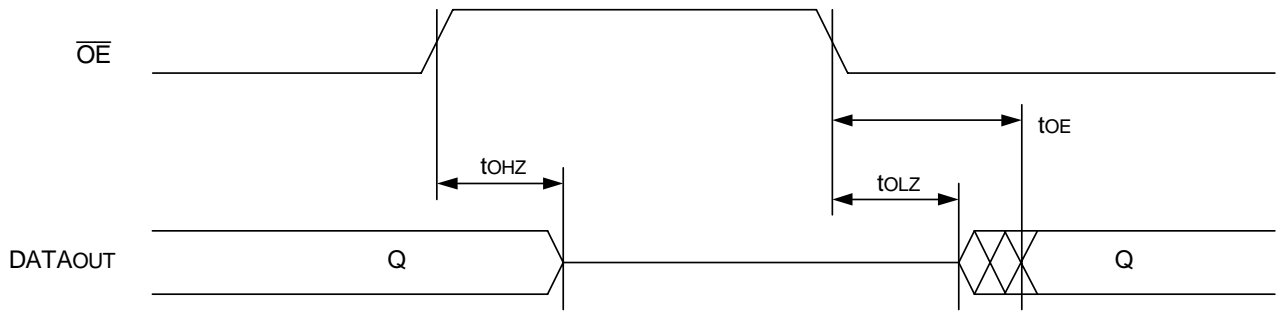
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NOTE:
1. A read operation is assumed to be in progress.

Ordering Information

5319 drw 12

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
75	71T75902S75BG	BG119	PBGA	C
	71T75902S75BG8	BG119	PBGA	C
	71T75902S75BGG	BGG119	PBGA	C
	71T75902S75BGG8	BGG119	PBGA	C
	71T75902S75PFG	PKG100	TQFP	C
	71T75902S75PFG8	PKG100	TQFP	C
	71T75902S75PFGI	PKG100	TQFP	I
	71T75902S75PFGI8	PKG100	TQFP	I
85	71T75902S85BG	BG119	PBGA	C
	71T75902S85BG8	BG119	PBGA	C
	71T75902S85BGG	BGG119	PBGA	C
	71T75902S85BGG8	BGG119	PBGA	C

5319t27.tbl

Datasheet Document History

Rev	Date	Pages	Description
0	05/25/00		Created Advance Information Datasheet
1	08/24/01	p. 1, 25	Removed reference of BQ165 package
		p. 8	Removed page of the 165 BGA pin configuration
		p. 24	Removed page of the 165 BGA package diagram outline
2	10/16/01	p. 7	Corrected 3.3V to 2.5V in Note 3
3	12/21/01	p. 5-7	Added clarification to JTAG pins, allow for NC. Added 36M address pin locations
4	05/29/02	p. 21	Corrected 100-pin TQFP package drawing
5	06/07/02	p. 1-4,7,14,21,22	Added complete JTAG functionality.
		p. 2,14	Added notes for ZZ pin internal pulldown and ZZ leakage current.
		p. 14	Updated ISB3 power supply current from 40 to 60mA for all speeds.
6	11/19/02	p.1-26	Changed datasheet from Advanced information to final release.
7	05/23/03	p.5,6,14,15,25	Added I-temp to the datasheet.
		p.6	Updated 165 BGA table.
8	04/01/04	p.1	Updated logo with new design.
		p.5,6	Clarified ambient and case operating temperatures.
		p.7	Updated I/O pin number order for the 119 BGA.
		p.24	Updated 119BGA Package Diagram Drawing.
9	02/20/09	p.25	Removed "IDT" from orderable parts number
10	09/08/17	p.1-23	Removed IDT71T75702 & 512K x 36 throughout the datasheet
		p. 1	In Features: Added text: "Green parts available, see Ordering Information"
			Moved the FBD from page 3 to page 1 & the Pin Description Summary from page 1 to page 2
			& the Pin Definitions from page 2 to page 3 in accordance with our standard datasheet format
		p.2	Description text corrected grammatical errors
		p.2-3	Removed $\overline{BW}_4$ & replaced with $\overline{BW}_2$, removed I/O$_{P4}$ and replaced with I/O$_{P2}$ in the Pin Description
			Summary & Pin Definitions tables
			Updated "36-bit word" to "18-bit word" for $\overline{BW}_1$-$\overline{BW}_2$ in Pin Definitions table
		p.3	Removed Functional Block Diagram for 512K x 36
		p.4	Removed fBGA capacitance table as this package is no longer offered for this device
		p.5	Added IDT logo, device & in accordance with the packaging code added PKG100
		p.5	Removed Pin Configuration 512K x 36, PKG100
		p.5	Removed footnote 4. for Pin Configuration 1M x 18, 119BGA
		p.7	Removed Pin Configuration 512K X 36, 119BGA
		p.7	Removed Description columns for $\overline{BW}_3$ and $\overline{BW}_4$ and removed Write Byte 3 and Write Byte 4 rows
			from Partial Truth Table for Writes and removed footnote 3
		p.8	Replaced P[1:4] with P[1:2] in Functional Timing Diagram
		p.13	Removed 8.0ns column from DC Electrical Chars Table
		p.14	Removed 8.0ns column from AC Electrical Chars Table
		p.15-19	Removed $\overline{BW}_1$ - $\overline{BW}_4$ from all of the Timing Waveforms and replaced with $\overline{BW}_1$ - $\overline{BW}_2$
		p.21	Changes made to the JTAG Identification Register Definitions Table for Instruction
			Field IDT Device ID (27:12), where Value 0x221 was removed and 71T75702 was removed
			from the Description column
		p.22	Ordering Information added Tray, T&R and Green indicators
			Updated package codes in Ordering Information for TQFP from PK100 to PKG100
			& for BGA from BGA119 to BGG119
			Ordering Information removed 80 speed grade
			Added Orderable Part Information from idt.com
		p.23-24	Removed Package Diagram Outlines for TQFP and BGA