

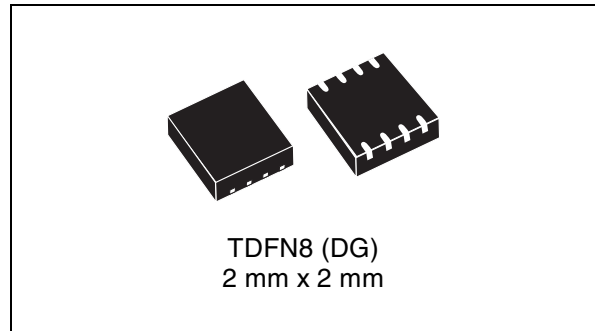


## STM6520

### Dual push-button Smart Reset™ with push-button controlled output delay

#### Features

- Dual Smart Reset™ push-button inputs, with user-selectable extended reset setup delay (by two-state input logic):  $t_{SRC} = 6, 10 \text{ s (min.)}$
- Push-button controlled reset pulse duration (no fixed nor minimum pulse width guaranteed)
- No power-on reset
- Dual reset outputs
  - $\overline{RST1}$  - active-low, open-drain
  - RST2 - active-high, push-pull
- Fixed Smart Reset™ input logic voltage levels
- Broad operating voltage range 1.65 V to 5.5 V, inactive reset output levels valid down to 1.0 V
- Low supply current 1.5  $\mu\text{A}$
- Operating temperature:  $-30 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$
- TDFN8 package: 2 mm x 2 mm x 0.75 mm
- RoHS compliant



#### Applications

- Mobile phones, smartphones
- e-books
- MP3 players
- Games
- Portable navigation devices
- Any application that requires delayed reset push-button(s) response for improved system stability

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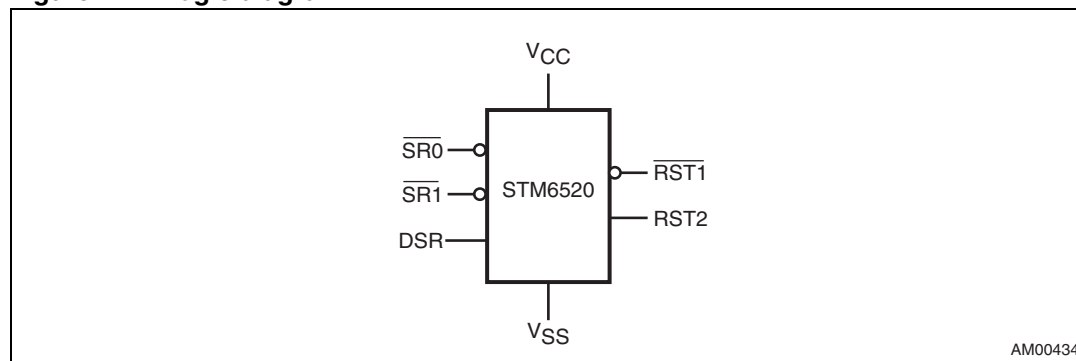
# 1 Description

The Smart Reset™ devices provide a useful feature that ensures inadvertent short reset push-button closures do not cause system resets. This is done by implementing extended Smart Reset™ input delay time ( $t_{SRC}$ ) and combined push-button inputs, which together ensures a safe reset and eliminates the need for a specific dedicated reset button.

This reset configuration provides versatility and allows the application to discriminate between a software generated interrupt and a hard system reset. When the input push-buttons are connected to microcontroller interrupt inputs, and are closed for a short time, the processor can only be interrupted. If the system still does not respond properly, continuing to keep the push-buttons closed for the extended setup time  $t_{SRC}$  causes a hard reset of the processor through the reset outputs.

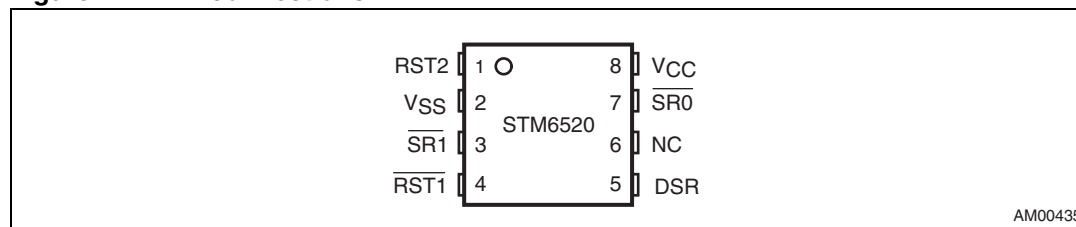
The STM6520 has two combined delayed Smart Reset™ inputs ( $\overline{SR0}$ ,  $\overline{SR1}$ ) with two user-selectable delayed Smart Reset™ setup time ( $t_{SRC}$ ) options of 7.5 s and 12.5 s typ., selected by a dual-state Smart Reset™ DSR input pin. When DSR is connected to ground,  $t_{SRC} = 7.5$  s, when connected to  $V_{CC}$ ,  $t_{SRC} = 12.5$  s (typ.). There are two reset outputs, both going active simultaneously after both of the Smart Reset™ inputs were held active for the selected  $t_{SRC}$  delay time. The outputs remain asserted until either or both inputs go to inactive logic level (for this device the output reset pulse duration is fully push-button controlled, meaning neither fixed nor minimum reset pulse width, nor power-on reset pulse is implemented). The first reset output,  $\overline{RST1}$ , is active-low, open-drain; the second reset output, RST2, is active-high, push-pull. The device fully operates over a broad  $V_{CC}$  range 1.65 to 5.5 V. Below 1.575 V typ. the inputs are ignored and outputs are deasserted; the deasserted reset output levels are then valid down to 1.0 V.

**Figure 1. Logic diagram**



AM00434

**Figure 2. Pin connections**



AM00435

## 2 Device overview

**Table 1. Signal names**

Symbol	Input/output	Description
$\overline{\text{RST1}}$	Output	First reset output, active-low, open-drain.
RST2	Output	Second reset output, active-high, push-pull.
$\overline{\text{SR0}}$	Input	Primary push-button Smart Reset™ input. Active-low.
$\overline{\text{SR1}}$	Input	Secondary push-button Smart Reset™ input. Active-low.
DSR	Input	A dual-state Smart Reset™ input delay selection pin. When connected to ground, $t_{\text{SRC}} = 7.5 \text{ s}$ ; when connected to $V_{\text{CC}}$ , $t_{\text{SRC}} = 12.5 \text{ s}$ (typ.). DSR is a DC-type input, intended to be either permanently grounded or permanently connected to $V_{\text{CC}}$ .
$V_{\text{CC}}$	Supply voltage	Positive supply voltage for the device. A 0.1 $\mu\text{F}$ decoupling ceramic capacitor is recommended to be connected between $V_{\text{CC}}$ and $V_{\text{SS}}$ pins.
$V_{\text{SS}}$	Supply ground	Ground
NC		No connect (not bonded; should be connected to $V_{\text{SS}}$ ).

## 3 Pin descriptions

### 3.1 Power supply ( $V_{CC}$ )

This pin is used to provide power to the Smart Reset™ device. A 0.1  $\mu\text{F}$  ceramic decoupling capacitor is recommended to be connected between the  $V_{CC}$  and  $V_{SS}$  pins, as close to the STM6520 device as possible.

### 3.2 Ground ( $V_{SS}$ )

This is the ground pin for the device.

### 3.3 Smart Reset™ inputs ( $\overline{\text{SR0}}$ , $\overline{\text{SR1}}$ )

Push-button Smart Reset™ inputs, active-low. Both inputs need to be asserted simultaneously for at least  $t_{\text{SRC}}$  to activate the reset outputs.

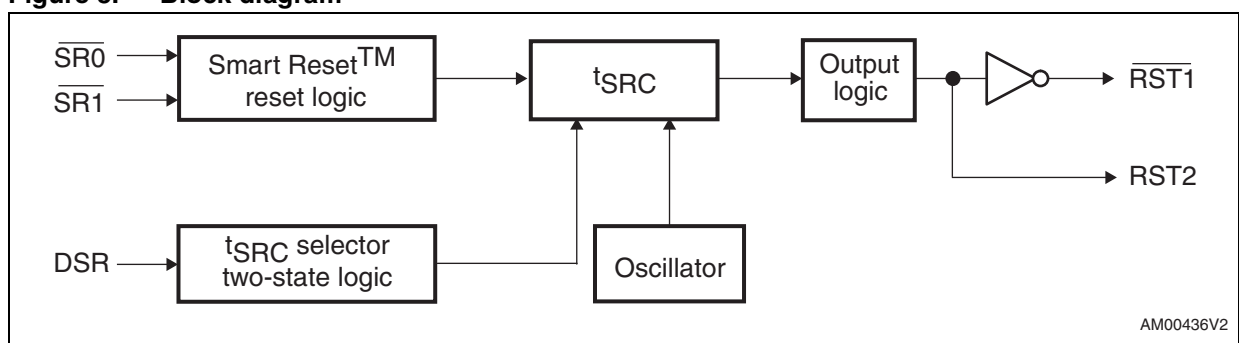
### 3.4 User-selectable Smart Reset™ delay (DSR)

An input that allows the user to program the setup time ( $t_{\text{SRC}}$ ) for which both the push-buttons need to be pressed to activate the reset outputs. Controlled by different voltage levels on the DSR pin: when connected to ground,  $t_{\text{SRC}} = 7.5 \text{ s}$ , when connected to  $V_{CC}$ ,  $t_{\text{SRC}} = 12.5 \text{ s}$  (typ.). DSR is a DC-type input, intended to be either permanently grounded or permanently connected to  $V_{CC}$ .

### 3.5 Reset outputs ( $\overline{\text{RST1}}$ , $\text{RST2}$ )

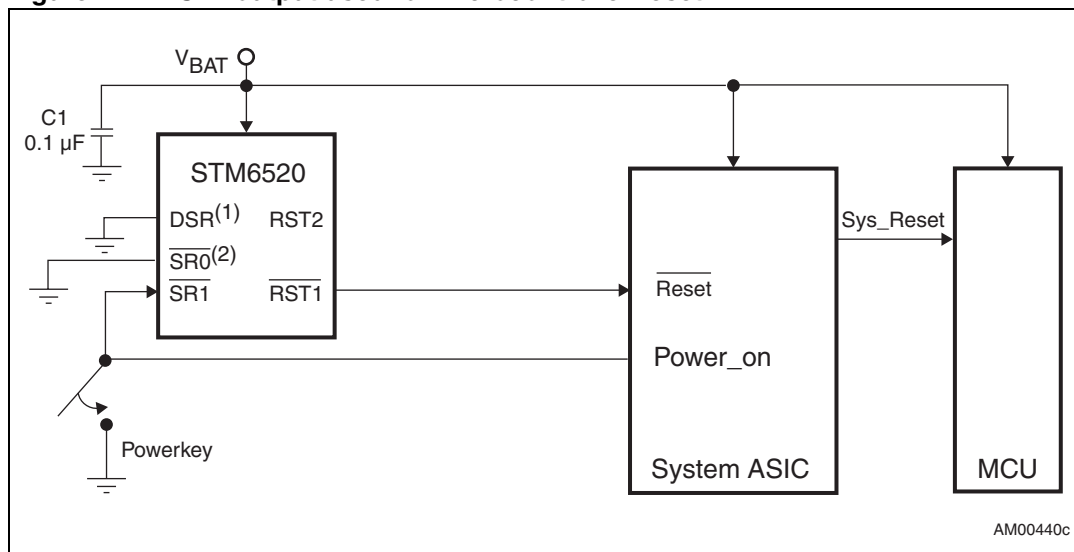
$\overline{\text{RST1}}$  is active-low, open-drain,  $\text{RST2}$  active-high, push-pull. Neither fixed nor minimum output reset pulse duration, nor power-on reset is implemented. Releasing any of the push-buttons while reset outputs are active, causes both outputs to deassert.

Figure 3. Block diagram



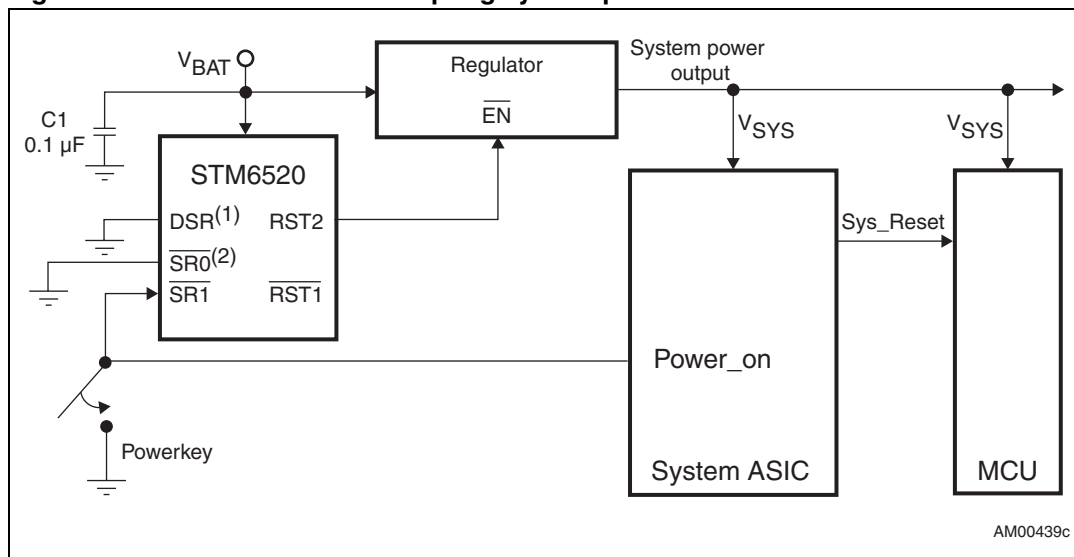
# 4 Typical application diagram

**Figure 4.  $\overline{\text{RST1}}$  output used for microcontroller reset**



1. DSR pin (pin 5) must be tied to  $V_{CC}$  or  $V_{SS}$ .
2. When only one Smart Reset™ input is used, connect the unused one permanently to  $V_{SS}$ .

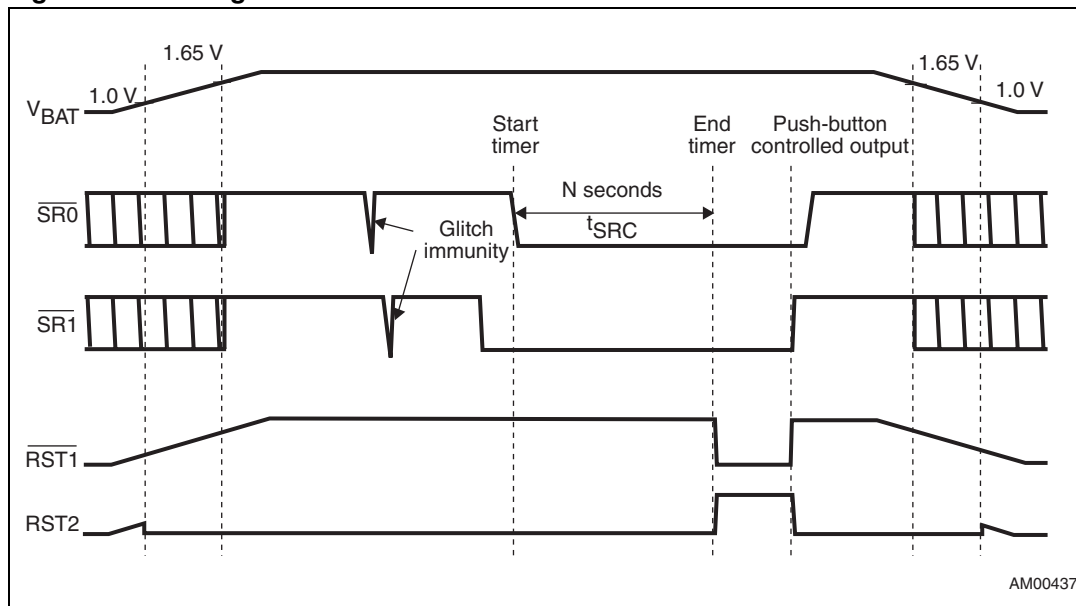
**Figure 5.  $\text{RST2}$  used for interrupting system power**



1. DSR pin (pin 5) must be tied to  $V_{CC}$  or  $V_{SS}$ .
2. When only one Smart Reset™ input is used, connect the unused one permanently to  $V_{SS}$ .

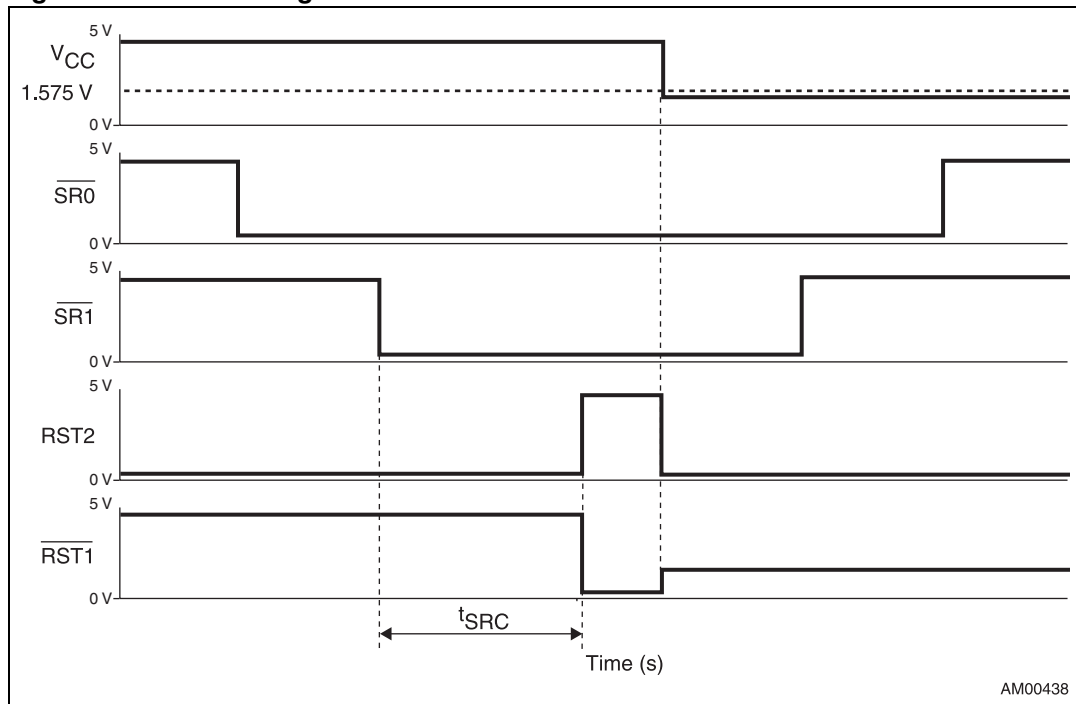


Figure 6. Timing waveforms



AM00437

Figure 7. Undervoltage condition



AM00438

Note: If undervoltage occurs ( $V_{CC}$  drops below 1.575 V typ.) while reset outputs are active, both outputs are released and go inactive.

# 5 Typical operating characteristics

Figure 8. Supply current ( $I_{CC}$ ) vs. temperature

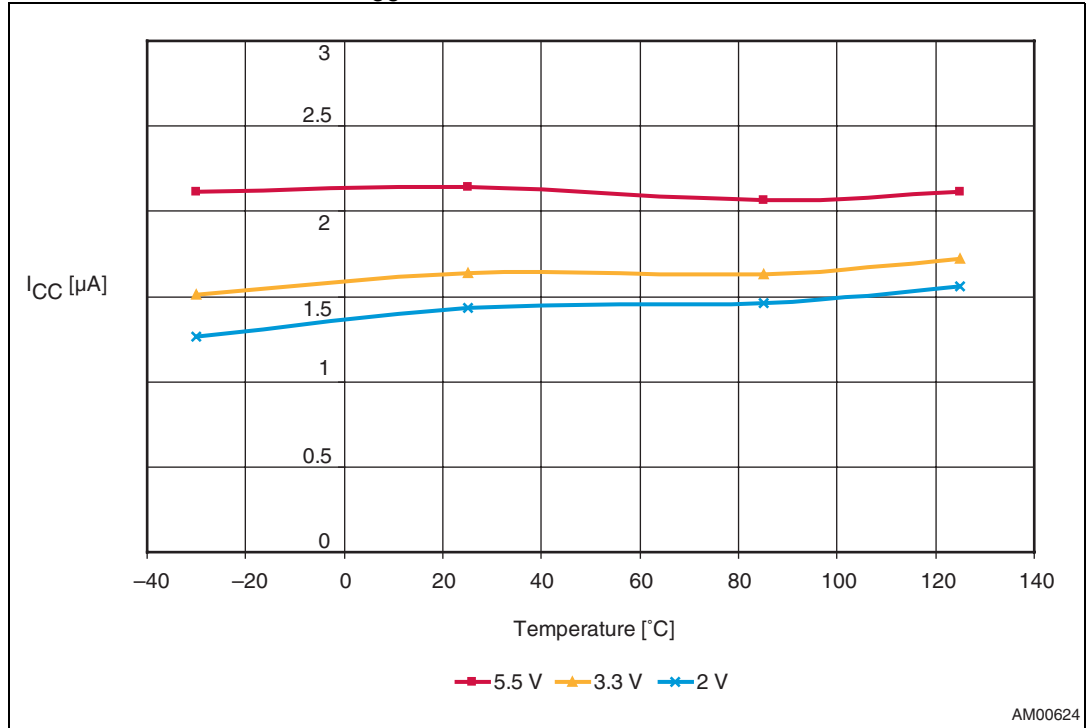
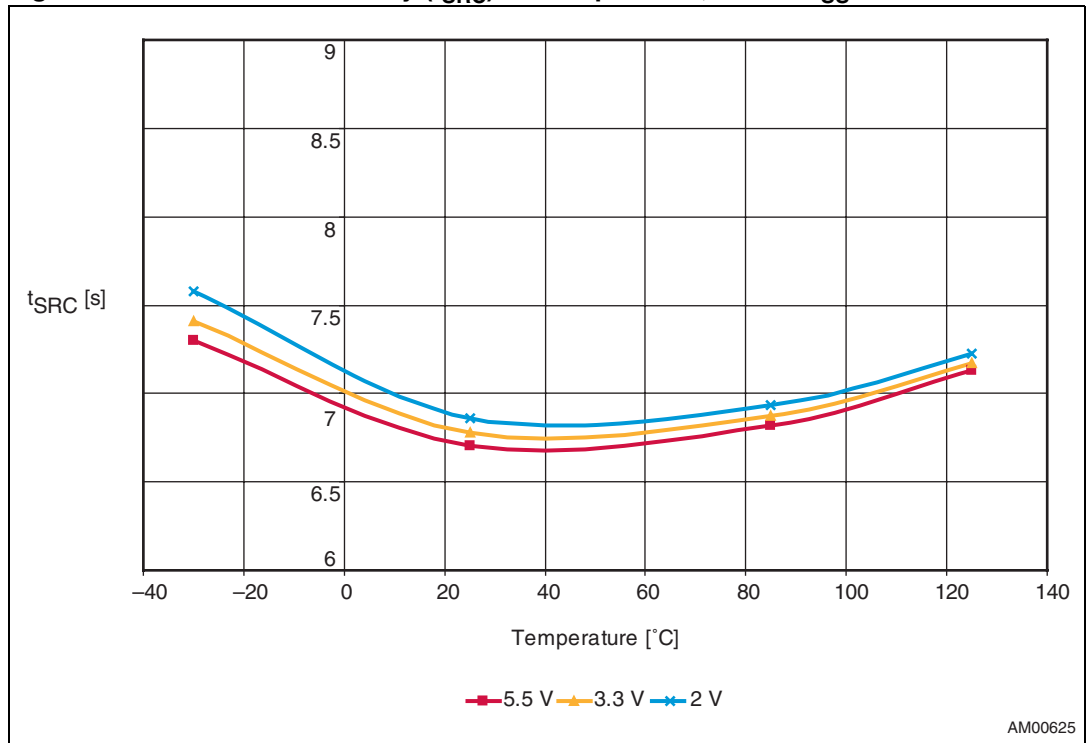


Figure 9. Smart Reset™ delay ( $t_{SRC}$ ) vs. temperature,  $DSR = V_{SS}$



## 6 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$T_{STG}$	Storage temperature ( $V_{CC}$ off)	-55 to +150	°C
$T_{SLD}^{(1)}$	Lead solder temperature for 10 seconds	260	°C
$\theta_{JA}$	Thermal resistance (junction to ambient)	TDFN8 149.0	°C/W
$V_{IO}$	Input or output voltage	-0.3 to 5.5 <sup>(2)</sup>	V
$V_{CC}$	Supply voltage	-0.3 to 7	V
<b>ESD</b>			
$V_{HBM}$	Electrostatic discharge protection, human body model, all pins (JESD22-A114-B level 2)	2	kV
$V_{RCDM}$	Electrostatic discharge protection, charged device model, all pins	1	kV
$V_{MM}$	Electrostatic discharge protection, machine model, all pins (JESD22-A115-A level A)	200	V
	Latch-up ( $V_{CC}$ pin, reset input pins)	EIA/JESD78	

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.
2. For RST2 -0.3 to  $V_{CC}$  +0.3 V only.

## 7 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics table that follow, are derived from tests performed under the Measurement Conditions summarized in [Table 3: Operating and measurement conditions](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 3. Operating and measurement conditions**

Parameter	Value	Unit
V <sub>CC</sub> supply voltage	1.65 to 5.5	V
Ambient operating temperature (T <sub>A</sub> )	-30 to +85	°C
Input rise and fall times	≤5	ns
Input pulse voltages	0.2 to 0.8 V <sub>CC</sub>	V
Input and output timing ref. voltages	0.3 to 0.7 V <sub>CC</sub>	V

**Figure 10. AC testing input/output waveforms**

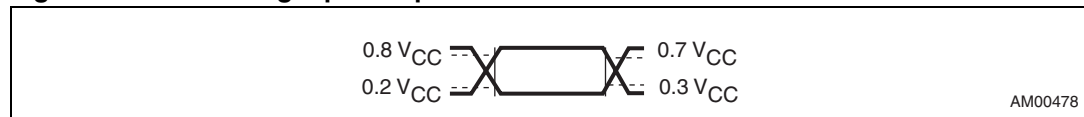


Table 4. DC and AC characteristics

Symbol	Parameter	Test conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units
V <sub>CC</sub>	Supply voltage range	Operating voltage <sup>(3)</sup>	1.65		5.5	V
I <sub>CC</sub>	Supply voltage	V <sub>CC</sub> = 3.0 V, t <sub>SRC</sub> counter is inactive		1.5	2.5	μA
		V <sub>CC</sub> = 5.0 V, t <sub>SRC</sub> counter is inactive		2.0	3.0	μA
		V <sub>CC</sub> = 3.0 V, t <sub>SRC</sub> counter is active		3.5		μA
		V <sub>CC</sub> = 5.0 V, t <sub>SRC</sub> counter is active		4.7		μA
V <sub>OL</sub>	Reset output voltage low	V <sub>CC</sub> ≥ 4.5 V, sinking 3.2 mA			0.3	V
		V <sub>CC</sub> ≥ 3.3 V, sinking 2.5 mA			0.3	V
		V <sub>CC</sub> ≥ 1.65 V, sinking 1 mA			0.3	V
V <sub>OH</sub>	Reset output voltage high, RST2	V <sub>CC</sub> ≥ 4.5 V, I <sub>SOURCE</sub> = 0.8 mA	0.8 V <sub>CC</sub>			V
		V <sub>CC</sub> ≥ 2.7 V, I <sub>SOURCE</sub> = 0.5 mA	0.8 V <sub>CC</sub>			V
		V <sub>CC</sub> ≥ 1.65 V, I <sub>SOURCE</sub> = 0.25 mA	0.8 V <sub>CC</sub>			V
I <sub>LO</sub>	Output leakage current, $\overline{\text{RST1}}$	Open-drain, V <sub>RST1</sub> = 5.5 V	-0.1		0.1	μA
<b>Smart Reset™</b>						
t <sub>SRC</sub>	Smart Reset™ delay	DSR = V <sub>SS</sub>	6	7.5	9	s
		DSR = V <sub>CC</sub>	10	12.5	15	s
V <sub>IL</sub>	$\overline{\text{SR0}}$ , $\overline{\text{SR1}}$ input voltage low		V <sub>SS</sub> - 0.3		0.3	V
V <sub>IH</sub>	$\overline{\text{SR0}}$ , $\overline{\text{SR1}}$ input voltage high		0.85		5.5	V
I <sub>LI</sub>	Input leakage current ( $\overline{\text{SR0}}$ , $\overline{\text{SR1}}$ , DSR pins)		-1		1	μA
	Input glitch immunity <sup>(4)</sup>	Corresponds to the actual t <sub>SRC</sub>		t <sub>SRC</sub>		s

1. Valid for ambient operating temperature: T<sub>A</sub> = -30 to +85 °C; V<sub>CC</sub> = 1.65 to 5.5 V (except where noted).

2. Typical value is at 25 °C and V<sub>CC</sub> = 3.3 V unless otherwise noted.

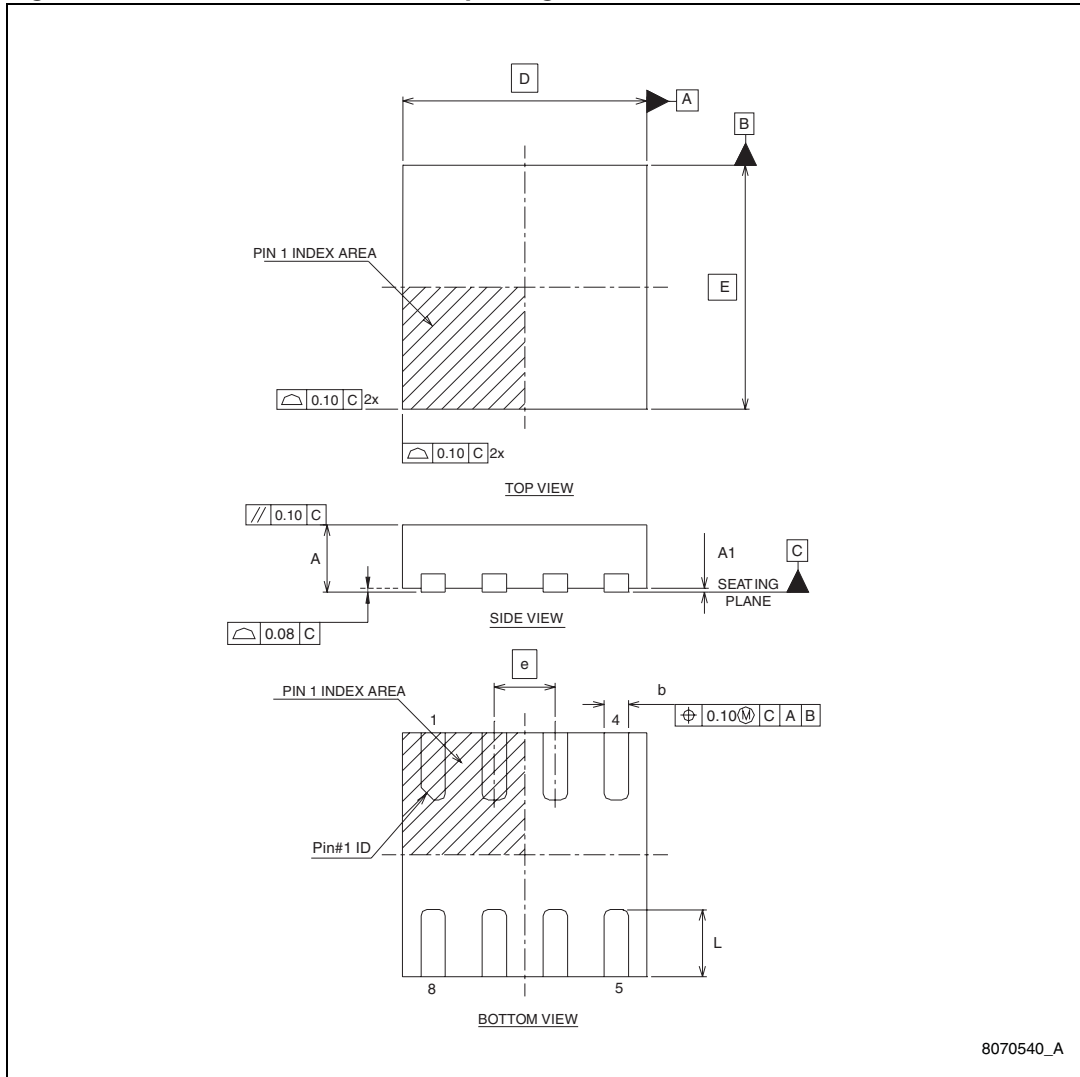
3. Reset outputs are deasserted below 1.575 V typ. and remain deasserted down to V<sub>CC</sub> = 1 V.

4. Input glitch immunity is equal to t<sub>SRC</sub> (when both SR inputs are low), otherwise infinite.

## 8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Figure 11. TDFN - 8-lead, 2 x 2 mm package outline**



**Table 5. TDFN – 8-lead 2 x 2 x 0.75 mm, 0.5 mm package mechanical data**

Symbol	Dimension (mm)			Dimension (inches)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D BSC	1.9	2.00	2.1	0.075	0.079	0.083
E BSC	1.9	2.00	2.1	0.075	0.079	0.083
e		0.50			0.020	
L	0.45	0.55	0.65	0.018	0.022	0.026

## 9 Package footprint

Figure 12. Landing pattern - TDFN – 8-lead 2 x 2 mm without thermal pad

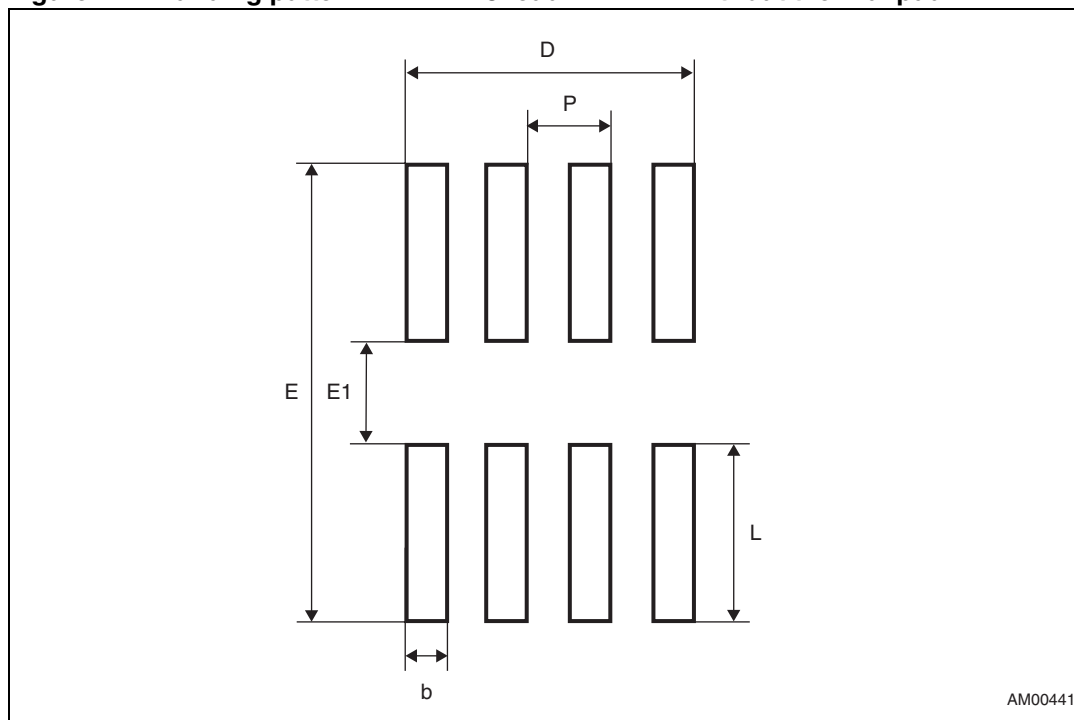


Table 6. Parameter for landing pattern - TDFN – 8-lead 2 x 2 mm package

Parameter	Description	Dimension (mm)		
		Min.	Nom.	Max.
L	Contact length	1.05	—	1.15
b	Contact width	0.25	—	0.30
E	Max. land pattern Y-direction	—	2.85	—
E1	Contact gap spacing	—	0.65	—
D	Max. land pattern X-direction	—	1.75	—
P	Contact pitch	—	0.5	—



# 10 Tape and reel information

Figure 13. Carrier tape

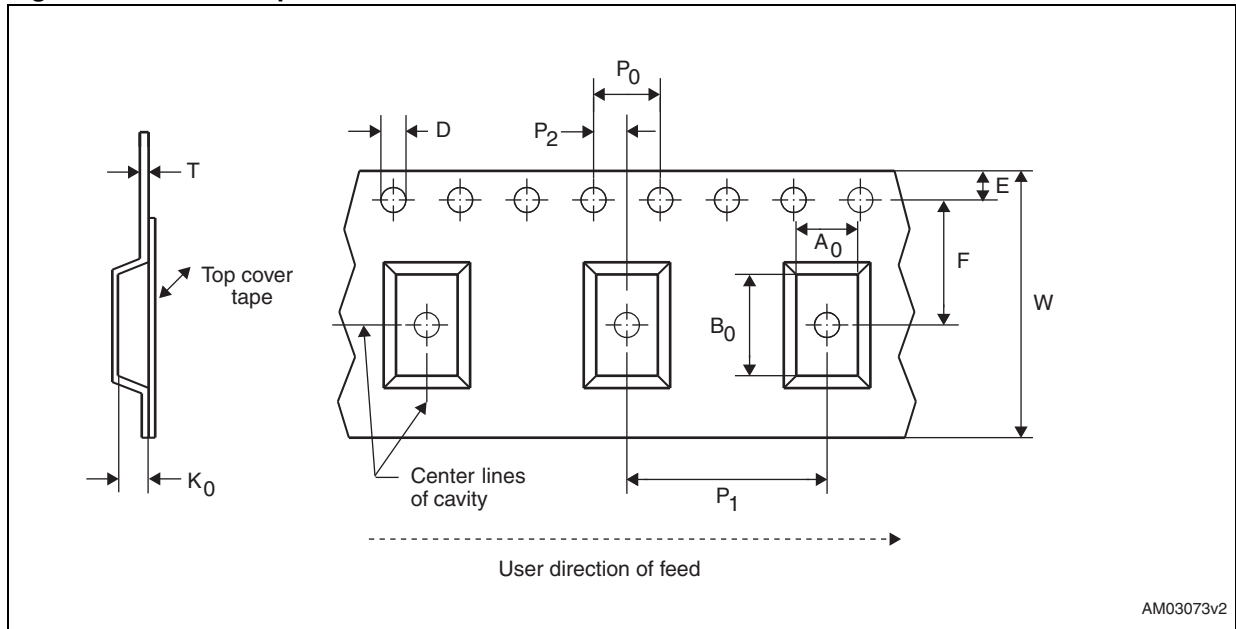


Table 7. Carrier tape dimensions

Package	W	D	E	P <sub>0</sub>	P <sub>2</sub>	F	A <sub>0</sub>	B <sub>0</sub>	K <sub>0</sub>	P <sub>1</sub>	T	Unit	Bulk qty.
TDFN8	8.00 +0.30 -0.10	1.50 +0.10/ -0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	3.50 ±0.05	2.30 ±0.05	2.30 ±0.05	1.00 ±0.05	4.00 ±0.10	0.250 ±0.05	mm	3000

Figure 14. Reel dimensions

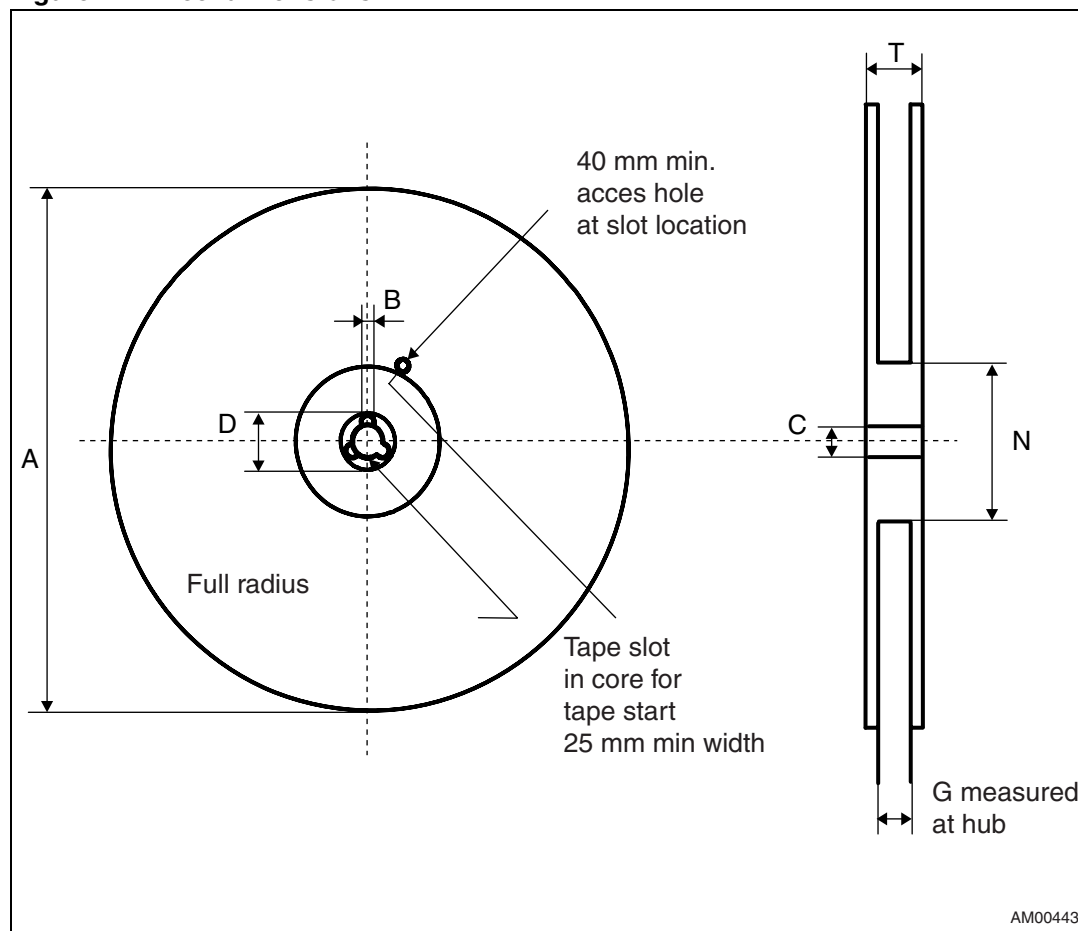
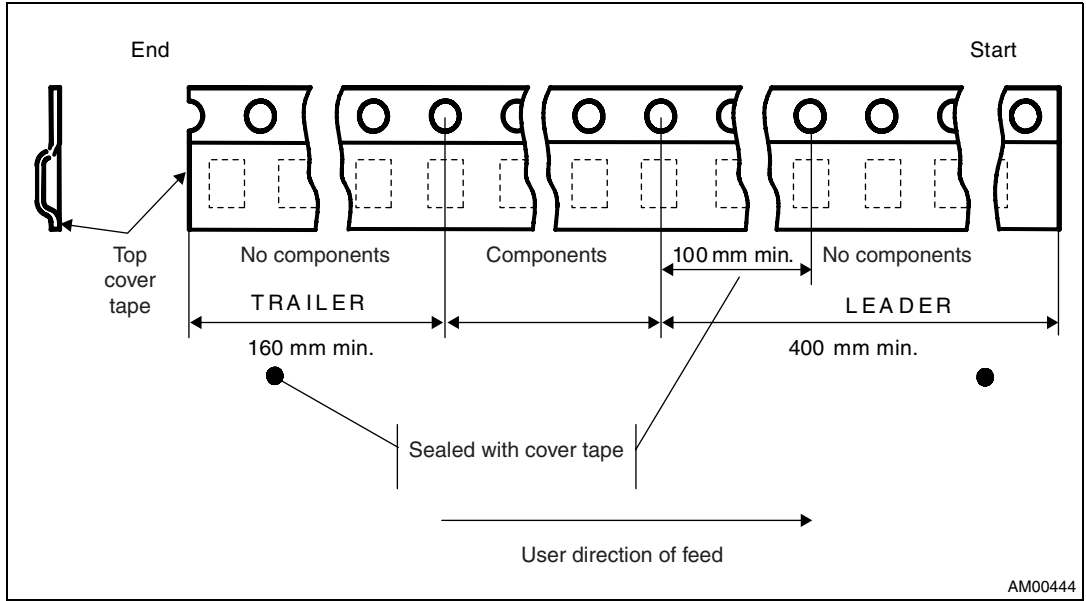


Table 8. Reel dimensions

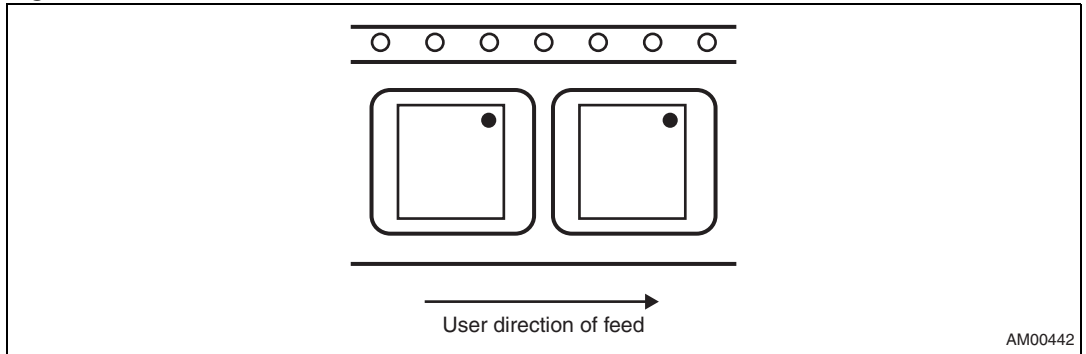
Tape sizes	A max.	B min.	C	D min.	N min.	G	T max.
8 mm	180 (7 inches)	1.50	13.0 +/- 0.20	20.20	60	8.4 +2/-0	14.40

Figure 15. Tape trailer/leader



AM00444

Figure 16. Pin 1 orientation



AM00442

- Note: 1 Drawings are not to scale.  
 2 All dimensions are in mm, unless otherwise noted.

# 11 Ordering information

**Table 9. Ordering information scheme**

Example:	STM6520	A	Q	R	R	DG	9	F
<b>Device type</b>	STM6520							
<b>Reset (<math>V_{CC}</math> monitoring threshold) voltage <math>V_{RST}</math></b>	A = no $V_{CC}$ monitoring feature							
<b>Smart Reset™ setup delay (<math>t_{SRC}</math>)</b>	Q = 7.5 or 12.5 s typ., user-selected (two-state); input comparator on SR0, SR1, no input pull-ups							
<b>Outputs type</b>	R = $\overline{RST1}$ active-low, open-drain, no pull-up; RST2 active-high, push-pull							
<b>Reset pulse timeout period (<math>t_{REC}</math>)</b>	R = push-button controlled (no defined $t_{REC}$ , no power-on reset)							
<b>Package</b>	DG = TDFN8 2 x 2 x 0.75 mm, 0.5 mm pitch							
<b>Temperature range</b>	9 = -30 °C to +85 °C							
<b>Shipping method</b>	F = ECOPACK® package, tape and reel							

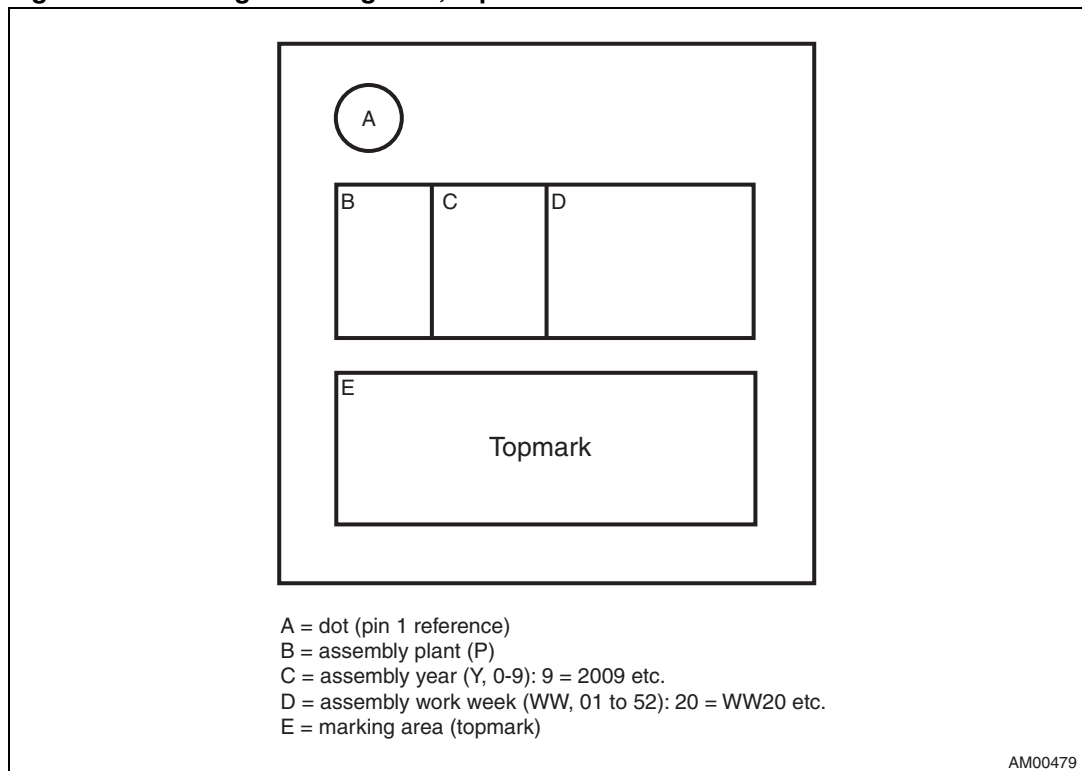
For other options, voltage threshold values etc. or for more information on any aspect of this device, please contact the ST sales office nearest you.

## 12 Package marking information

**Table 10. Package marking**

Part number	Package	Topmark
STM6520AQRRDG9F	TDFN8 2 x 2 x 0.75 mm, 0.5 mm pitch	DRM
STM6520AQRRDG9F	TDFN8 2 x 2 x 0.75 mm, 0.5 mm pitch	ERM

**Figure 17. Package marking area, top view**



## 13 Revision history

**Table 11. Document revision history**

Date	Revision	Changes
08-Jul-2009	1	Initial release.
20-Oct-2009	2	Document reformatted, updated <a href="#">Section 1: Description</a> , <a href="#">Table 1</a> , <a href="#">Figure 4</a> , <a href="#">Figure 5</a> , <a href="#">Table 4</a> , renamed <a href="#">Section 2: Device overview</a> , added <a href="#">Section 5: Typical operating characteristics</a> , updated supply voltage range in <a href="#">Table 4</a> .
20-Jan-2010	3	Updated <a href="#">Section 1: Description</a> , <a href="#">Table 1</a> .
06-May-2010	4	Updated title, <a href="#">Features</a> , <a href="#">Applications</a> , <a href="#">Table 5</a> .
31-May-2010	5	Replaced “smart reset” by “Smart Reset™”, updated <a href="#">Applications</a> , <a href="#">Section 1</a> , <a href="#">Section 3.1</a> , <a href="#">Section 3.5</a> , <a href="#">Figure 4</a> , <a href="#">Figure 5</a> , <a href="#">Table 2</a> , <a href="#">Table 4</a> , <a href="#">Table 6</a> and <a href="#">Table 10</a> .
06-Jan-2011	6	Updated I <sub>CC</sub> - supply voltage in <a href="#">Table 4</a> .

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