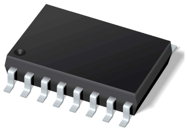


QUAD DIFFERENTIAL PECL RECEIVERS

FEATURES

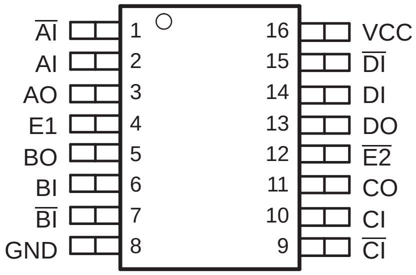
- **Functional Replacement for the Agere BRF1A**
- **Pin Equivalent to General Trade 26LS32**
- **High Input Impedance Approximately 8 kΩ**
- **<2.6-ns Maximum Propagation Delay**
- **TB5R3 Provides 50-mV Hysteresis (Typical)**
- **-1.1-V to 7.1-V Common-Mode Input Voltage Range**
- **Single 5-V ±10% Supply**
- **ESD Protection HBM > 3 kV and CDM > 2 kV**
- **Operating Temperature Range: -40°C to 85°C**
- **Available in Gull-Wing SOIC (JEDEC MS-013, DW) and SOIC (D) Package**

APPLICATIONS

- **Digital Data or Clock Transmission Over Balanced Lines**

PIN ASSIGNMENTS

SOIC PACKAGE
(TOP VIEW)



DESCRIPTION

These quad differential receivers accept digital data over balanced transmission lines. They translate differential input logic levels to TTL output logic levels.

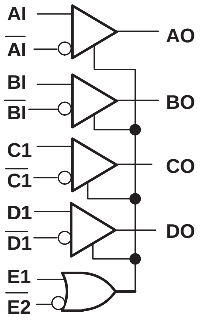
The TB5R3 is a pin- and function-compatible replacement for the Agere systems BRF1A; it includes 3-kV HBM and 2-kV CDM ESD protection.

The power-down loading characteristics of the receiver input circuit are approximately 8 kΩ relative to the power supplies; hence they do not load the transmission line when the circuit is powered down.

The packaging for this differential line receiver is a 16-pin gull wing SOIC (DW) or a 16 pin SOIC (D).

The enable inputs of this device include internal pull-up resistors of approximately 40 kΩ that are connected to V_{CC} to ensure a logical high level input if the inputs are open circuited.

FUNCTIONAL BLOCK DIAGRAM



Enable Truth Table

E1	$\overline{E2}$	OUTPUT CONDITION
0	0	Active
1	0	Active
0	1	Disabled
1	1	Active

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER[1]	PART MARKING	PACKAGE[2]	LEAD FINISH	STATUS
TB5R3DW	TB5R3	Gull-Wing SOIC	NiPdAu	Production
TB5R3D	TB5R3	SOIC	NiPdAu	Production

(1) Add the R suffix for tape and reel carrier (i.e., TB5R3DR)
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING $T_A \leq 25°C$	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT WITH NO AIR FLOW	DERATING FACTOR[1] $T_A \geq 25°C$	POWER RATING $T_A = 85°C$
DW	Low-K[2]	831 mW	120.3°C/W	8.3 mW/°C	332 mW
	High-K[3]	1240 mW	80.8°C/W	12.4 mW/°C	494 mW
D	Low-K[2]	763 mW	131.1°C/W	7.6 mW/°C	305 mW
	High-K[3]	1190 mW	84.1°C/W	11.9 mW/°C	475 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted with no air flow.
(2) In accordance with the low-K thermal metric definitions of EIA/JESD51-3.
(3) In accordance with the high-K thermal metric definitions of EIA/JESD51-7.

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to-Board Thermal Resistance	DW	53.7	°C/W
		D	47.5	
θ_{JC}	Junction-to-Case Thermal Resistance	DW	47.1	°C/W
		D	44.2	

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

			UNIT
Supply voltage, V_{CC}			0 V to 6 V
Magnitude of differential bus (input) voltage, $\|V_{AI} - V_{\overline{AI}}\|$, $\|V_{BI} - V_{\overline{BI}}\|$, $\|V_{CI} - V_{\overline{CI}}\|$, $\|V_{DI} - V_{\overline{DI}}\|$			8.4 V
ESD	Human Body Model[2]	All pins	±3.5 kV
	Charged-Device Model[3]	All pins	±2 kV
Continuous power dissipation			See Dissipation Rating Table
Storage temperature, T_{stg}			-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(3) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Bus pin input voltage, V_{AI}, $V_{\overline{AI}}$, $V_{BI}V_{\overline{BI}}$, V_{CI} , or $V_{\overline{CI}}$, V_{DI}, $V_{\overline{DI}}$	-1.2(1)		7.2	V
Magnitude of differential input voltage, $\lvert V_{AI} - V_{\overline{AI}}\rvert$, $\lvert V_{BI} - V_{\overline{BI}}\rvert$, $\lvert V_{CI} - V_{\overline{CI}}\rvert$, $\lvert V_{DI} - V_{\overline{DI}}\rvert$	0.1		6	V
Low-level enable input voltage(2), V_{IL} (V_{CC} = 5.5 V)			0.8	V
High-level enable input voltage(2), V_{IH} (V_{CC} = 5.5 V)	2			V
Operating free-air temperature, T_A	-40		85	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet, unless otherwise noted.
(2) The input levels and difference voltage provide no noise immunity and should be tested only in a static, noise-free environment.

DEVICE ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current(1)	Outputs disabled			50	mA
		Outputs enabled			48	mA

(1) Current is dc power draw as measured through GND pin and does not include power delivered to load.

RECEIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Output low voltage	V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.4	V
V_{OH}	Output high voltage	V_{CC} = 4.5 V,	I_{OH} = -400 µA	2.4			V
V_{IK}	Enable input clamp voltage	V_{CC} = 4.5 V,	I_I = -5 mA			-1(1)	V
V_{TH+}	Positive-going differential input threshold voltage(2), ($V_{xI} - V_{\overline{xI}}$)	x = A, B, C, or D				100	mV
V_{TH-}	Negative-going differential input threshold voltage(2), ($V_{xI} - V_{\overline{xI}}$)	x = A, B, C, or D				-100(1)	mV
V_{HYST}	Differential input threshold voltage hysteresis, ($V_{TH+} - V_{TH–}$)				50		mV
I_{OZL}	Output off-state current, (High-Z)	V_{CC} = 5.5 V	V_O = 0.4 V			-20(1)	µA
I_{OZH}			V_O = 2.4 V			20	µA
I_{OS}	Output short circuit current	V_{CC} = 5.5 V				-400(1)	mA
I_{IL}	Enable input low current	V_{CC} = 5.5 V,	V_{IN} = 0.4 V			-400(1)	µA
I_{IH}	Enable input high current	V_{CC} = 5.5 V	V_{IN} = 2.7 V			20	µA
	Enable input reverse current		V_{IN} = 5.5 V			100	µA
I_{IL}	Differential input low current	V_{CC} = 5.5V,	V_{IN} = -1.2 V			-2(1)	mA
I_{IH}	Differential input high current	V_{CC}= 5.5V,	V_{IN} = 7.2 V			1	mA
R_O	Small-signal output resistance	Output High			50		Ω
		Output Low			25		

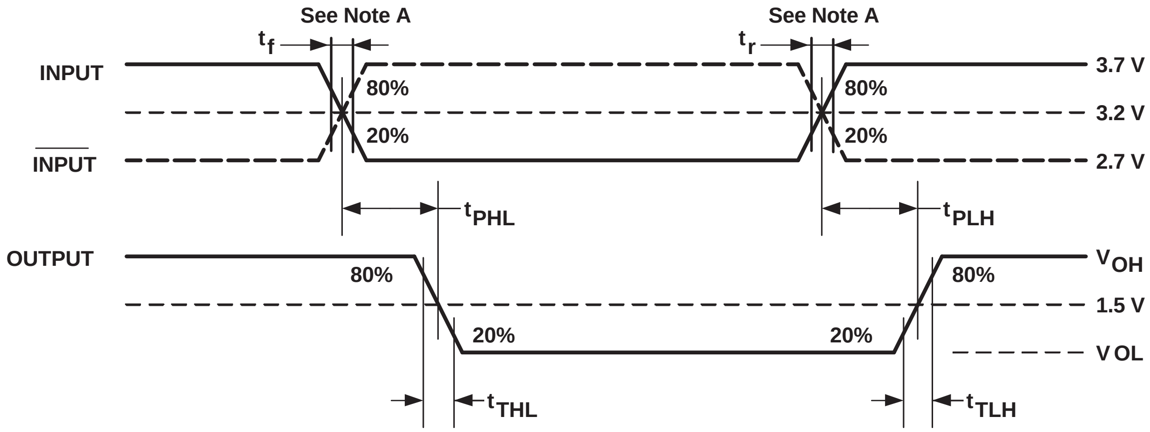
(1) This parameter is listed using a magnitude and polarity/direction convention, rather than an algebraic convention, to match the original Agere data sheet.
(2) The input levels and difference voltage provide no noise immunity and should be tested only in a static, noise-free environment.

SWITCHING CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

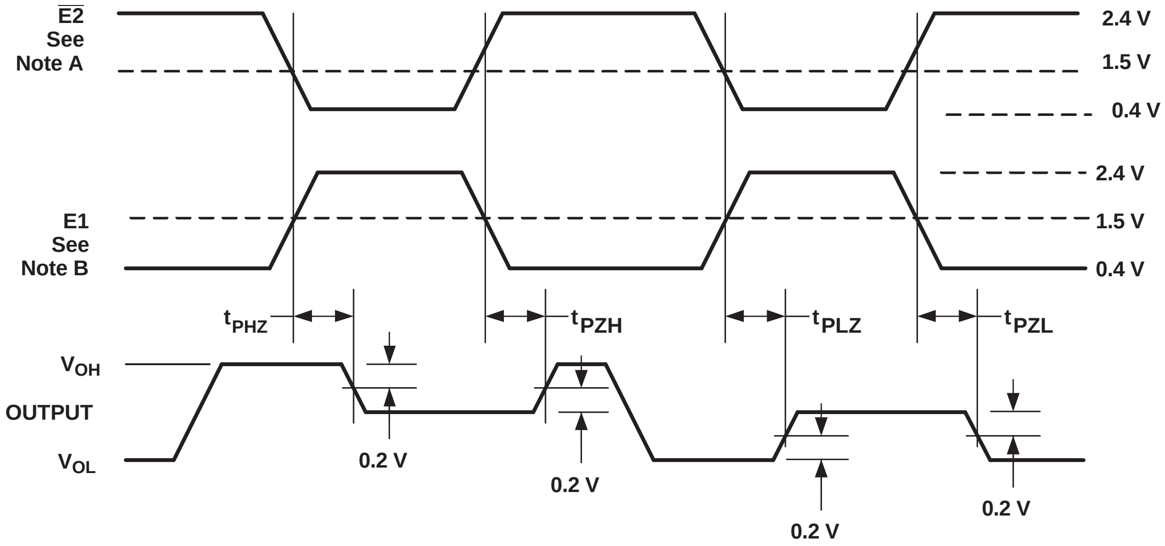
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 0 pF[1], See Figure 2 and Figure 4		1.64	<2.6	ns
t_{PHL}	Propagation delay time, high-to-low-level output			1.57	<2.6	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, See Figure 2 and Figure 4[2]		2.2	3.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			2.1	3.5	
t_{PHZ}	Output disable time, high-level-to-high-impedance output[3]	C_L = 5 pF, See Figure 3 and Figure 5		7.7	12	ns
t_{PLZ}	Output disable time, low-level-to-high-impedance output[3]			5.2	12	ns
t_{skew1}	Pulse-width distortion, $\|t_{PHL}$ - $t_{PLH}\|$	C_L = 10 pF, See Figure 2 and Figure 4			0.7	ns
		C_L = 150 pF, See Figure 2 and Figure 4			4	ns
$\Delta t_{skew1p-p}$	Part-to-part output waveform skew	C_L = 10 pF, T_A = 75°C, See Figure 2 and Figure 4		0.8	1.4	ns
		C_L = 10 pF, See Figure 2 and Figure 4			1.5	ns
Δt_{skew}	Same part output waveform skew	C_L = 10 pF, See Figure 2 and Figure 4			0.3	ns
t_{PZH}	Output enable time, high-impedance-to-high-level output[3]	C_L = 10 pF, See Figure 3 and Figure 4		6.9	12	ns
t_{PZL}	Output enable time, high-impedance-to-low-level output[3]			6.3	12	ns
t_{TLH}	Rise time (20%-80%)	C_L = 10 pF, See Figure 2 and Figure 4			1	ns
t_{THL}	Fall time (80%-20%)				1	ns

(1) The propagation delay values with a 0 pF load are based on design and simulation.
(2) t_r/t_f: 3 ns (20% - 80%)
(3) See Table 1.



A. t_r/t_f: 3 ns (20% - 80%)

Figure 1. Receiver Propagation Delay Times

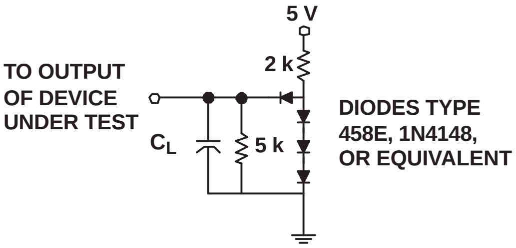


A. $\overline{E2}$ = 1 while E1 changes states.

B. E1 = 0 while $\overline{E2}$ changes states.

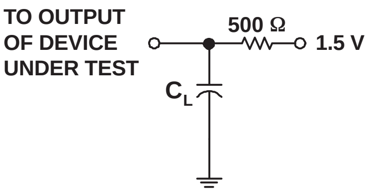
Figure 2. Receiver Enable and Disable Timing

Parametric values specified under the Electrical Characteristics and Timing Characteristics sections for the data transmission driver devices are measured with the following output load circuits.



C_L includes test-fixture and probe capacitance.

Figure 3. Receiver Propagation Delay Time and Enable Time (t_{PZH}, t_{PZL}) Test Circuit

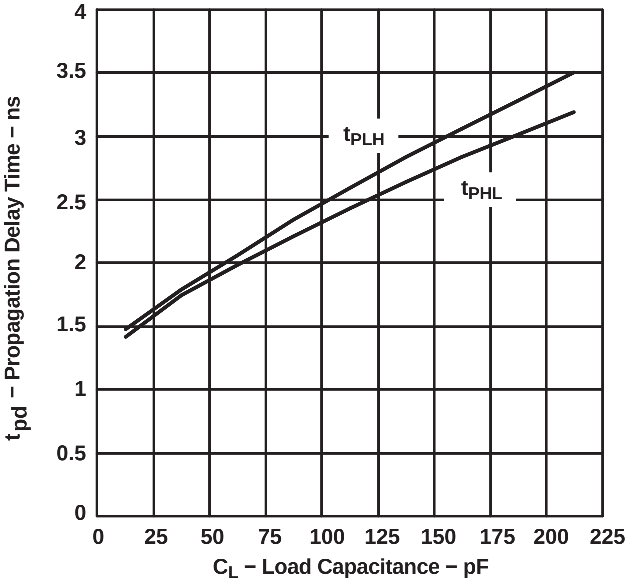


C_L includes test-fixture and probe capacitance.

Figure 4. Receiver Disable Time (t_{PHZ}, t_{PLZ}) Test Circuit

TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY vs LOAD CAPACITANCE



NOTE: This graph is included as an aid to the system designers. Total circuit delay varies with load capacitance. The total delay is the sum of the delay due to external capacitance and the intrinsic delay of the device. Intrinsic delay is listed in the table above as the 0 pF load condition. The incremental increase in delay between the 0 pF load condition and the actual total load capacitance represents the extrinsic, or external delay contributed by the load.

Figure 5.

TYPICAL CHARACTERISTICS (continued)

LOW-TO-HIGH PROPAGATION DELAY
vs
JUNCTION TEMPERATURE

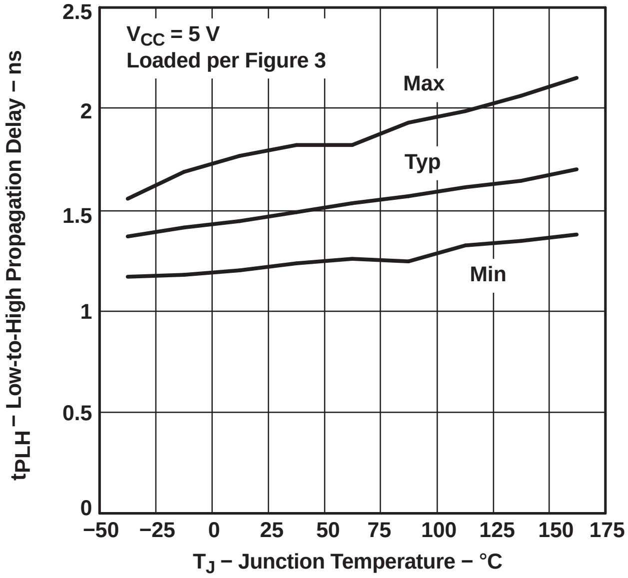


Figure 6.

HIGH-TO-LOW PROPAGATION DELAY
vs
JUNCTION TEMPERATURE

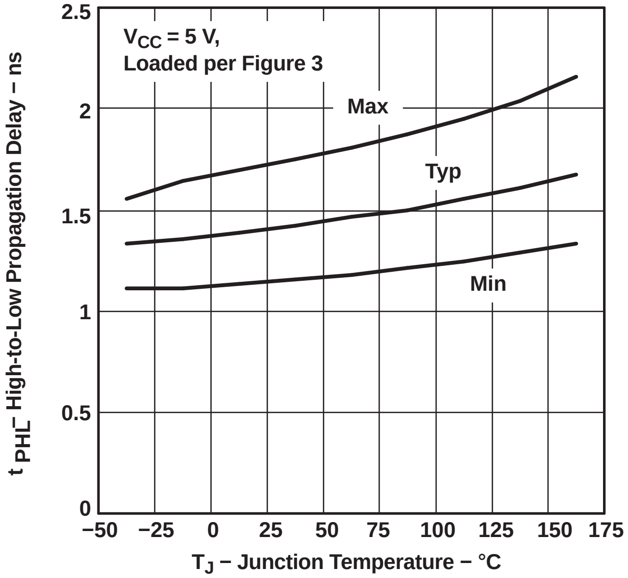


Figure 7.

MINIMUM V_{OH} AND MAXIMUM V_{OL}
vs
JUNCTION TEMPERATURE

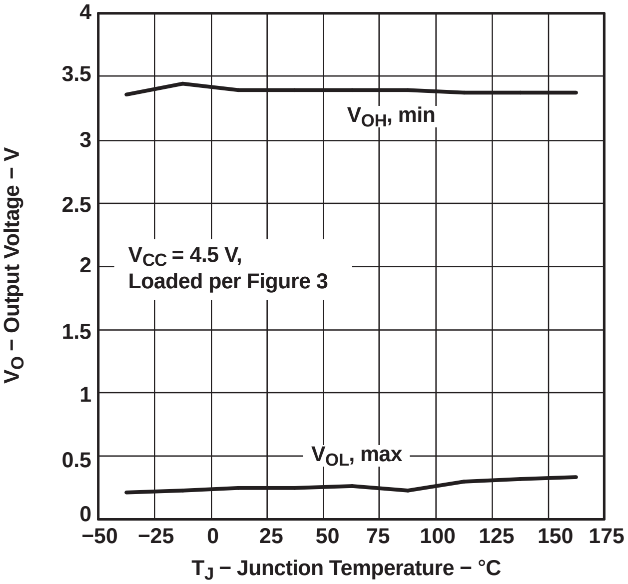


Figure 8.

TYPICAL AND MAXIMUM I_{CC}
vs
JUNCTION TEMPERATURE

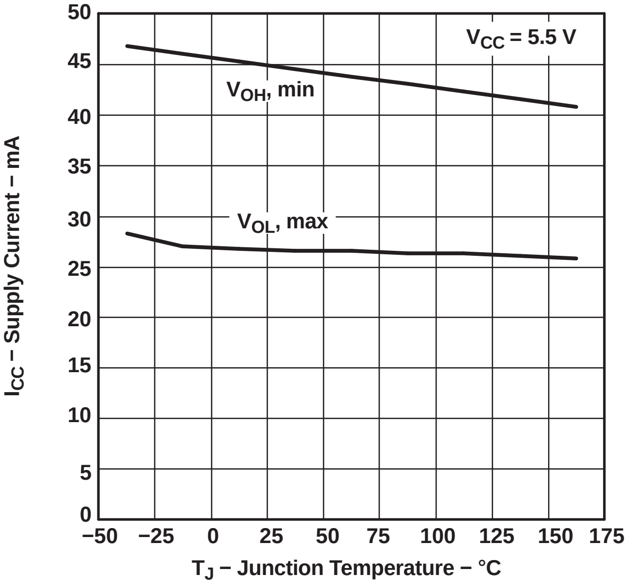


Figure 9.

APPLICATION INFORMATION

Power Dissipation

The power dissipation rating, often listed as the package dissipation rating, is a function of the ambient temperature, T_A, and the airflow around the device. This rating correlates with the device's maximum junction temperature, sometimes listed in the absolute maximum ratings tables. The maximum junction temperature accounts for the processes and materials used to fabricate and package the device, in addition to the desired life expectancy.

There are two common approaches to estimating the internal die junction temperature, T_J. In both of these methods, the device internal power dissipation P_D needs to be calculated This is done by totaling the supply power(s) to arrive at the system power dissipation:

$$\sum \left(V_{Sn} \times I_{Sn}\right) \tag{1}$$

and then subtracting the total power dissipation of the external load(s):

$$\sum \left(V_{Ln} \times I_{Ln}\right) \tag{2}$$

The first T_J calculation uses the power dissipation and ambient temperature, along with one parameter: θ_{JA}, the junction-to-ambient thermal resistance, in degrees Celsius per watt.

The product of P_D and θ_{JA} is the junction temperature rise above the ambient temperature. Therefore:

$$T_J = T_A + \left(P_D \times \theta_{JA}\right) \tag{3}$$

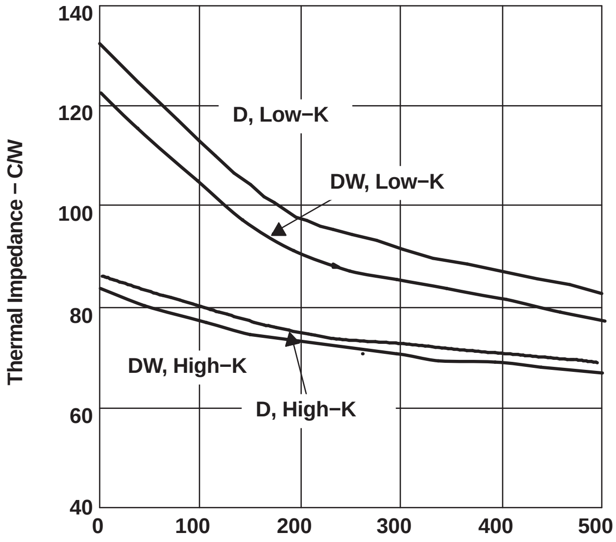


Figure 10. Thermal Impedance vs Air Flow

Note that θ_{JA} is highly dependent on the PCB on which the device is mounted and on the airflow over the device and PCB. JEDEC/EIA has defined standardized test conditions for measuring θ_{JA}. Two commonly used conditions are the low-K and the high-K boards, covered by EIA/JESD51-3 and EIA/JESD51-7 respectively. Figure 10 shows the low-K and high-K values of θ_{JA} versus air flow for this device and its package options.

The standardized θ_{JA} values may not accurately represent the conditions under which the device is used. This can be due to adjacent devices acting as heat sources or heat sinks, to nonuniform airflow, or to the system PCB having significantly different thermal characteristics than the standardized test PCBs. The second method of system thermal analysis is more accurate. This calculation uses the power dissipation and ambient temperature, along with two device and two system-level parameters:

- θ_{JC}, the junction-to-case thermal resistance, in degrees Celsius per watt
- θ_{JB}, the junction-to-board thermal resistance, in degrees Celsius per watt
- θ_{CA}, the case-to-ambient thermal resistance, in degrees Celsius per watt
- θ_{BA}, the board-to-ambient thermal resistance, in degrees Celsius per watt.

In this analysis, there are two parallel paths, one through the case (package) to the ambient, and another through the device to the PCB to the ambient. The system-level junction-to-ambient thermal impedance, $\theta_{JA(S)}$, is the equivalent parallel impedance of the two parallel paths:

$$T_J = T_A + \left(P_D \times \theta_{JA(S)}\right) \tag{4}$$

where

$$\theta_{JA(S)} = \frac{\left[\left(\theta_{JC} + \theta_{CA}\right) \times \left(\theta_{JB} + \theta_{BA}\right)\right]}{\left(\theta_{JC} + \theta_{CA} + \theta_{JB} + \theta_{BA}\right)} \tag{5}$$

The device parameters θ_{JC} and θ_{JB} account for the internal structure of the device. The system-level parameters θ_{CA} and θ_{BA} take into account details of the PCB construction, adjacent electrical and mechanical components, and the environmental conditions including airflow. Finite element (FE), finite difference (FD), or computational fluid dynamics (CFD) programs can determine θ_{CA} and θ_{BA}. Details on using these programs are beyond the scope of this data sheet, but are available from the software manufacturers.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TB5R3DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TB5R3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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GENERIC PACKAGE VIEW

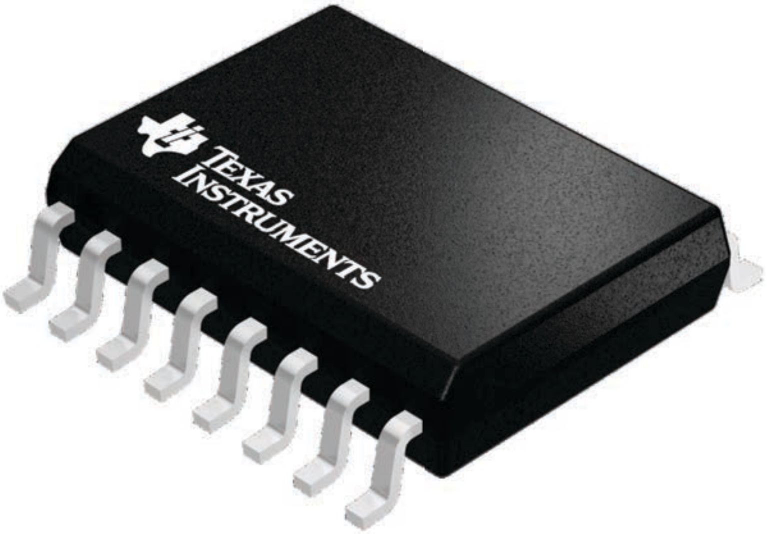
DW 16

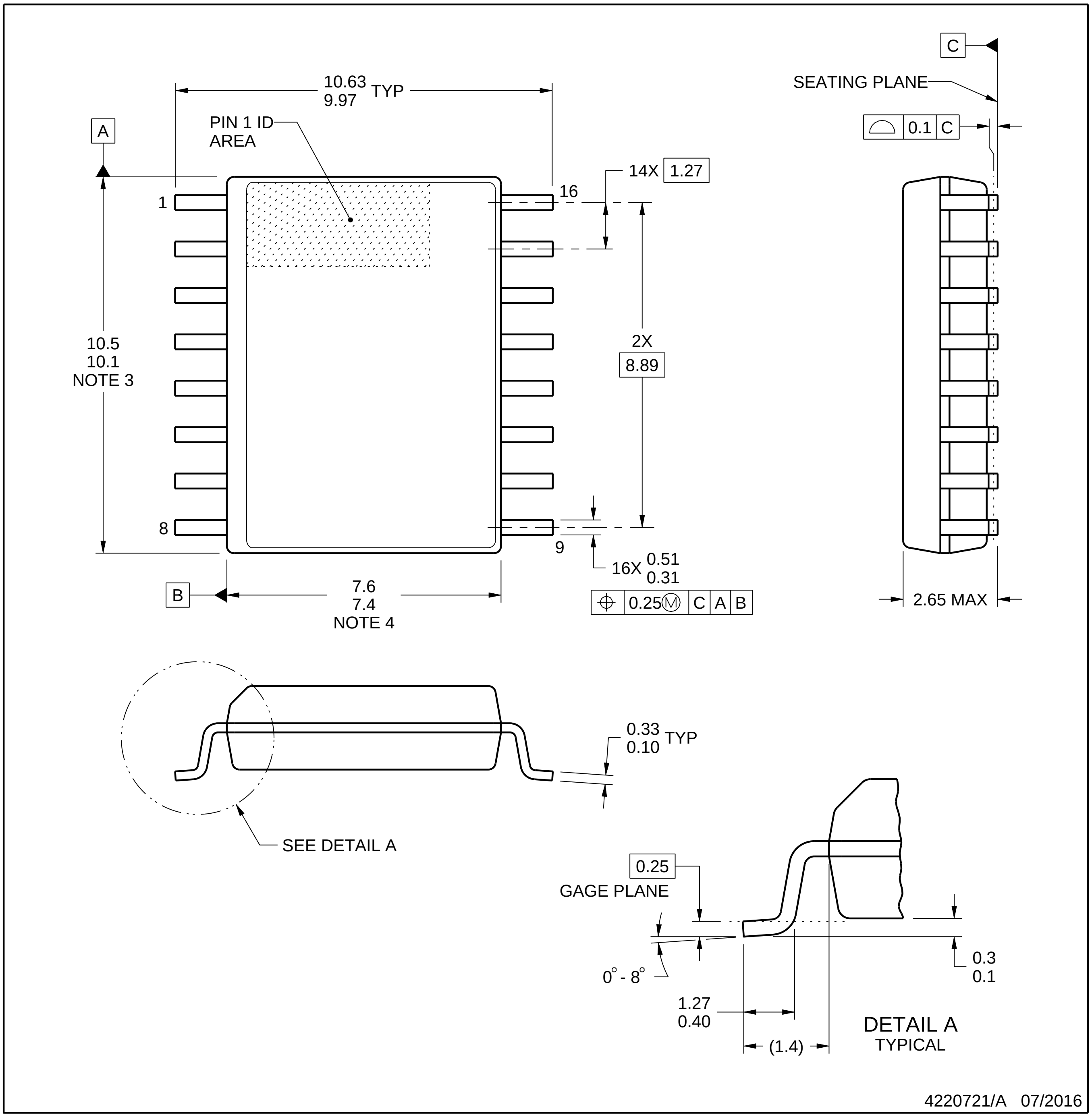
SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

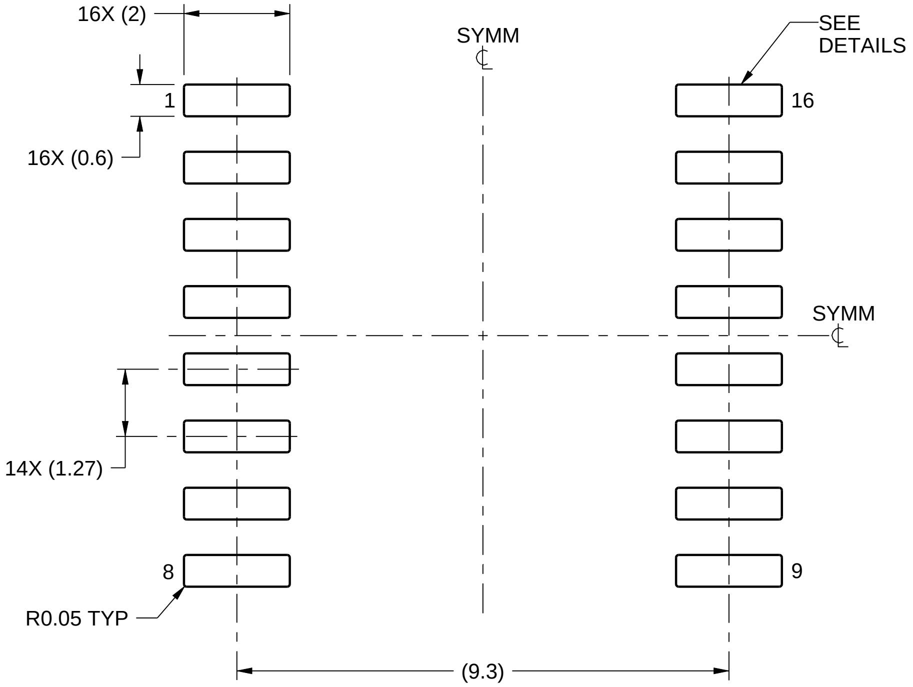
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



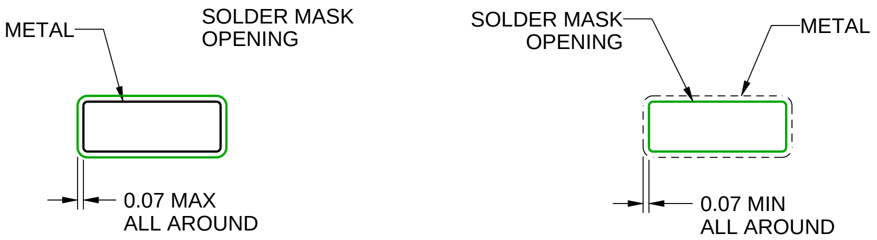


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X



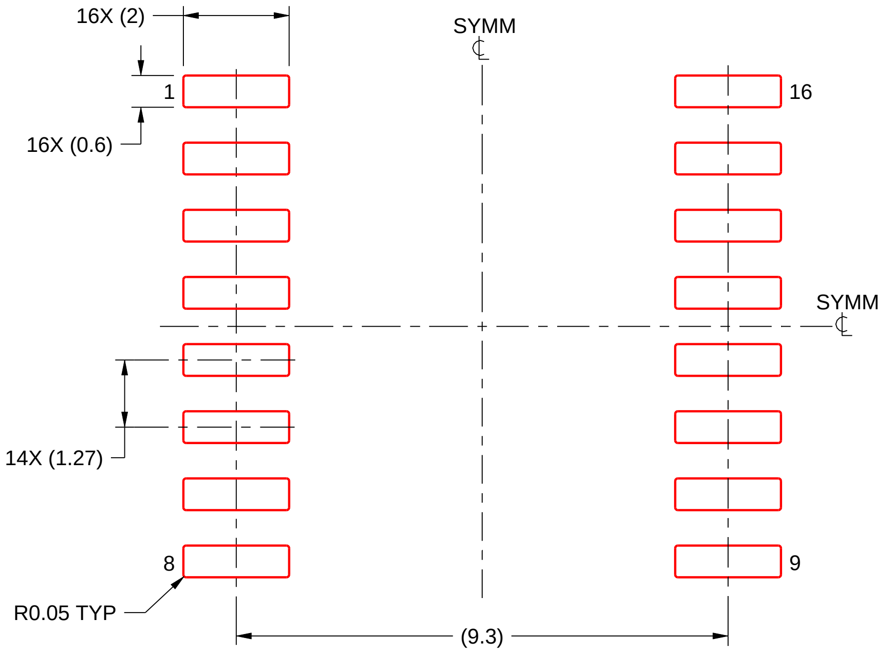
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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