ISL24211

Programmable V_{COM} Calibrator with EEPROM and Output Buffer

FN7585
Rev 0.00
February 23, 2011

The ISL24211 is an 8-bit programmable current sink that can be used in conjunction with an external voltage divider to generate a voltage source (V_{COM}) positioned between the analog supply voltage and ground. The current sink's full-scale range is controlled by an external resistor, R_{SET}. With the appropriate choice of external resistors R_1 and R_2, the V_{COM} voltage range can be controlled between any arbitrary voltage range. The ISL24211 has an 8-bit data register and 8-bit EEPROM for storing both a volatile and a permanent value for its output, with an I^2C interface to read and write to the register and EEPROM. After the part is programmed, the I^2C interface is no longer needed; on power-up the EEPROM contents are automatically transferred to the data register, and the pre-programmed output voltage appears on the VCOM_OUT pin.

The ISL24211 also features an integrated, wide-bandwidth, high output drive buffer amplifier that can directly drive the V_{COM} input of an LCD panel.

The ISL24211 is available in an 10 Ld 3mm x 3mm TDFN package. This package has a maximum height of 0.8mm for very low profile designs. The ambient operating temperature range is
-40°C to +85°C.

Features

- 8-bit, 256-Step, Adjustable Sink Current Output
- 60MHz V_{COM} Buffer/Amplifier
- 4.5V to 19.0V Analog Supply Range for Normal Operation (10.8V Minimum Analog Supply Voltage for Programming)
- 2.25V to 3.6V Logic Supply Voltage Operating Range
- 400kHz, I^2C Interface
- On-Chip 8-Bit EEPROM
- Guaranteed Monotonic Over-Temperature
- Compatible with applications using the 7-bit ISL45041
- Pb-free (RoHS-compliant)
- Ultra-Thin 10 Ld TDFN (3 x 3 x 0.8mm max)

Applications

- LCD Panel V_{COM} Generator
- Electrophoretic Display V_{COM} Generator

Related Literature

- AN1627 "ISL24211IRTZ-EVALZ Evaluation Board User Guide"

Typical Application

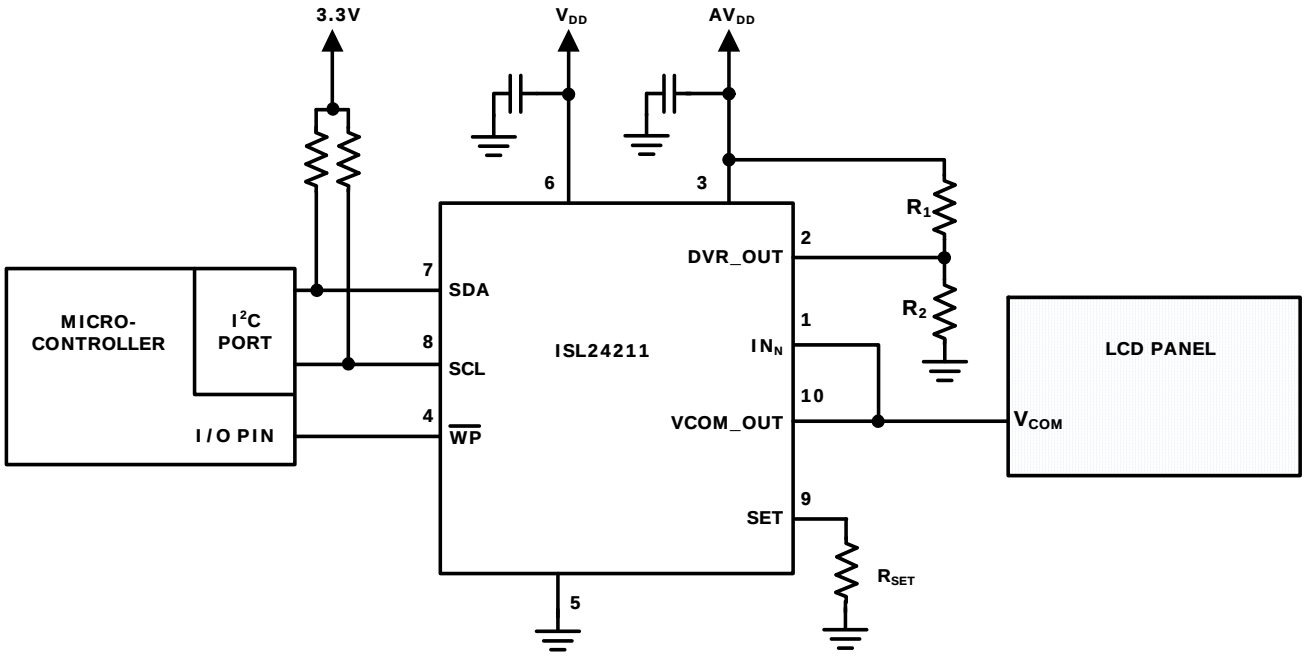


FIGURE 1. TYPICAL ISL24211 APPLICATION

Block Diagram

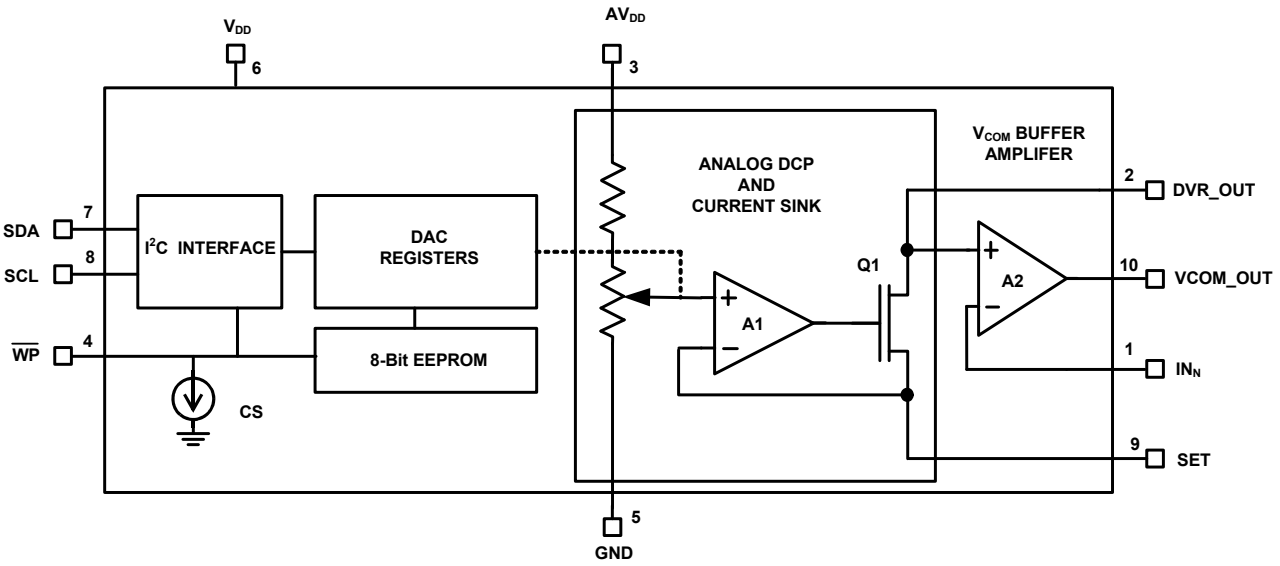
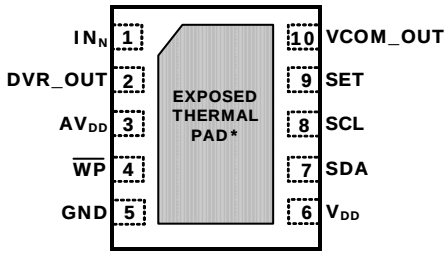


FIGURE 2. BLOCK DIAGRAM OF THE ISL24211

Pin Configuration

ISL24211
(10 LD TDFN)
TOP VIEW



(*THERMAL PAD CONNECTS TO GND)

Pin Descriptions

PIN NAME	PIN NUMBER	FUNCTION
IN_N	1	Negative (inverting) input of the V_{COM} buffer op amp. This pin is used to provide feedback from the end point of the V_{COM} trace.
DVR_OUT	2	Adjustable Sink Current Output Pin. The current sunk into the DVR_OUT pin is equal to the DAC setting times the maximum adjustable sink current divided by 256. See the “SET” pin function description below (pin 9) for the maximum adjustable sink current setting. Also tied to the non-inverting input of buffer amp.
AV_{DD}	3	Analog Power Supply Input. Bypass to GND with 0.1µF capacitor.
$\overline{WP}$	4	EEPROM Write Protect. Active Low. 0 = Programming disabled; 1 = Programming allowed.
GND	5	Ground connection.
V_{DD}	6	Digital power supply input. Bypass to GND with 0.1µF capacitor.
SDA	7	I^2C Serial Data Input
SCL	8	I^2C Clock Input
SET	9	Maximum Sink Current Adjustment Point. Connect a resistor from SET to GND to set the maximum adjustable sink current of the DVR_OUT pin. The maximum adjustable sink current is equal to (AV_{DD}/20) divided by R_{SET}.
VCOM_OUT	10	Output of the buffer amplifier
PAD	-	Thermal pad should be connected to system ground plane to optimize thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	INTERFACE	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL24211IRTZ	211Z	I^2C	-40 to +85	10 Ld 3x3 TDFN	L10.3x3A
ISL24211IRTZ-EVALZ	Evaluation Board				

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page ISL24211. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

Supply Voltage
- AV_{DD} to GND 20V
- V_{DD} to GND 4V

Input Voltage with respect to Ground
- SET, IN_N 4V
- SCL, SDA and $\overline{WP}$ . . . . . V_{DD} + 0.3V

Output Voltage with respect to Ground
- DVR_OUT, VCOM_OUT . . . . . AV_{DD}

Continuous Output Current
- DVR_OUT 5mA
- VCOM_OUT . . . . . ±100mA

ESD Ratings
- Human Body Model (Tested per JESD22-A114) 7kV
- Machine Model (Tested per JESD22-A115) 300V
- Charged Device Model (Tested per JESD22-C101) 2kV

Latch Up (Tested per JESD 78, Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld TDFN Package (Notes 4, 5)	53	11

Moisture Sensitivity (see Technical Brief TB363)
- All Packages . . . . . Level 1

Maximum Die Temperature . . . . . +150°C

Storage Temperature . . . . . -65°C to +150°C

Pb-free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Operating Range
- AV_{DD} . . . . . 4.5V to 19V
- V_{DD} . . . . . 2.25V to 3.6V

Ambient Operating Temperature . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Test Conditions: V_{DD} = 3.3V, AV_{DD} = 18V, R_{SET} = 5kΩ, R_1 = 10kΩ, R_2 = 10kΩ, (See Figure 5), V_{COM_OUT} pin connected to IN_N, unless otherwise specified. Typicals are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
DC CHARACTERISTICS						
V_{DD}	V_{DD} Supply Range - Operating		**2.25**		**3.6**	V
AV_{DD}	AV_{DD} Supply Range Supporting EEPROM Programming		**10.8**		**19**	V
AV_{DD}	AV_{DD} Supply Range for Wide-Supply Operation (not supporting EEPROM Programming)		**4.5**		**19**	V
I_{DD}	V_{DD} Supply Current	$\overline{WP}$ = SCL = SDA = V_{DD}		95	**300**	µA
I_{AVDD}	AV_{DD} Supply Current	$\overline{WP}$ = SCL = SDA = V_{DD}		3.8	**6.5**	mA
DVR_OUT CHARACTERISTICS						
ZSE_{SET}	SET Zero-Scale Error				**±3**	LSB
FSE_{SET}	SET Full-Scale Error				**±8**	LSB
TCV_{SET}	SET Voltage Drift			7		µV/°C
V_{DVR_OUT}	DVR_OUT Voltage Range	I_{DVR_OUT} < 0.5mA	**V_{SET} + 0.4**		**AV_{DD}**	V
I_{DVR_OUT}	Maximum DVR_OUT Sink Current			4		mA
INL	Integral Non-Linearity				**±2**	LSB
DNL	Differential Non-Linearity				**±1**	LSB
OUTPUT AMPLIFIER CHARACTERISTICS						
V_{OS}	Input Offset Voltage			±2	**±15**	mV
TCV_{OS}	Input Offset Voltage Drift			-6.3		µV/°C
I_B	Input Bias Current			0.001	**±1**	µA
CMRR	Common-Mode Rejection Ratio		**55**	75		dB
PSRR	Power Supply Rejection Ratio		**60**	82		dB
A_{VOL}	Open Loop Gain		**55**	75		dB
V_{OL}	Output Swing Low	I_L = -5mA		50	**150**	mV

Electrical Specifications Test Conditions: V_{DD} = 3.3V, AV_{DD} = 18V, R_{SET} = 5kΩ, R_1 = 10kΩ, R_2 = 10kΩ, (See Figure 5), V_{COM_OUT} pin connected to IN_N, unless otherwise specified. Typicals are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{OH}	Output Swing High	I_L = 5mA	**17.85**	17.9		V
I_{SC}	Short Circuit Current (Sinking)		**300**	430		mA
	Short Circuit Current (Sourcing)		**450**	555		mA
SR	Slew Rate (Rising)	1kΩ || 8pF Load	**70**	116		V/µs
	Slew Rate (Falling)	1kΩ || 8pF Load	**50**	93		V/µs
t_S	Settling Time to 0.2%			150		ns
BW	-3dB Bandwidth			60		MHz
I^2C INPUTS AND OUTPUT						
V_{IH_I2C}	SDA, SCL Logic 1 Input Voltage		**1.44**			V
V_{IL_I2C}	SDA, SCL Logic 0 Input Voltage				**0.55**	V
V_{HYS_I2C}	SDA, SCL Hysteresis			260		mV
I_{L_I2C}	SDA, SCL Input Leakage Current				**±1**	µA
V_{OL_I2C}	SDA Output Logic Low	I = -3mA			**0.4**	V
$V_{IH\_\overline{WP}}$	$\overline{WP}$ Input Logic High		**$0.7V_{DD}$**			V
$V_{IL\_\overline{WP}}$	$\overline{WP}$ Input Logic Low				**$0.3V_{DD}$**	V
$V_{HYS\_\overline{WP}}$	$\overline{WP}$ Input Hysteresis			260		mV
$I_{L\_\overline{WP}}$	$\overline{WP}$ Input Leakage Current		**-0.20**	-0.5	**-1**	µA
I^2C TIMING						
f_{CLK}	I^2C Clock Frequency				**400**	kHz
t_{SCH}	I^2C Clock High Time		**0.6**			µs
t_{SCL}	I^2C Clock Low Time		**1.3**			µs
t_{DSP}	I^2C Spike Rejection Filter Pulse Width		**0**		**50**	ns
t_{SDS}	I^2C Data Set Up Time		**250**			ns
t_{SDH}	I^2C Data Hold Time		**250**			ns
t_{BUF}	I^2C Time Between Stop and Start		**200**			µs
t_{STS}	I^2C Repeated Start Condition Set-up		**0.6**			µs
t_{STH}	I^2C Repeated Start Condition Hold		**0.6**			µs
t_{SPS}	I^2C Stop Condition Set-up		**0.6**			µs
C_{SDA}	SDA Pin Capacitance				**10**	pF
C_{SCL}	SCL Pin Capacitance				**10**	pF
t_{WR}	EEPROM Write Cycle Time				**100**	ms

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Application Information

LCD panels have a V_{COM} (common voltage) that must be precisely set to minimize flicker. Figure 3 shows a typical V_{COM} adjustment circuit using a mechanical potentiometer, and the equivalent circuit replacement using the ISL24211. Having a digital I^2C interface enables automatic, digital flicker minimization during production test and alignment. After programming, the I^2C interface has no further use therefore, the ISL24211 automatically powers up with the correct V_{COM} voltage programmed previously.

The ISL24211 uses a digitally controllable potentiometer (DCP), with 256 steps of resolution (see Figure 4) to change the current drawn at the DVR_OUT pin, which then changes the voltage created by the R_1 to R_2 resistor divider (see Figure 5). The DVR_OUT voltage is then buffered by A2 to generate a buffered output voltage at the V_{COM_OUT} pin, capable of directly driving the V_{COM} input of an LCD panel. The amount of current sunk is controlled by the setting of the DCP, which is recalled at power-up from the ISL24211's internal EEPROM. The EEPROM is typically programmed during panel manufacture. As noted in the Electrical Specifications on page 4, the ISL24211 requires a minimum AV_{DD} voltage of 10.8V for EEPROM programming, but will work in normal operation (with no EEPROM programming) down to 4.5V.

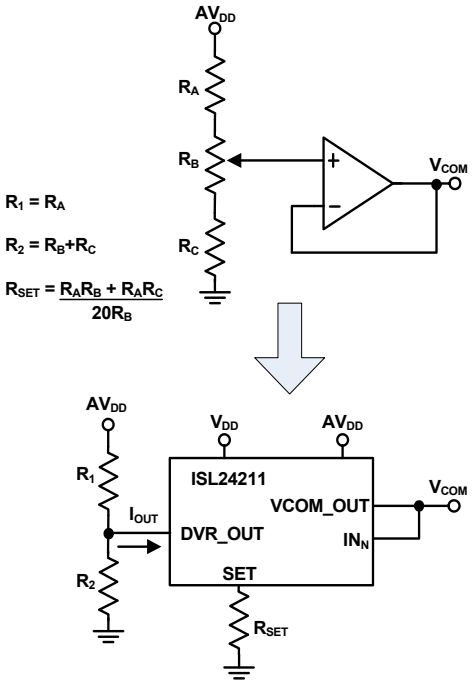


FIGURE 3. MECHANICAL ADJUSTMENT REPLACEMENT

DCP (Digitally Controllable Potentiometer)

The DCP controls the voltage that ultimately controls the SET current. Figure 4 shows the relationship between the register value and the DCP's tap position. Note that a register value of 0 selects the first step of the resistor string. The output voltage of the DCP is given in Equation 1:

$$V_{DCP} = \left(\frac{RegisterValue + 1}{256}\right)\left(\frac{AV_{DD}}{20}\right) \quad \text{(EQ. 1)}$$

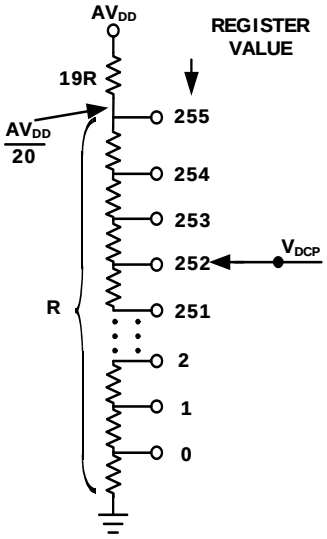


FIGURE 4. SIMPLIFIED SCHEMATIC OF DCP

Output Current Sink

Figure 5 shows the schematic of the DVR_OUT current sink. The combination of amplifier A1, transistor Q1, and resistor R_{SET} forms a voltage-controlled current source, with the voltage determined by the DCP setting.

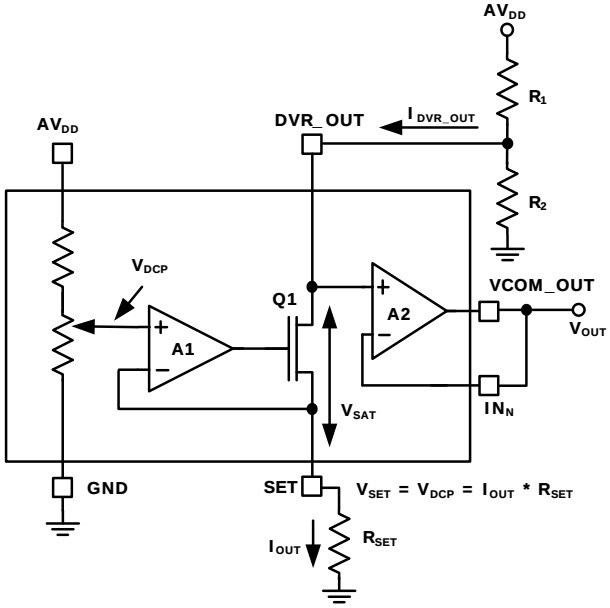


FIGURE 5. CURRENT SINK CIRCUIT

The external R_{SET} resistor sets the full-scale (maximum) sink current that can be pulled from the DVR_OUT node. The relationship between I_{DVR_OUT} and Register Value is shown in Equation 2.

$$I_{DVROUT} = \frac{V_{DCP}}{R_{SET}} = \left(\frac{RegisterValue + 1}{256}\right)\left(\frac{AV_{DD}}{20}\right)\left(\frac{1}{R_{SET}}\right) \quad \text{(EQ. 2)}$$

The maximum value of I_{DVR_OUT} can be calculated by substituting the maximum register value of 255 into Equation 2, resulting in Equation 3:

$$I_{DVROUT(MAX)} = \frac{A_{VDD}}{20R_{SET}} \quad \text{(EQ. 3)}$$

Equation 2 can also be used to calculate the unit sink current step size per Register Code, resulting in Equation 4:

$$I_{STEP} = \frac{AV_{DD}}{(256)(20)(R_{SET})} \quad \text{(EQ. 4)}$$

Determination of R_{SET}

The ultimate goal for the ISL24211 is to generate an adjustable voltage between two endpoints, V_{COM_MIN} and V_{COM_MAX}, with a fixed power supply voltage, AV_{DD}. This is accomplished by choosing the correct values for R_{SET}, R_1 and R_2. The exact value of R_{SET} is not critical. Values from 1k to more than 100k will work under most conditions. The following expression calculates the minimum R_{SET} value:

$$R_{SET(MIN)} = \left(\frac{\frac{AV_{DD}}{16}}{\left(V_{OUT(MIN)} - \frac{AV_{DD}}{20}\right)}\right)(k\Omega) \quad \text{(EQ. 5)}$$

Note that this is the absolute minimum value for R_{SET}. Larger R_{SET} values reduce quiescent power, since R_1 and R_2 are proportional to R_{SET}. The ISL24211 is tested with a 5kΩ R_{SET}.

Determination of R_1 and R_2

With AV_{DD}, $V_{COM(MIN)}$ and $V_{COM(MAX)}$ known and R_{SET} chosen per the above requirements, R_1 and R_2 can be determined using Equations 6 and 7:

$$R_1 = 5120 \cdot R_{SET}\left(\frac{V_{COM(MAX)} - V_{COM(MIN)}}{256 \cdot V_{COM(MAX)} - V_{COM(MIN)}}\right) \quad \text{(EQ. 6)}$$

$$R_2 = 5120 \cdot R_{SET}\left(\frac{V_{COM(MAX)} - V_{COM(MIN)}}{255 \cdot AV_{DD} + V_{COM(MIN)} - 256 \cdot V_{COM(MAX)}}\right) \quad \text{(EQ. 7)}$$

Final Transfer Function

The voltage at DVR_OUT can be calculated from Equation 8:

$$V_{DVROUT} = AV_{DD}\left(\frac{R_2}{R_1+R_2}\right)\left(1 - \frac{RegisterValue + 1}{256}\left(\frac{R_1}{20R_{SET}}\right)\right) \quad \text{(EQ. 8)}$$

With amplifier A2 in the unity-gain configuration (V_{COM_OUT} tied to IN_N as shown in Figure 5), $V_{DVROUT} = V_{COM\_OUT} = V_{COM}$.

Example

As an example, suppose the A_{VDD} supply is 15V, the desired V_{COM_MIN}= 6.5V and the desired V_{COM_MAX} = 8.5V. R_{SET} is arbitrarily chosen to be 7.5kΩ.

First, verify that our chosen R_{SET} meets the minimum requirement described in Equation 5:

$$(7.5k\Omega) > \left(R_{SET(MIN)} = \left(\frac{\frac{15}{16}}{\left(6.5V - \frac{15}{20}\right)}\right) = 0.163k\Omega\right) \quad \text{(EQ. 9)}$$

Using Equations 6 and 7, calculate the values of R_1 and R_2:

$$R_1 = 5120 \cdot 7500 \cdot \left(\frac{8.5-6.5}{256 \cdot 8.5 - 6.5}\right) = 35.4k\Omega \quad \text{(EQ. 10)}$$

$$R_2 = 5120 \cdot 7500 \cdot \left(\frac{8.5 - 6.5}{255 \cdot 15 + 6.5 - 256 \cdot 8.5}\right) = 46.4k\Omega \quad \text{(EQ. 11)}$$

Table 1 shows the resulting V_{COM} voltage as a function of register value for these conditions.

TABLE 1. EXAMPLE V_{DVR_OUT} vs REGISTER VALUE

REGISTER VALUE	V_{DVR_OUT} (V)
0	8.49
20	8.34
40	8.18
60	8.02
80	7.87
100	7.71
120	7.55
127	7.50
140	7.40
160	7.24
180	7.09
200	6.93
220	6.77
240	6.62
255	6.50

Output Voltage Span Calculation

It is also possible to calculate $V_{COM(MIN)}$ and $V_{COM(MAX)}$ from the existing resistor values.

V_{COM_MIN} occurs when the greatest current, $I_{DVR(MAX)}$, is drawn from the middle node of the R1/R2 divider. Substituting RegisterValue = 255 into Equation 8 gives the following:

$$V_{COM(MIN)} = AV_{DD}\left(\frac{R_2}{R_1+R_2}\right)\left(1 - \left(\frac{R_1}{20R_{SET}}\right)\right) \quad \text{(EQ. 12)}$$

Similarly, RegisterValue = 0 for $V_{COM(MAX)}$:

$$V_{COM(MAX)} = AV_{DD}\left(\frac{R_2}{R_1+R_2}\right)\left(1 - \frac{1}{256}\left(\frac{R_1}{20R_{SET}}\right)\right) \quad \text{(EQ. 13)}$$

By finding the difference of Equation 13 and Equation 12, the total span of V_{COM} can be found:

$$V_{COM}SPAN = AV_{DD}\left(\frac{R_2}{R_1+R_2}\right)\left(1-\frac{1}{256}\right)\left(\frac{R_1}{20R_{SET}}\right) \quad \text{(EQ. 14)}$$

Assuming that the $I_{DVROUT}(MIN)$ = 0 instead of I_{STEP}, the expression in Equation 14 simplifies to:

$$V_{COM}SPAN = \left(\frac{R_1 \cdot R_2}{R_1+R_2}\right)\left(\frac{AV_{DD}}{20R_{SET}}\right) = \left(\frac{R_1 \cdot R_2}{R_1+R_2}\right)I_{DVROUT}(MAX) \quad \text{(EQ. 15)}$$

DVR_OUT Pin Leakage Current

When the voltage on the DVR_OUT pin is greater than 10V, an additional leakage current flows into the pin in addition to the I_{SET} current. Figure 6 shows the I_{SET} current and the DVR_OUT pin current for DVR_OUT pin voltage up to 19V. In applications where the voltage on the DVR_OUT pin will be greater than 10V, the actual output voltage will be lower than the voltage calculated by Equation 8. The graph in Figure 6 was measured with R_{SET} = 4.99kΩ.

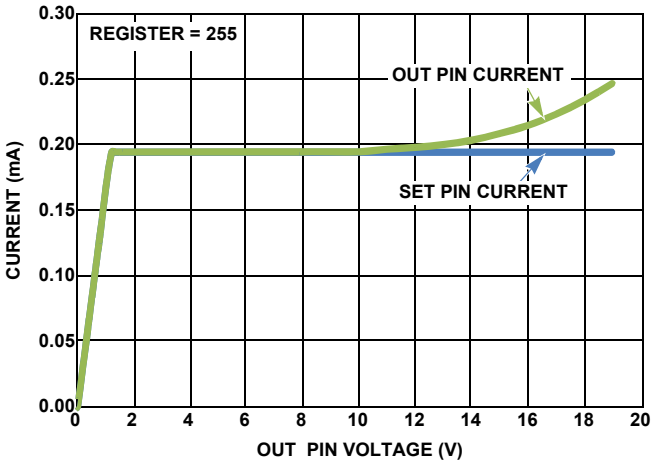


FIGURE 6. DVR_OUT PIN LEAKAGE CURRENT

Power Supply Sequence

The recommended power supply sequencing is shown in Figure 7. When applying power, V_{DD} should be applied before or at the same time as AV_{DD}. The minimum time for t_{VS} is 0µs. When removing power, the sequence of V_{DD} and AV_{DD} is not important.

Do not remove V_{DD} or AV_{DD} within 100ms of the start of the EEPROM programming cycle. Removing power before the EEPROM programming cycle is completed may result in corrupted data in the EEPROM.

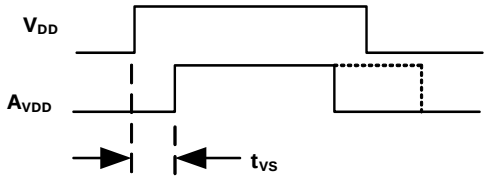


FIGURE 7. POWER SUPPLY SEQUENCE

Operating and Programming Supply Voltage and Current

To program the EEPROM, AV_{DD} must be ≥10.8V. If programming is not required, the ISL24211 will operate over an AV_{DD} range of 4.5V to 19V.

During EEPROM programming, I_{DD} and I_{AVDD} will temporarily be higher than their quiescent currents. Figure 8 shows a typical I_{DD} and I_{AVDD} current profile during EEPROM programming. The current pulses are Erase and Write cycles. The EEPROM programming algorithm is shown in Figure 9. The algorithm attempts up to 4 erase cycles and 4 programming cycles, however typical parts only require 1 cycle of each, sometimes 2 when AV_{DD} is near the minimum 10.8V limit.

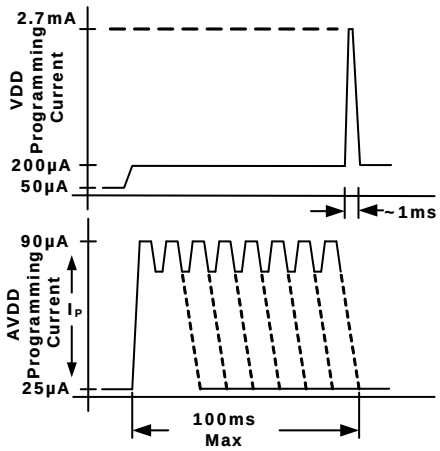


FIGURE 8. I_{DD} AND I_{AVDD} CURRENT PROFILE DURING EEPROM PROGRAMMING

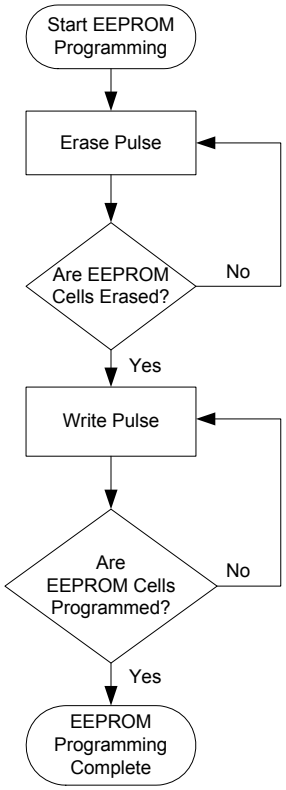


FIGURE 9. EEPROM PROGRAMMING FLOWCHART

ISL24211 Programming

The ISL24211 accepts I^2C bus address and data when the $\overline{WP}$ pin is high. The ISL24211 ignores the I^2C bus when the $\overline{WP}$ pin is low. Figure 10 shows the serial data format for writing the register and programming the EEPROM. Figure 11 shows the serial data format for reading the DAC register. Table 2 shows the truth table for reading and writing the device.

TABLE 2. ISL24211 READ AND WRITE CONTROL

$\overline{WP}$ PIN	R/$\overline{W}$	$\overline{P}$	FUNCTION
0	1	X	Read Register.
0	0	1	Will acknowledge I^2C transactions. Will not write to register.
0	0	0	Will acknowledge I^2C transactions. Will not write to EEPROM.
1	1	X	Read DAC Register.
1	0	1	Write DAC Register.
1	0	0	Program EEPROM.

Programming the EEPROM memory transfers the current DAC register value to the EEPROM and occurs when the control bits select the programming mode and the AV_{DD} voltage is >10.8V. After the EEPROM programming cycle is started, the $\overline{WP}$ pin can be returned to logic low while the EEPROM write completes, which takes a maximum of 100ms.

The ISL24211 uses a 6-bit I^2C address, which is “100111yx” for the first transmitted byte. Bit x is the R/$\overline{W}$ bit, and Bit y is the LSB (D0) of the DCP register code to be written. The complete read and write protocol is shown in Figures 10 and 11.

I^2C Bus Signals

The ISL24211 uses fixed voltages for its I^2C thresholds, rather than the percentage of V_{DD} described in the I^2C specification (see Table 3). This should not cause a problem in most systems, but the I^2C logic levels in a specific design should be checked to ensure they are compatible with the ISL24211.

TABLE 3. ISL24211 I^2C BUS LOGIC LEVELS

SYMBOL	ISL24211	I^2C STANDARD
V_{IL_I2C}	0.55V	$0.3*V_{DD}$
V_{IH_I2C}	1.44V	$0.7*V_{DD}$

I²C Read and Write Format

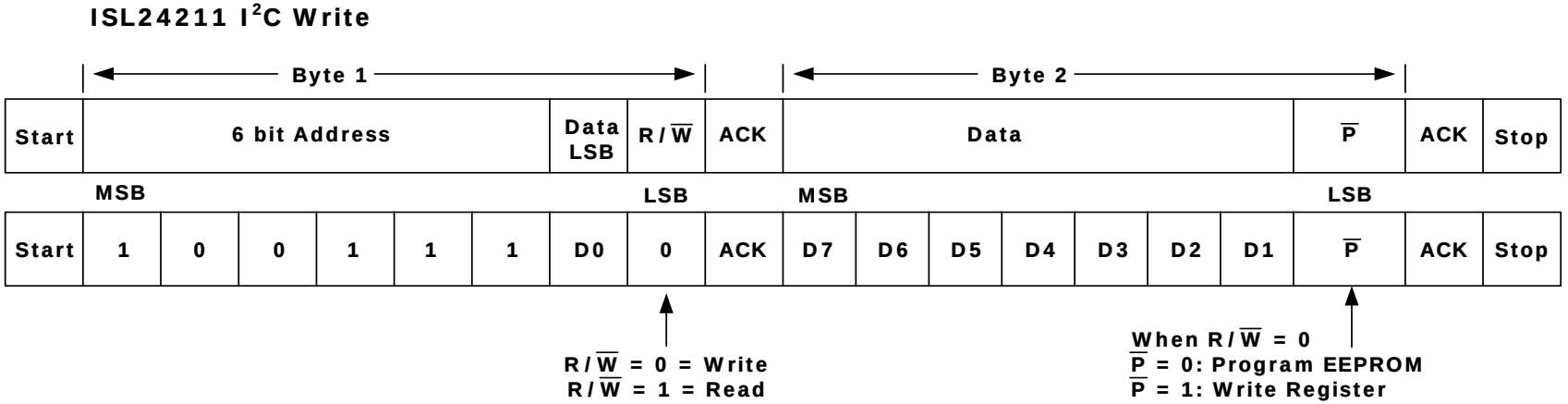


FIGURE 10. I²C WRITE FORMAT

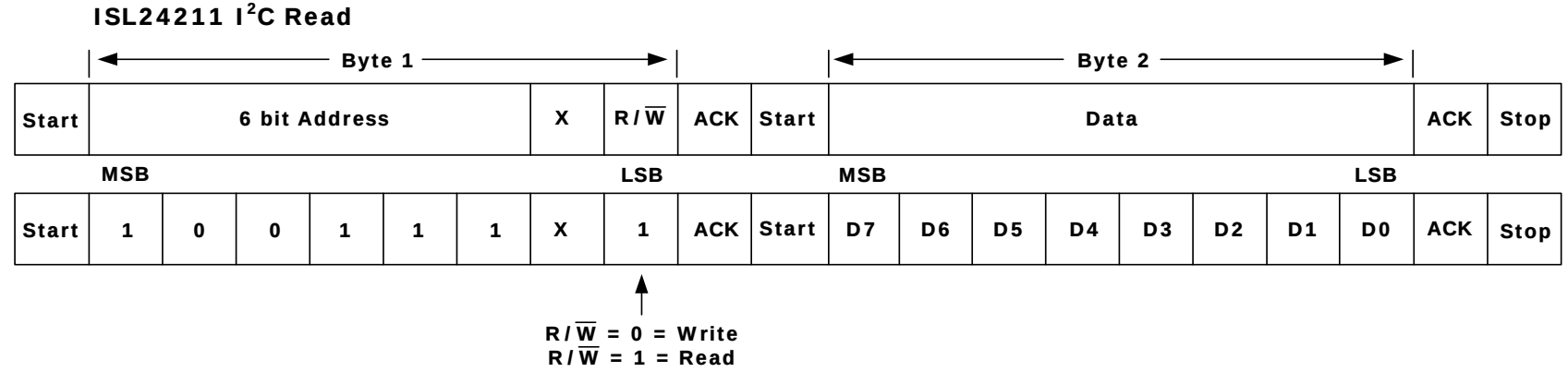


FIGURE 11. I²C READ FORMAT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
2/23/11	FN7585.0	Initial Release.

Products

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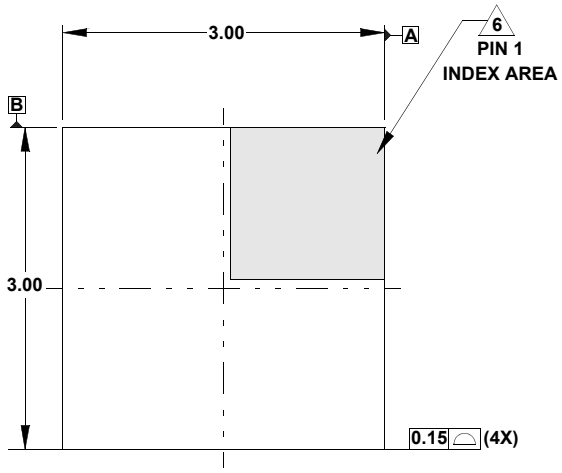
FITs are available from our website at http://rel.intersil.com/reports/sear

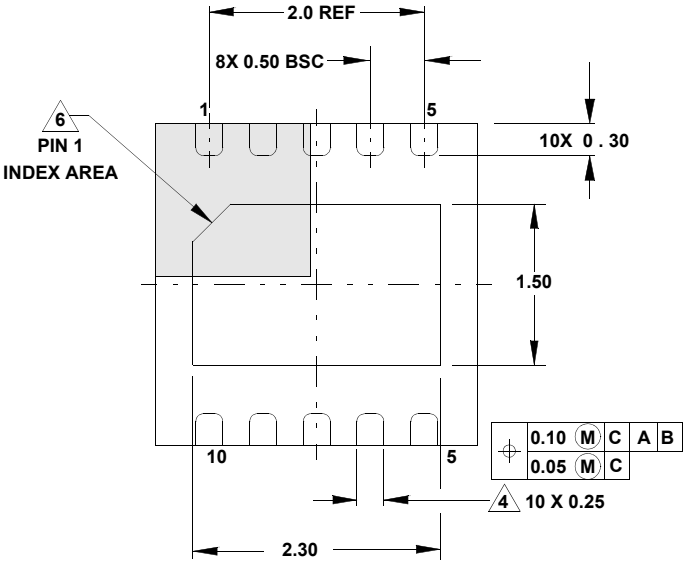
Package Outline Drawing

L10.3x3A

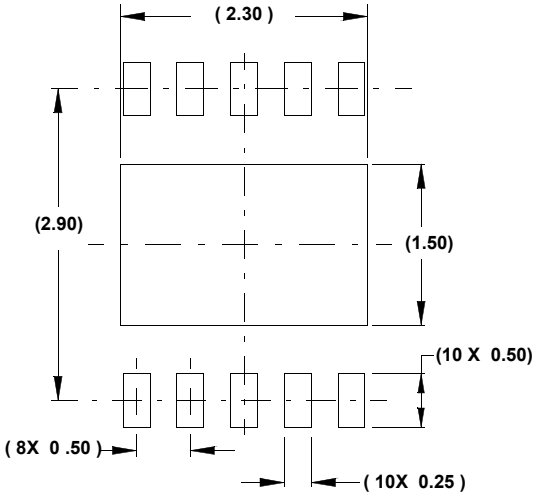
10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 5, 3/10



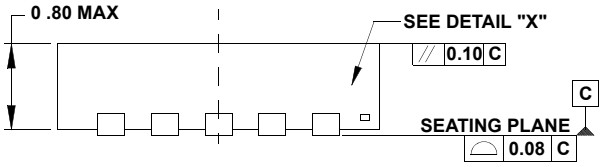
TOP VIEW



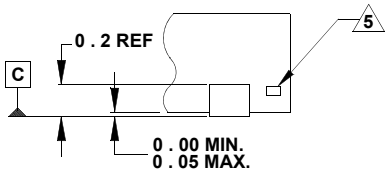
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
   Angular ±2.50°
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229-WEED-3 except exposed pad length (2.30mm).