DS90C402 Dual Low Voltage Differential Signaling (LVDS) Receiver

Check for Samples: DS90C402

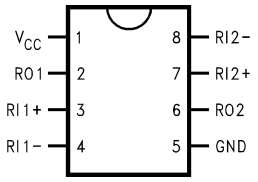
FEATURES

- **Ultra Low Power Dissipation**
- **Operates above 155.5 Mbps**
- **Standard TIA/EIA-644**
- **8 Lead SOIC Package saves PCB space**
- **V_{CM} ±1V center around 1.2V**
- **±100 mV Receiver Sensitivity**

DESCRIPTION

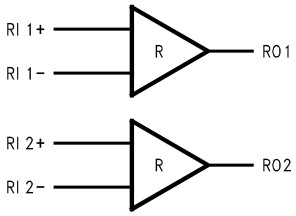
The DS90C402 is a dual receiver device optimized for high data rate and low power applications. This device along with the DS90C401 provides a pair chip solution for a dual high speed point-to-point interface. The device is in a PCB space saving 8 lead small outline package. The receiver offers ±100 mV threshold sensitivity, in addition to common-mode noise protection.

Connection Diagram



See Package Number D (SOIC)

Functional Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{CC})		−0.3V to +6V
Input Voltage (R_{IN+}, R_{IN-})		−0.3V to (V_{CC} + 0.3V)
Output Voltage (R_{OUT})		−0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation @ +25°C	D Package	1025 mW
	Derate D Package	8.2 mW/°C above +25°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)		+260°C
Maximum Junction Temperature		+150°C
ESD Rating[3]	(HBM, 1.5 kΩ, 100 pF)	≥ 3,500V
	(EIAJ, 0 Ω, 200 pF)	≥ 250V

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) ESD Rating: HBM (1.5 kΩ, 100 pF) ≥ 3,500V EIAJ (0Ω, 200 pF) ≥ 250V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Receiver Input Voltage	GND		2.4	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} = + 1.2V		R_{IN+}, R_{IN-}			+100	mV
V_{TL}	Differential Input Low Threshold				−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V		−10	±1	+10	µA
		V_{IN} = 0V			−10	± 1	+10	µA
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		R_{OUT}	3.8	4.9		V
		I_{OH} = −0.4mA, Inputs terminated			3.8	4.9		V
		I_{OH} = −0.4mA, Inputs Open			3.8	4.9		V
		I_{OH} = −0.4mA, Inputs Shorted				4.9		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				0.07	0.3	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V[3]			−15	−60	−100	mA
I_{CC}	No Load Supply Current	Inputs Open		V_{CC}		3.5	10	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
(2) All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.
(3) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Switching Characteristics

V_{CC} = +5.0V ± 10%, T_A = −40°C to +85°C(1)(2)(3)(4)(5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 5 pF, V_{ID} = 200 mV (Figure 1 and Figure 2)	1.0	3.40	6.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	3.48	6.0	ns
t_{SKD}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$		0	0.08	1.2	ns
t_{SK1}	Channel-to-Channel Skew(3)		0	0.6	1.5	ns
t_{SK2}	Chip to Chip Skew(4)				5.0	ns
t_{TLH}	Rise Time			0.5	2.5	ns
t_{THL}	Fall Time			0.5	2.5	ns

(1) All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, ZO = 50Ω, t_r and t_f (0%–100%) ≤ 1 ns for R_{IN}.
(3) Channel-to-Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with an event on the inputs.
(4) Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.
(5) C_L includes probe and jig capacitance.

Parameter Measurement Information

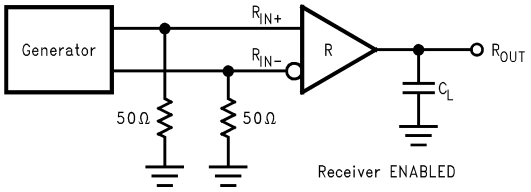


Figure 1. Receiver Propagation Delay and Transition Time Test Circuit

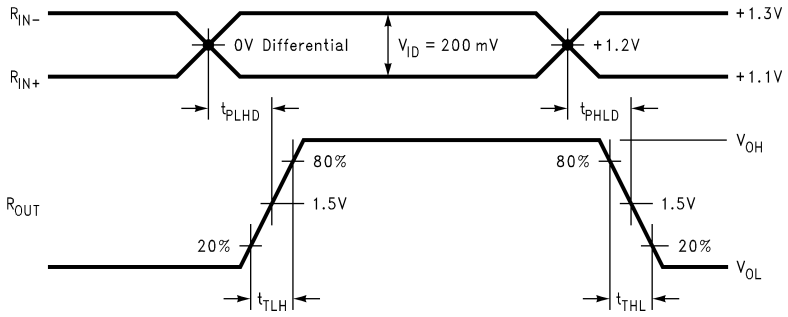


Figure 2. Receiver Propagation Delay and Transition Time Waveforms

TYPICAL APPLICATION

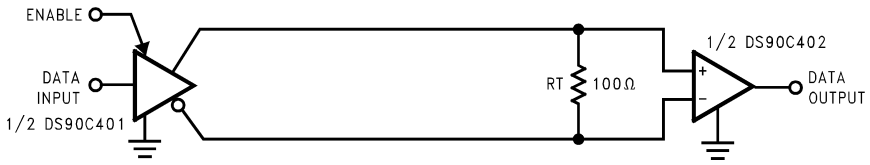


Figure 3. Point-to-Point Application

Applications Information

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 3. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90C402 differential line receiver is capable of detecting signals as low as 100 mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. Both receiver input pins should honor their specified operating input voltage range of 0V to +2.4V (measured from each pin to ground), exceeding these limits may turn on the ESD protection circuitry which will clamp the bus voltages.

Fail-Safe Feature:

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DS90C402 is a dual receiver device, and if an application requires only one receiver, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will ensure a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

PIN DESCRIPTIONS

Pin No.	Name	Description
2, 6	R_{OUT}	Receiver output pin
3, 7	$R_{IN}+$	Positive receiver input pin
4, 8	$R_{IN}-$	Negative receiver input pin
5	GND	Ground pin
1	V_{CC}	Positive power supply pin, +5V ± 10%

Typical Performance Characteristics

Output High Voltage vs Power Supply Voltage

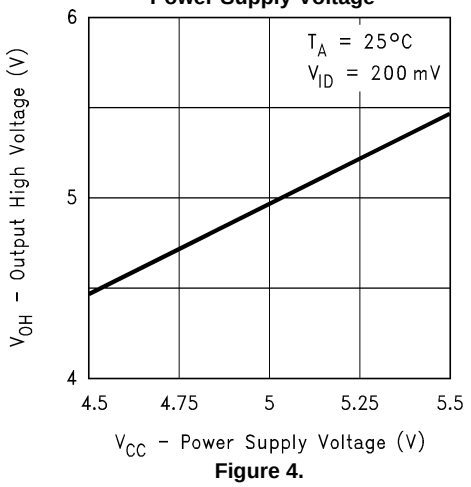


Figure 4.

Output High Voltage vs Ambient Temperature

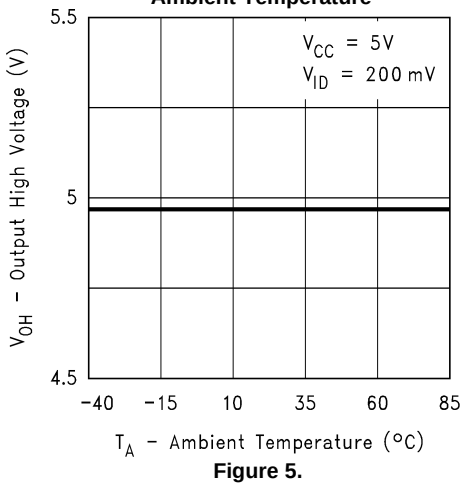


Figure 5.

Output Low Voltage vs Power Supply Voltage

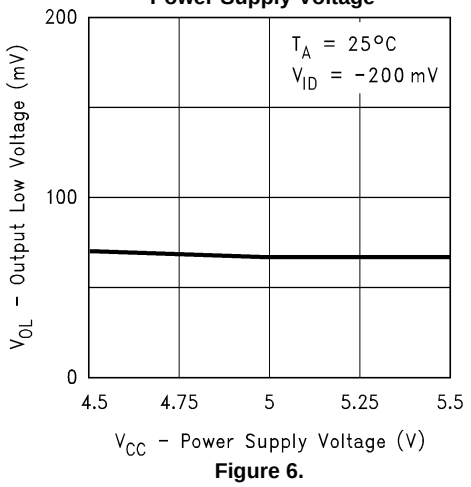


Figure 6.

Output Low Voltage vs Ambient Temperature

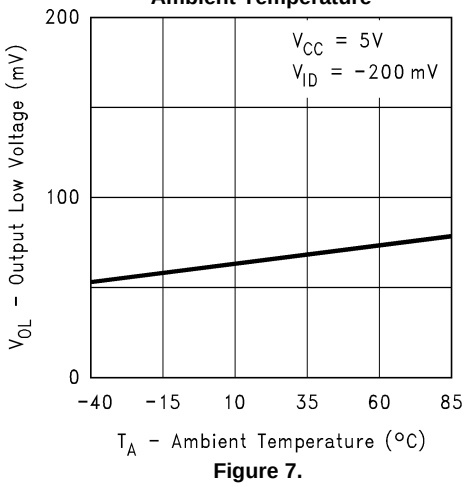


Figure 7.

Output Short Circuit Current vs Power Supply Voltage

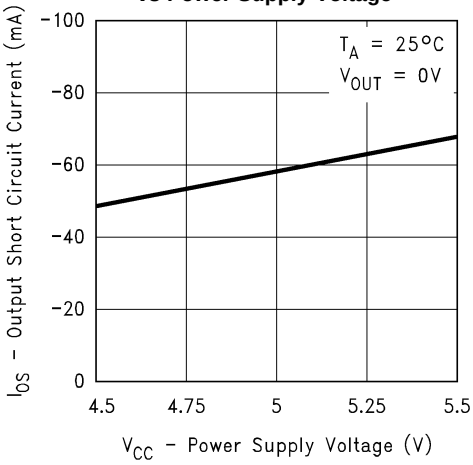


Figure 8.

Output Short Circuit Current vs Ambient Temperature

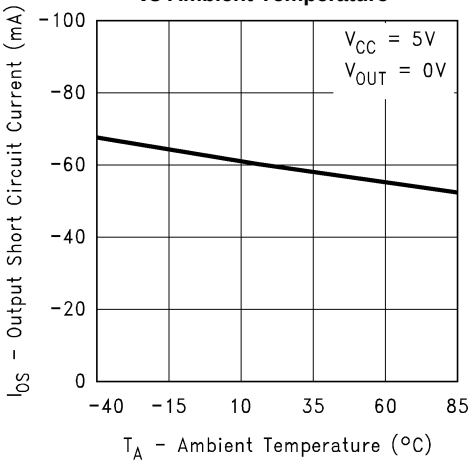


Figure 9.

Typical Performance Characteristics (continued)

Differential Propagation Delay vs Power Supply Voltage

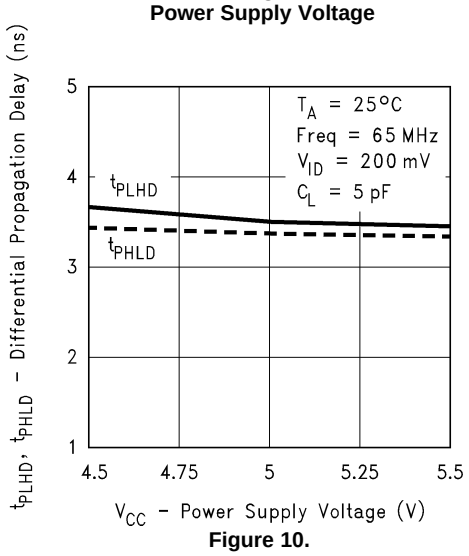


Figure 10.

Differential Propagation Delay vs Ambient Temperature

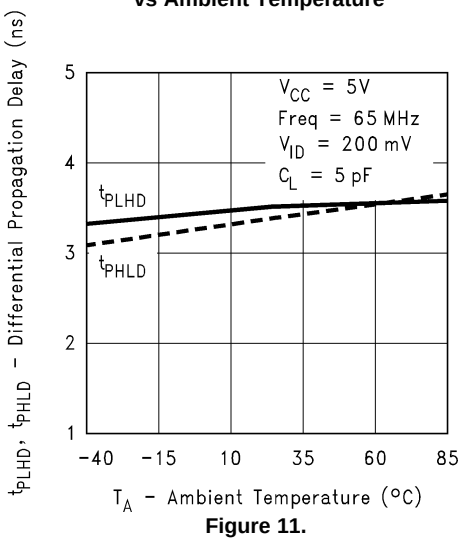


Figure 11.

Differential Skew vs Power Supply Voltage

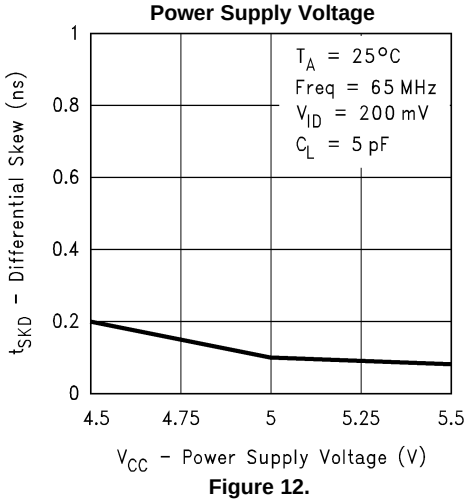


Figure 12.

Differential Skew vs Ambient Temperature

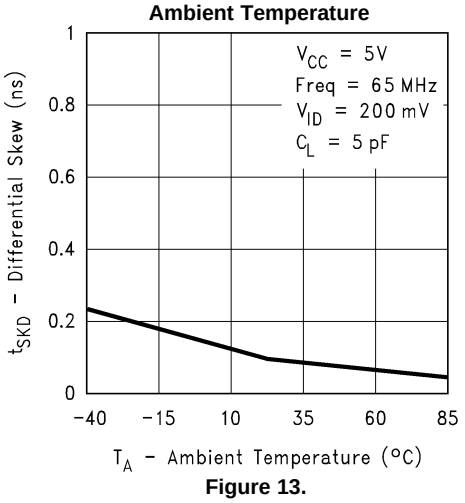


Figure 13.

Transition Time vs Power Supply Voltage

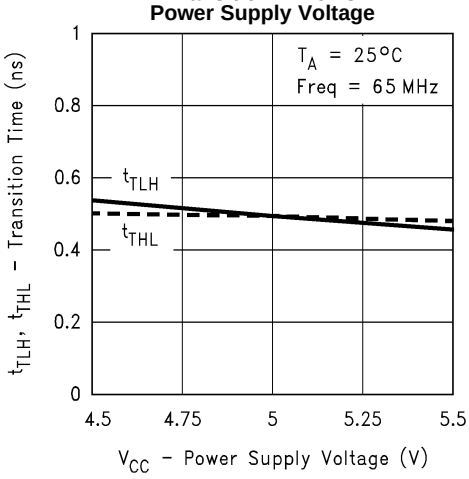


Figure 14.

Transition Time vs Ambient Temperature

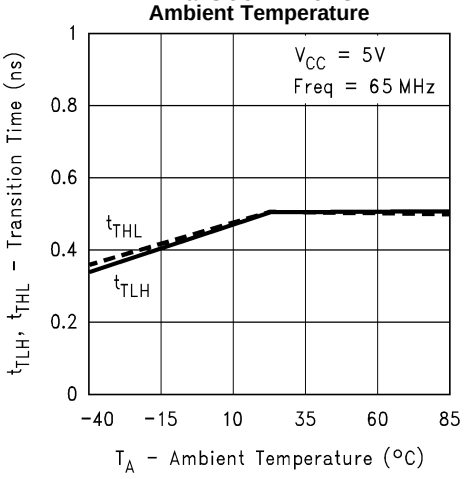


Figure 15.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90C402M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	DS90C 402M	
DS90C402M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	DS90C 402M	Samples
DS90C402MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	DS90C 402M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

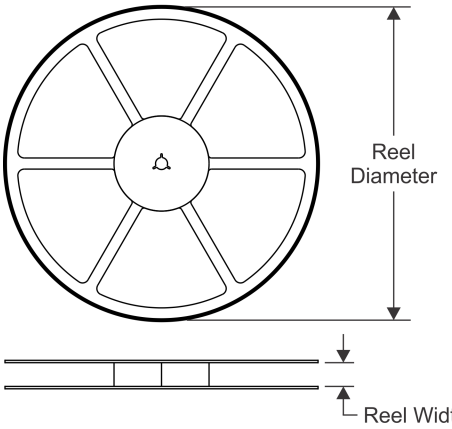
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

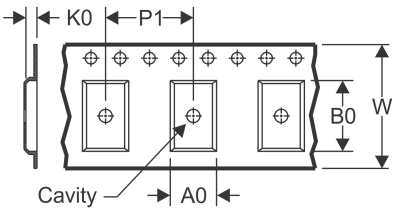
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

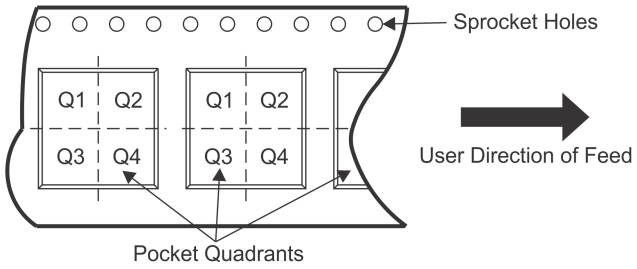


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

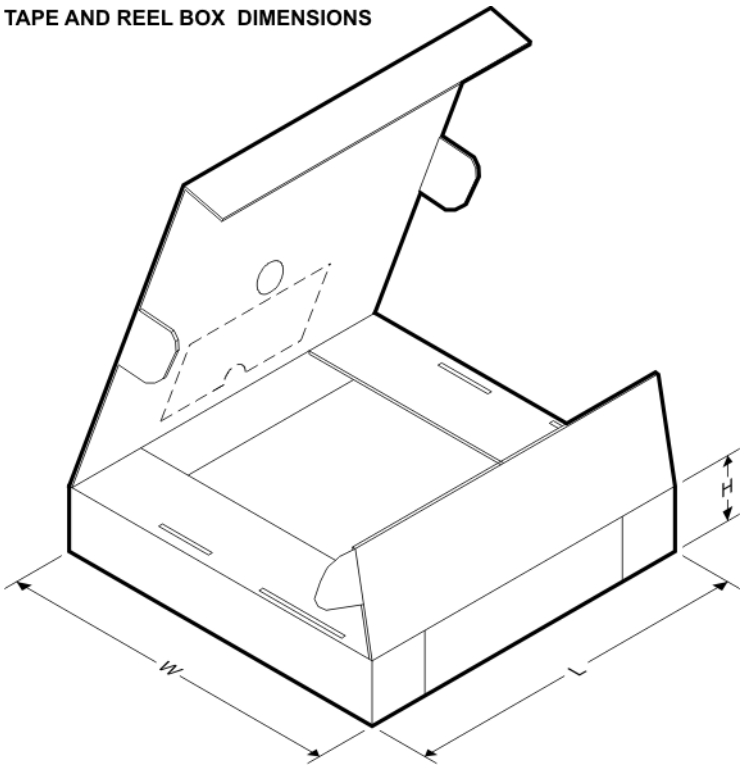
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

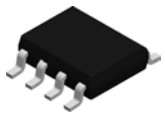
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90C402MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90C402MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

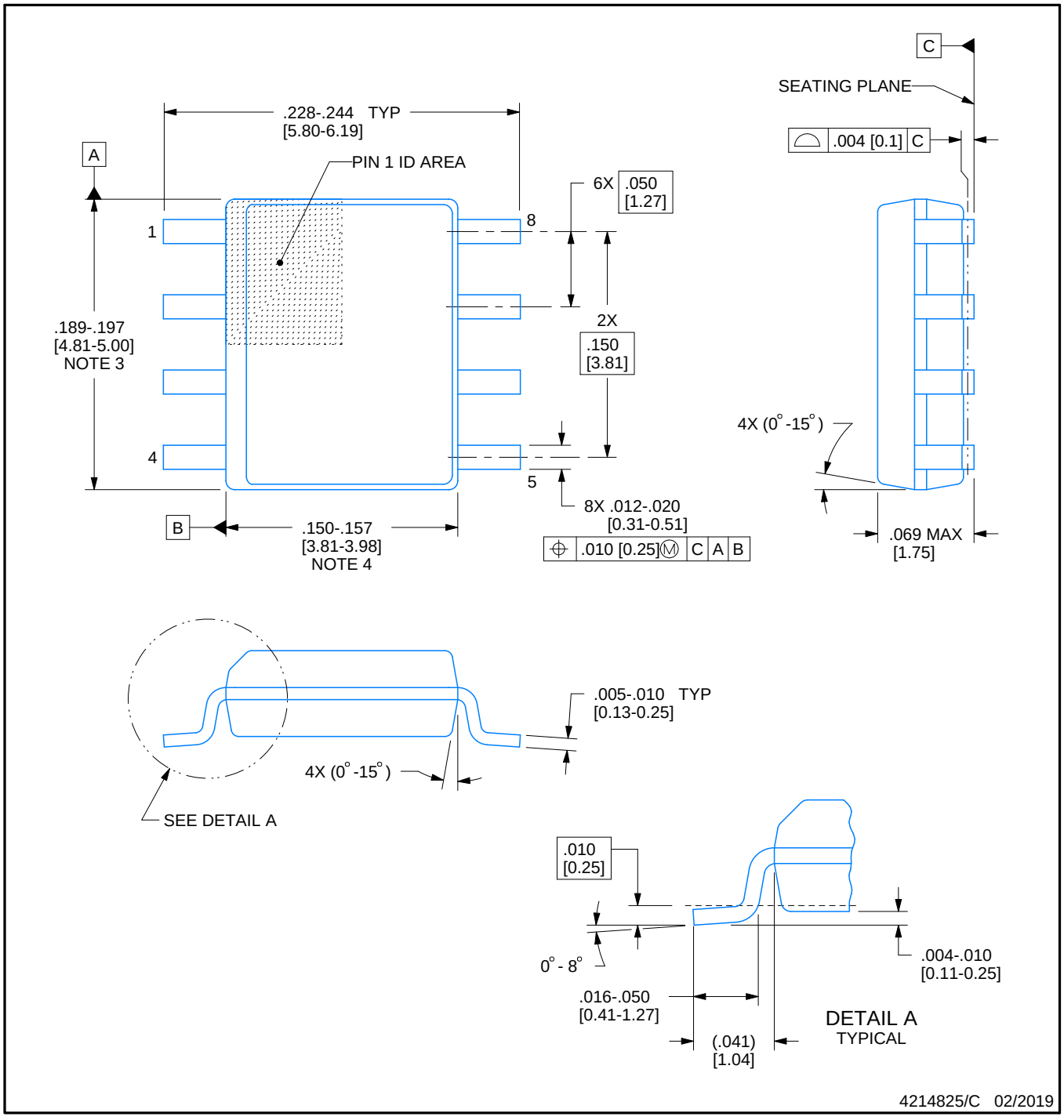


PACKAGE OUTLINE

D0008A

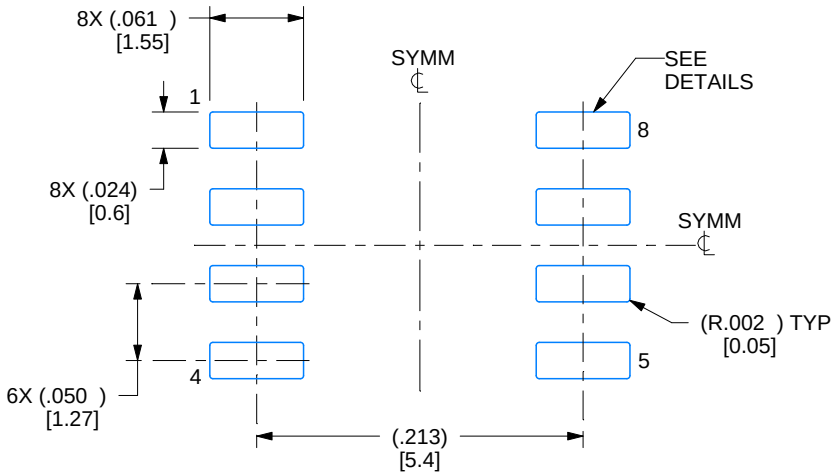
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

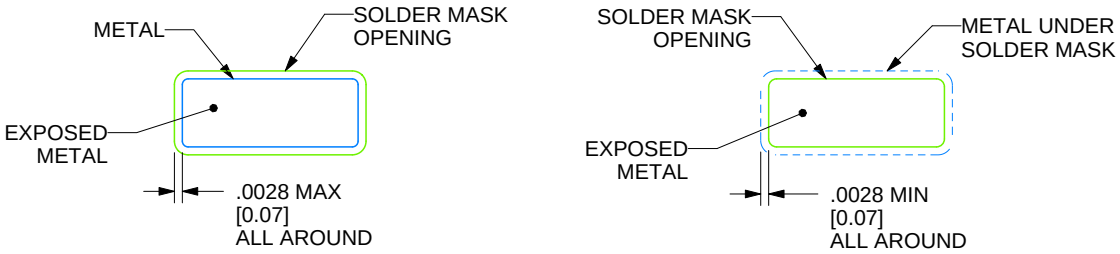


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

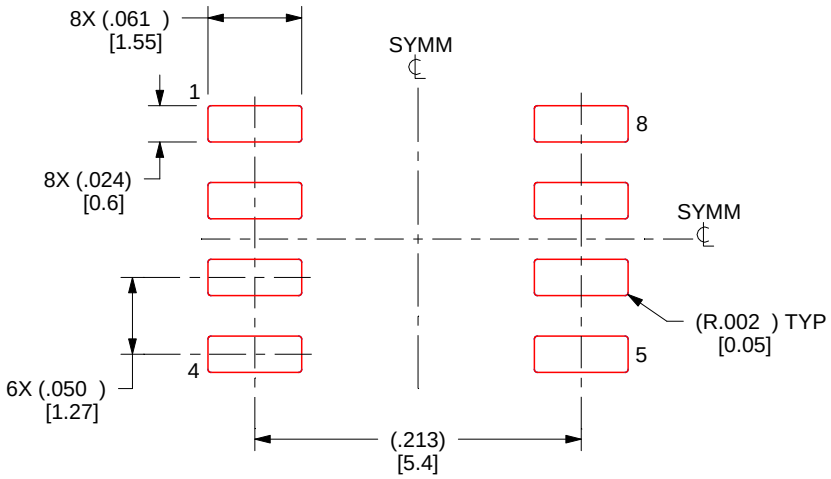
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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