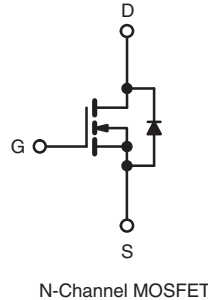
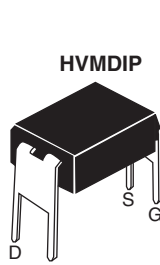


Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	$V_{GS} = 5.0$ V	0.54
Q_g (Max.) (nC)	6.1	
Q_{gs} (nC)	2.6	
Q_{gd} (nC)	3.3	
Configuration	Single	



FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS} = 4$ V and 5 V
- 175 °C Operating Temperature
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912


 Available
RoHS*
 COMPLIANT

Note

* Lead (Pb)-containing terminations are not RoHS-compliant. Exemptions may apply.

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION	
Package	HVMDIP
Lead (Pb)-free	IRLD110PbF
	SiHLD110-E3
SnPb	IRLD110
	SiHLD110

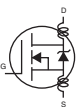

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	100	V	
Gate-Source Voltage	V_{GS}	± 10		
Continuous Drain Current	V_{GS} at 5.0 V	$T_A = 25$ °C	A	
		$T_A = 100$ °C		
Pulsed Drain Current ^a	I_{DM}	8.0		
Linear Derating Factor		0.0083	W/°C	
Single Pulse Avalanche Energy ^b	E_{AS}	100	mJ	
Avalanche Current ^a	I_{AR}	1.0	A	
Repetitive Avalanche Energy ^a	E_{AR}	0.13	mJ	
Maximum Power Dissipation	$T_A = 25$ °C	P_D	1.3	W
Peak Diode Recovery dV/dt ^c	dV/dt	5.5	V/ns	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d		

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$ V, starting $T_J = 25$ °C, $L = 6.4$ mH, $R_g = 25$ Ω , $I_{AS} = 5.6$ A (see fig. 12).
- $I_{SD} \leq 5.6$ A, $dI/dt \leq 75$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
- 1.6 mm from case.



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$		-	0.12	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 10\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}$	$I_D = 0.60\text{ A}^b$	-	-	0.54	Ω
		$V_{GS} = 4.0\text{ V}$	$I_D = 0.50\text{ A}^b$	-	-	0.76	
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 0.60\text{ A}^b$		1.3	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$		-	250	-	μF
Output Capacitance	C_{oss}			-	80	-	
Reverse Transfer Capacitance	C_{rss}			-	15	-	
Total Gate Charge	Q_g	$V_{GS} = 5.0\text{ V}$	$I_D = 5.6\text{ A}, V_{DS} = 80\text{ V}, \text{ see fig. 6 and 13}^b$	-	-	6.1	nC
Gate-Source Charge	Q_{gs}			-	-	2.6	
Gate-Drain Charge	Q_{gd}			-	-	3.3	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, I_D = 5.6\text{ A}, R_g = 12\text{ }\Omega, R_D = 8.4\text{ }\Omega, \text{ see fig. 10}^b$		-	9.3	-	ns
Rise Time	t_r			-	4.7	-	
Turn-Off Delay Time	$t_{d(off)}$			-	16	-	
Fall Time	t_f			-	17	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L_S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	1.0	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	8.0	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 1.0\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 5.6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	110	130	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.50	0.65	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\text{ }\%$.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

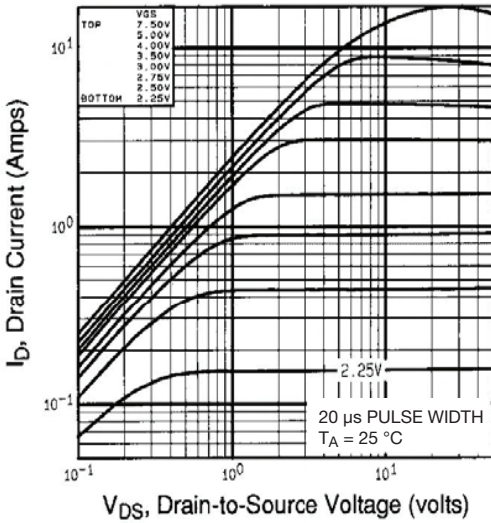


Fig. 1 - Typical Output Characteristics, $T_A = 25\text{ }^\circ\text{C}$

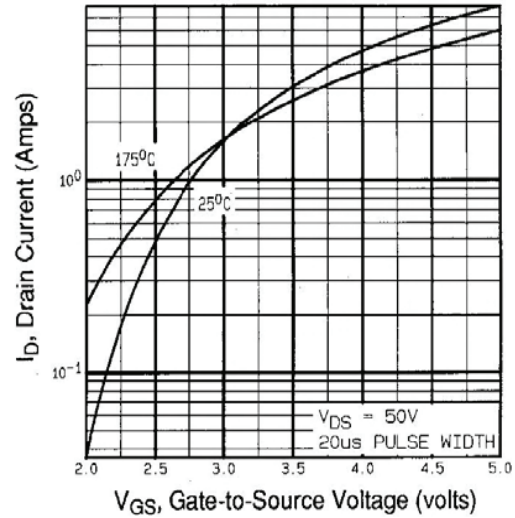


Fig. 3 - Typical Transfer Characteristics

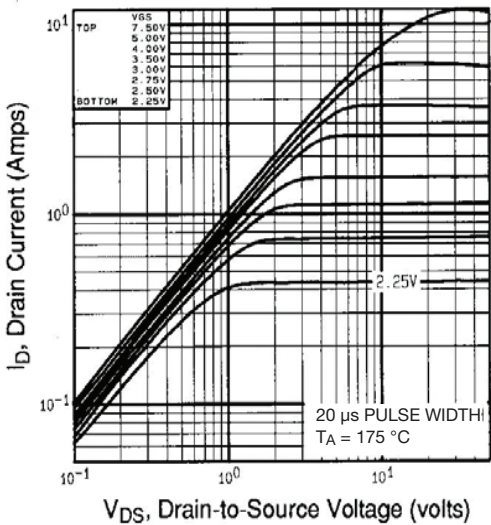


Fig. 2 - Typical Output Characteristics, $T_A = 175\text{ }^\circ\text{C}$

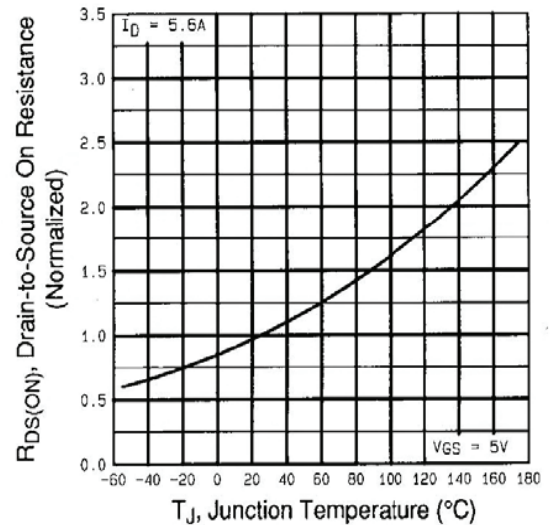


Fig. 4 - Normalized On-Resistance vs. Temperature

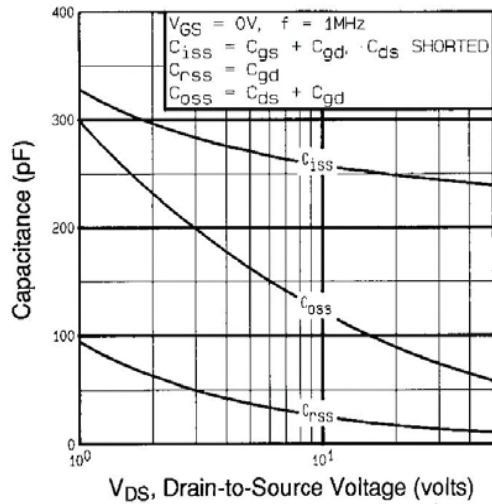


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

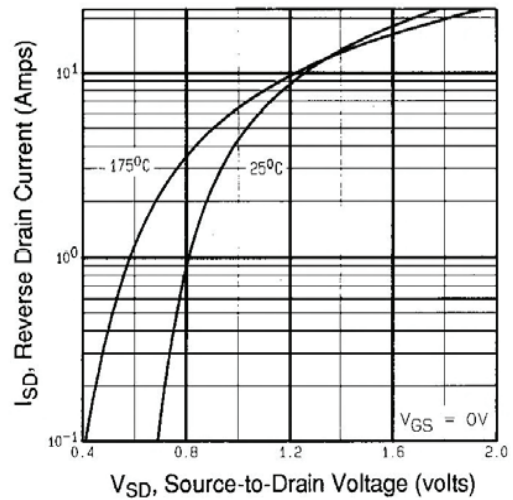


Fig. 7 - Typical Source-Drain Diode Forward Voltage

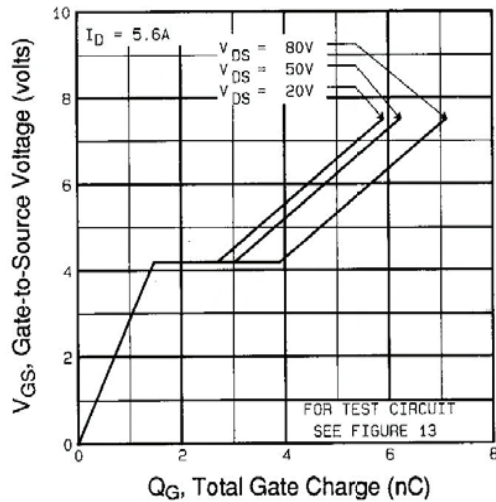


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

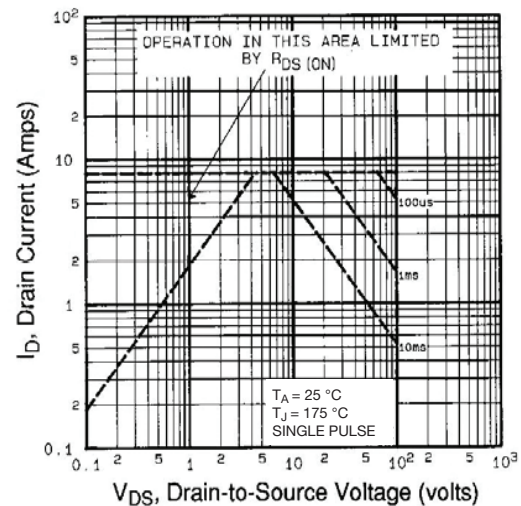


Fig. 8 - Maximum Safe Operating Area

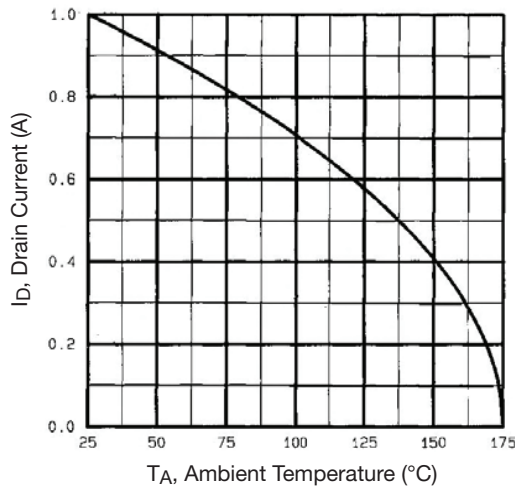


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

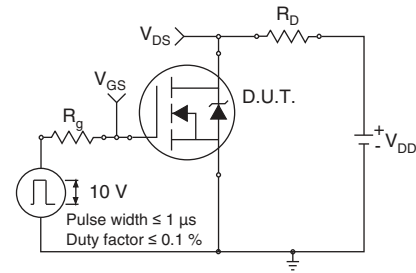


Fig. 10 - Switching Time Test Circuit

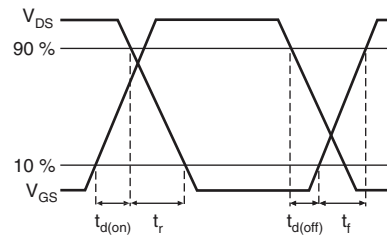


Fig. 11 - Switching Time Waveforms

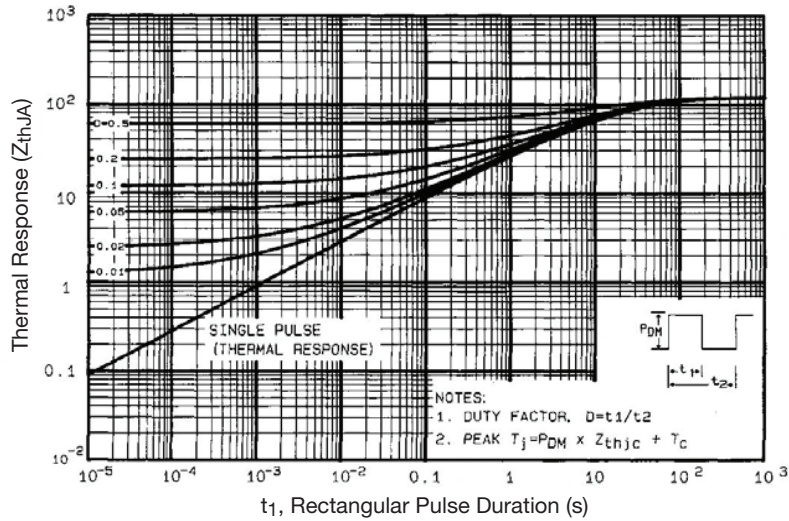


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

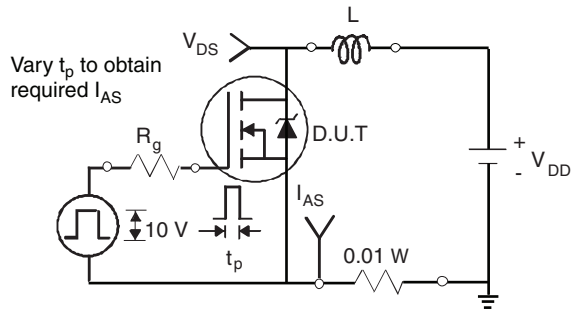


Fig. 13 - Unclamped Inductive Test Circuit

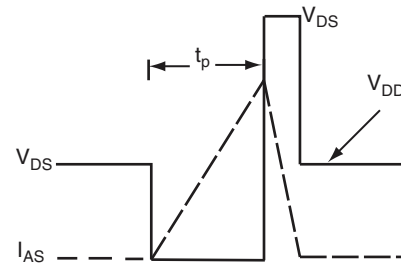


Fig. 14 - Unclamped Inductive Waveforms

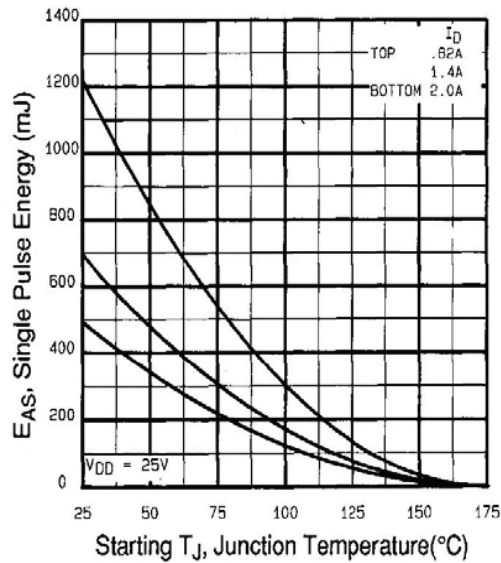


Fig. 15 - Maximum Avalanche Energy vs. Drain Current

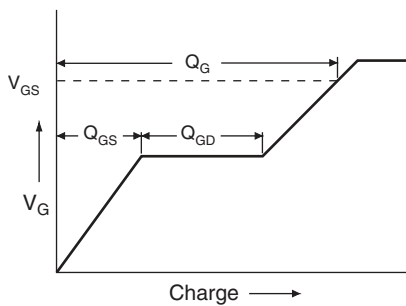


Fig. 16 - Basic Gate Charge Waveform

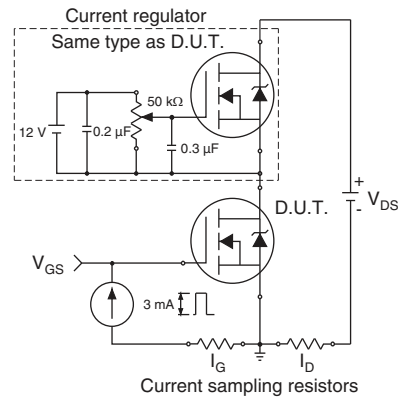
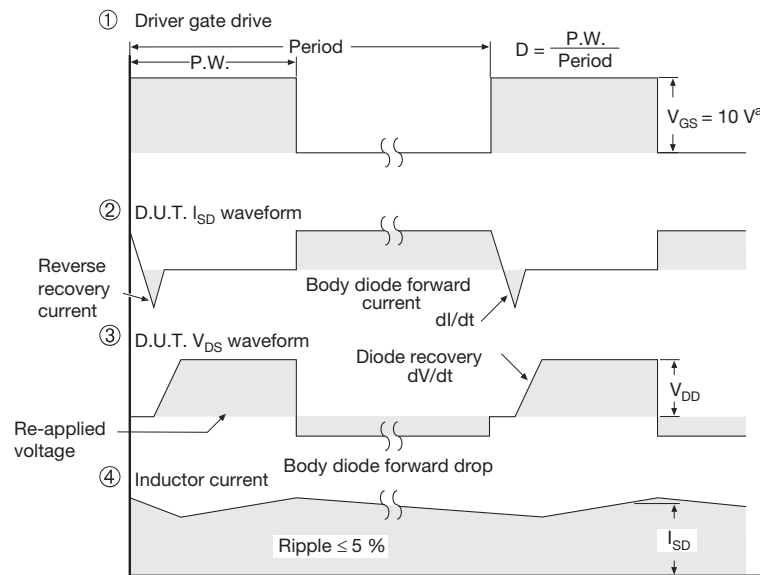
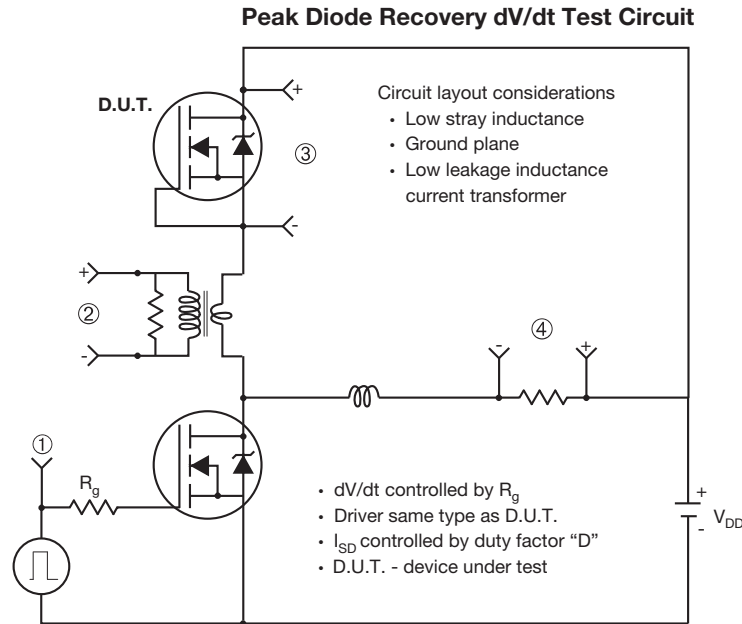


Fig. 17 - Gate Charge Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 18 - For N-Channel

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HVM DIP (High voltage)



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10
DWG: 5974

Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.



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