



## IF AUTOMATIC GAIN CONTROLLER (IF-AGC), 50 - 800 MHz

### Typical Applications

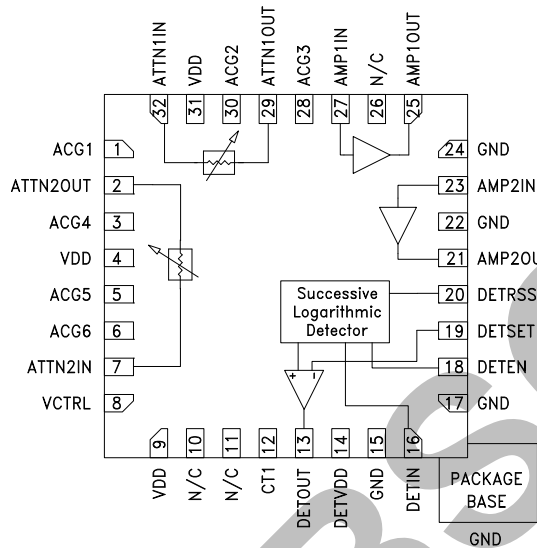
The HMC992LP5E is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

### Features

- Wide Gain Control Range: -10 to +38 dB
- High Output IP3: +40 dBm
- Positive Analog Control: 0V to +5V
- Configurable with 1 or 2 Attenuators
- 32 Lead 5x5 mm SMT Package: 25 mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC992LP5E is an IF analog controlled variable gain amplifier composed of two identical voltage variable attenuators in combination with an InGaP HBT gain block MMIC amplifier which operates from 0.1 to 0.8 GHz, and can be controlled to provide anywhere from -10 dB attenuation, to 40 dB of gain. The HMC992LP5E delivers noise figure of 6 dB in its maximum gain state, with output IP3 of up to +40 dBm. The HMC992LP5E is housed in a RoHS compliant 5x5 mm QFN leadless package, and requires no external matching components.

### Electrical Specifications,

$T_A = +25^\circ\text{C}$ , 50 Ohm System,  $V_{dd} = ATTN1V_{dd} = ATTN2V_{dd} = DETV_{dd} = +5V$  [1]

| Parameter                       | Frequency   | Min. | Typ.           | Max. | Units    |
|---------------------------------|---|------|----------------|------|----------|
| Gain (VCTRL = 0V)               | 1 Attenuator Operation<br>0.1 - 0.5 GHz<br>0.8 GHz            | 35   | 40<br>36       |      | dB<br>dB |
|                                 | 2 Attenuator Operation<br>0.1 - 0.3 GHz<br>0.5 GHz<br>0.8 GHz | 32   | 38<br>36<br>33 |      | dB       |
| Gain Control Range              | 1 Attenuator Operation<br>0.1 - 0.5 GHz<br>0.8 GHz            |      | 25<br>20       |      | dB       |
|                                 | 2 Attenuator Operation<br>0.1 - 0.5 GHz<br>0.8 GHz            |      | 48<br>42       |      | dB       |
| Input Return Loss (VCTRL = 0V)  | 1 Attenuator Operation<br>0.1 - 0.5 GHz<br>0.8 GHz            |      | 15<br>12       |      | dB       |
|                                 | 2 Attenuator Operation<br>0.1 - 0.8 GHz                       |      | 12             |      | dB       |
| Output Return Loss (VCTRL = 0V) | 1 Attenuator Operation<br>0.1 GHz<br>0.3 - 0.5 GHz<br>0.8 GHz |      | 11<br>12<br>14 |      | dB       |
|                                 | 2 Attenuator Operation<br>0.1 - 0.8 GHz                       |      | 12             |      | dB       |

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**IF AUTOMATIC GAIN CONTROLLER  
(IF-AGC), 50 - 800 MHz**
**Electrical Specifications** (continued),

 $T_A = +25^\circ\text{C}$ , 50 Ohm System,  $V_{dd} = \text{ATTN1}V_{dd} = \text{ATTN2}V_{dd} = \text{DET}V_{DD} = +5\text{V}$  [1]

| Parameter   | Frequency   | Min.        | Typ.        | Max. | Units        |
|---|-------------|-------------|-------------|------|--------------|
| Output Third Order Intercept Point<br>(Two-Tone Output Power= 0 dBm Each Tone) (VCTRL = 0V) | 0.1 GHz     |             | 42          |      | dBm<br>dBm   |
|   | 0.3 GHz     |             | 44          |      |              |
|   | 0.5 GHz     |             | 39          |      |              |
|   | 0.8 GHz     |             | 35          |      |              |
| Output Power for 1dB Compression (VCTRL = 0V)   | 0.1 GHz     |             | 18.5        |      | dBm<br>dBm   |
|   | 0.3 GHz     |             | 18.9        |      |              |
|   | 0.5 GHz     |             | 19          |      |              |
|   | 0.8 GHz     |             | 18.8        |      |              |
| Noise Figure (VCTRL = 0V)   |             |             | 6           |      | dB           |
| Supply Current (I <sub>dd</sub> )   |             |             | 215         |      | mA           |
| <b>Power Detector</b>   |             |             |             |      |              |
|   | <b>Typ.</b> | <b>Typ.</b> | <b>Typ.</b> |      | <b>Units</b> |
| Input Frequency   | 100         | 500         | 900         |      | MHz          |
| ±3 dB Dynamic Range   | 61          | 61          | 62          |      | dB           |
| DETOUT Slope  | 17.2        | 17.2        | 17.1        |      | mV/dB        |
| DETOUT Intercept  | -68.1       | -68.6       | -68.9       |      | dBm          |
| Variation of DETOUT with<br>Temperature from -40°C to +85°C @20dBm Input                    | -1.3        | -1.2        | -1.2        |      | dB           |

[1] Unless otherwise noted, test conditions: ATTN1 + ATTN2 + AMP1 + AMP2 in cascade.

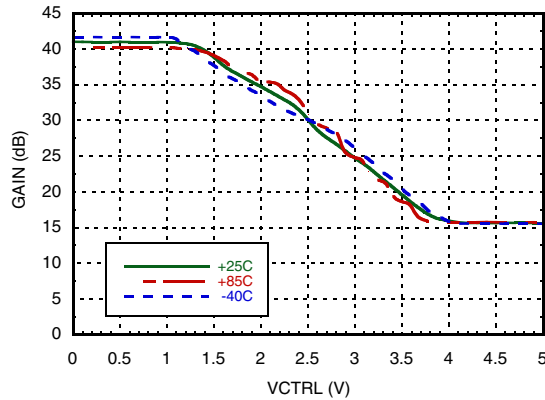
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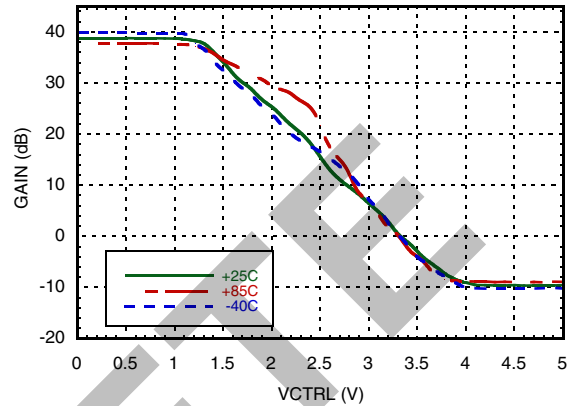
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AUTOMATIC GAIN CONTROL - SMT

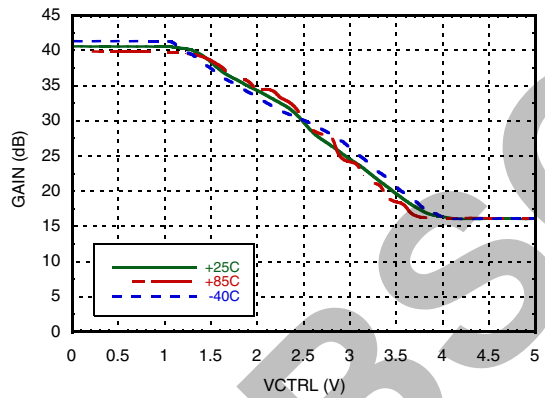
**Gain vs. VCTRL @ 100MHz<sup>[1]</sup>**



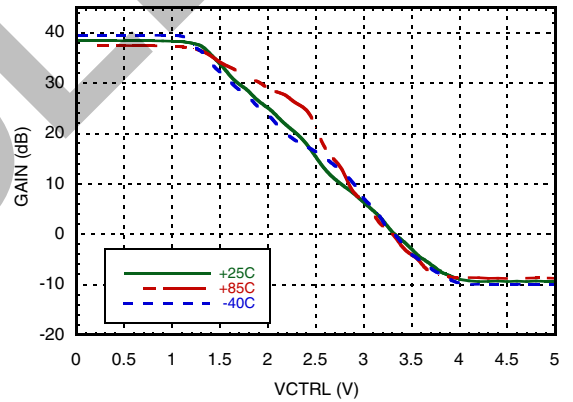
**Gain vs. VCTRL @ 100MHz<sup>[2]</sup>**



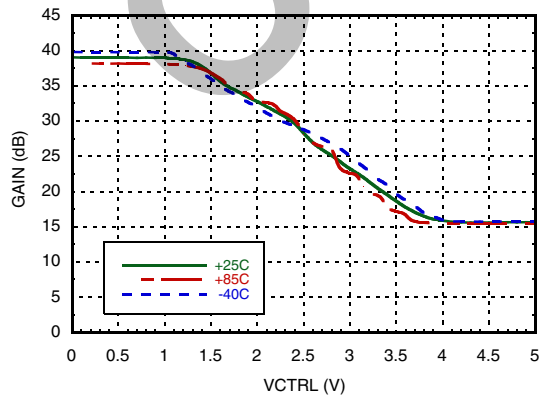
**Gain vs. VCTRL @ 300MHz<sup>[1]</sup>**



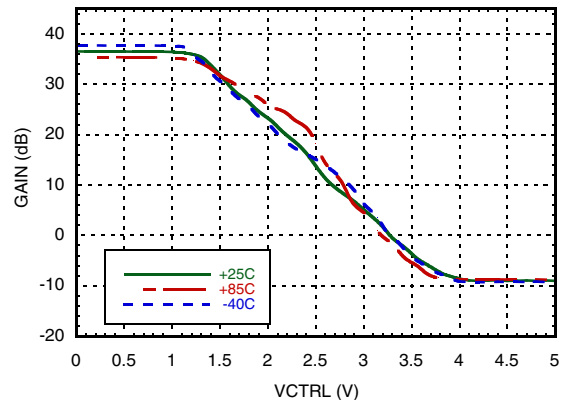
**Gain vs. VCTRL @ 300MHz<sup>[2]</sup>**



**Gain vs. VCTRL @ 500MHz<sup>[1]</sup>**



**Gain vs. VCTRL @ 500MHz<sup>[2]</sup>**



[1] ATTN1 + AMP1 + AMP2, CT1=0V

[2] ATTN1 + ATTN2 + AMP1 + AMP2, CT1=0V

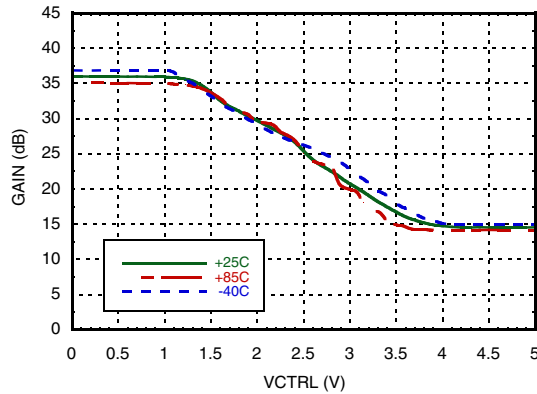
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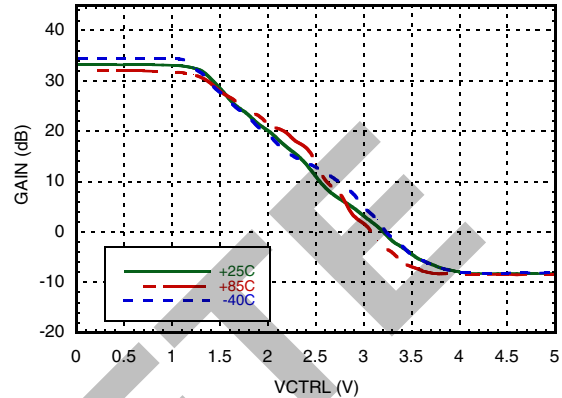


**IF AUTOMATIC GAIN CONTROLLER (IF-AGC), 50 - 800 MHz**

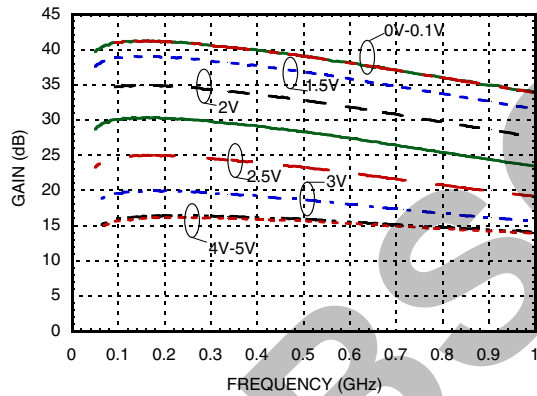
**Gain vs. VCTRL @ 800MHz<sup>[1]</sup>**



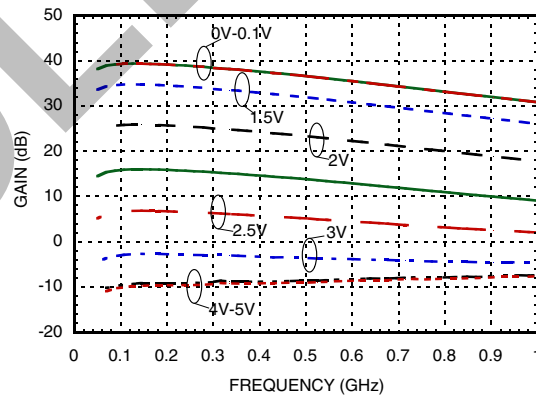
**Gain vs. VCTRL @ 800MHz<sup>[2]</sup>**



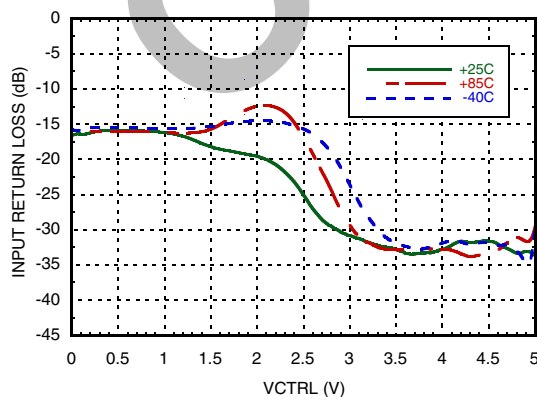
**Gain vs. Frequency over VCTRL<sup>[1][3]</sup>**



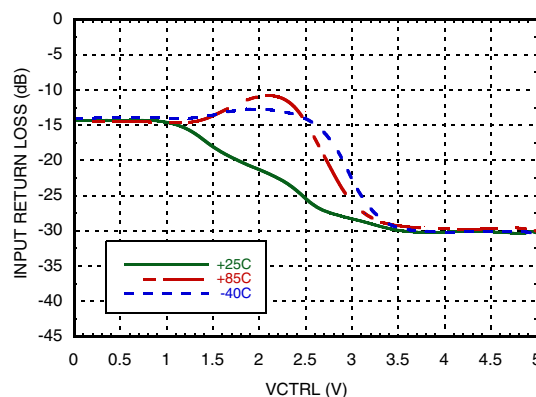
**Gain vs. Frequency over VCTRL<sup>[2][3]</sup>**



**Input Return Loss vs. VCTRL @ 100MHz<sup>[1]</sup>**



**Input Return Loss vs. VCTRL @ 100MHz<sup>[2]</sup>**



[1] ATTN1 + AMP1 + AMP2, CT1=0V

[2] ATTN1 + ATTN2 + AMP1 + AMP2, CT1=0V

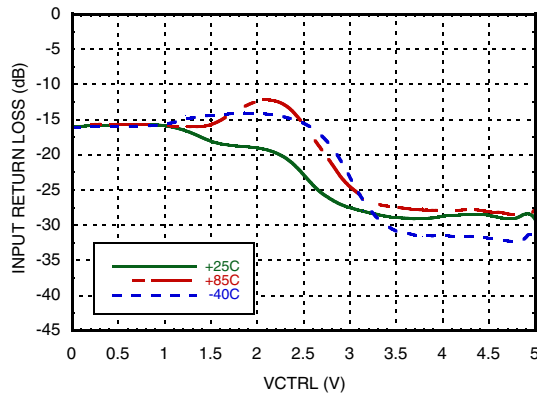
[3] At 25°C



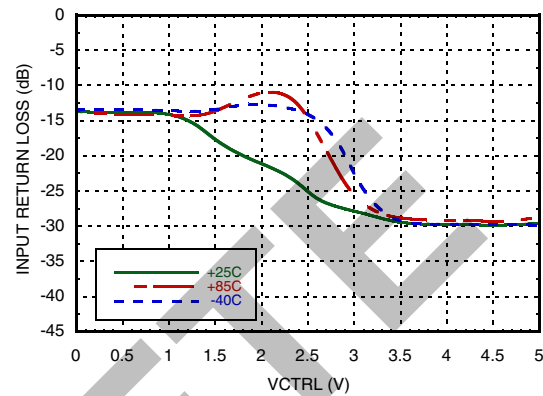
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AUTOMATIC GAIN CONTROL - SMT

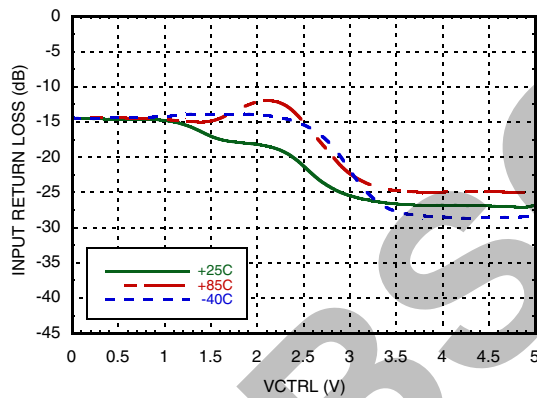
**Input Return Loss vs. VCTRL @ 300MHz<sup>[1]</sup>**



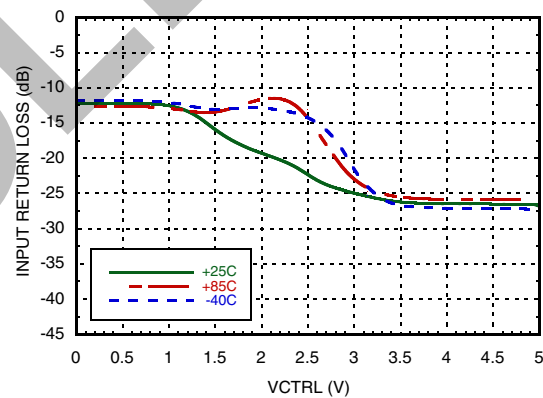
**Input Return Loss vs. VCTRL @ 300MHz<sup>[2]</sup>**



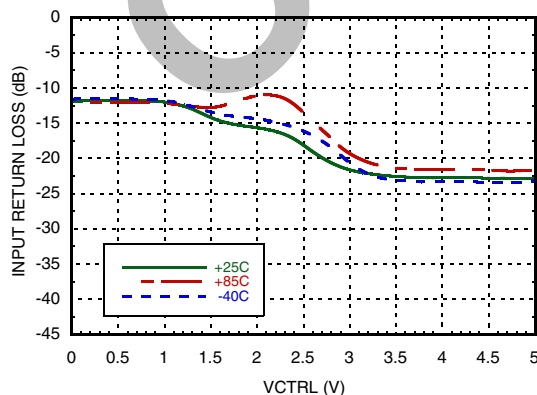
**Input Return Loss vs. VCTRL @ 500MHz<sup>[1]</sup>**



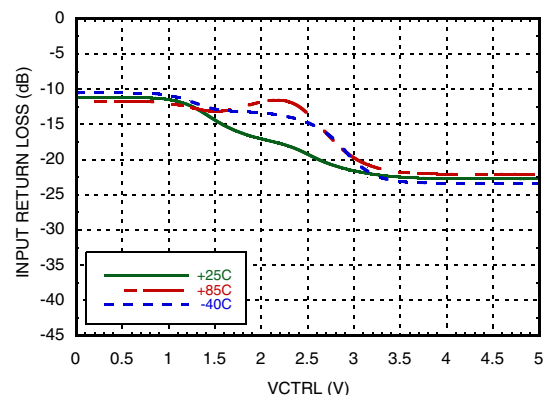
**Input Return Loss vs. VCTRL @ 500MHz<sup>[2]</sup>**



**Input Return Loss vs. VCTRL @ 800MHz<sup>[1]</sup>**



**Input Return Loss vs. VCTRL @ 800MHz<sup>[2]</sup>**



[1] ATTN1 + AMP1 + AMP2, CT1=0V

[2] ATTN1 + ATTN2 + AMP1 + AMP2, CT1=0V

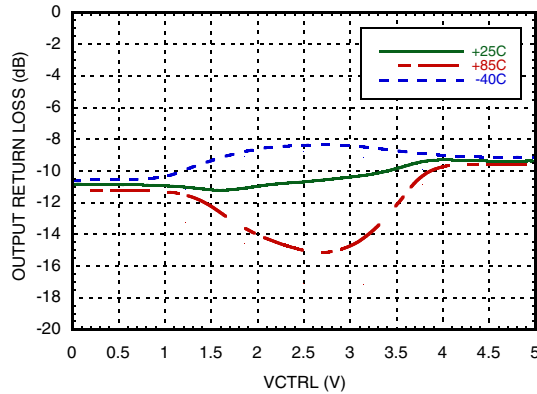
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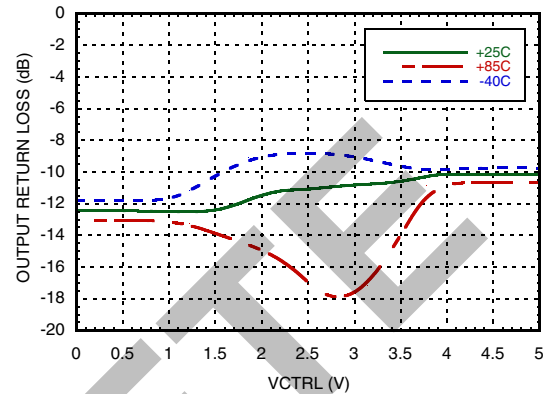


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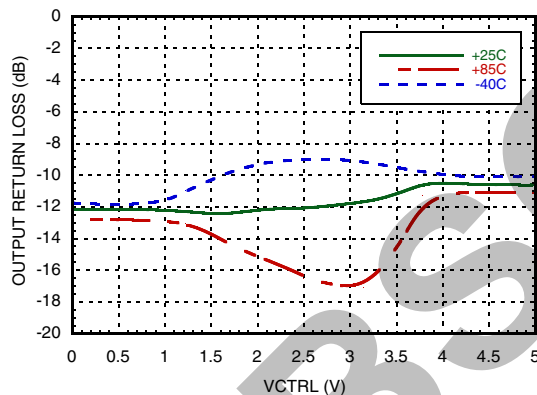
**Output Return Loss vs. VCTRL @ 100MHz<sup>[1]</sup>**



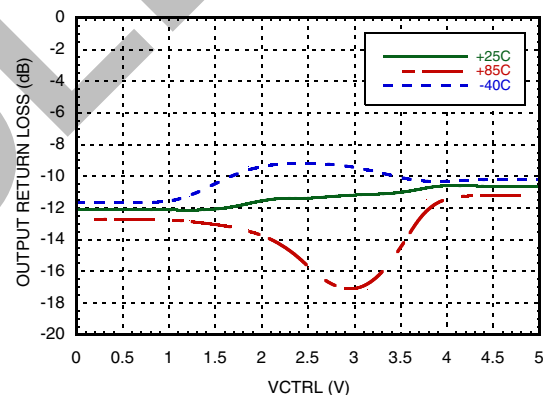
**Output Return Loss vs. VCTRL @ 100MHz<sup>[2]</sup>**



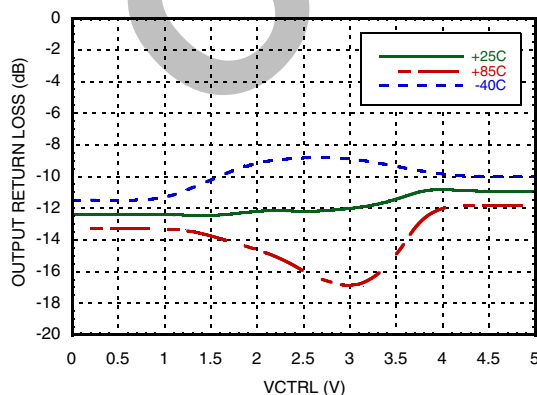
**Output Return Loss vs. VCTRL @ 300MHz<sup>[1]</sup>**



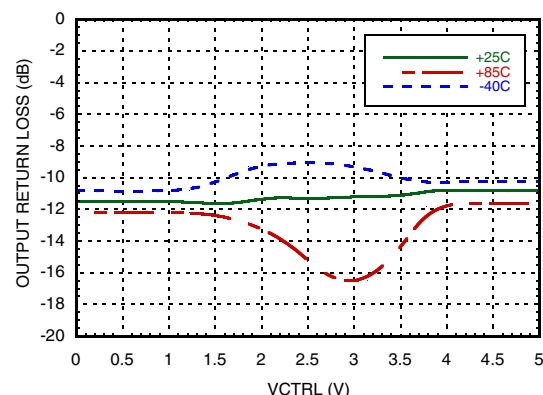
**Output Return Loss vs. VCTRL @ 300MHz<sup>[2]</sup>**



**Output Return Loss vs. VCTRL @ 500MHz<sup>[1]</sup>**



**Output Return Loss vs. VCTRL @ 500MHz<sup>[2]</sup>**



[1] ATTN1 + AMP1 + AMP2, CT1=0V

[2] ATTN1 + ATTN2 + AMP1 + AMP2, CT1=0V

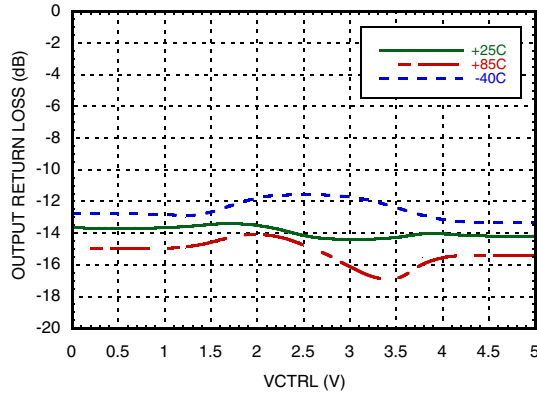
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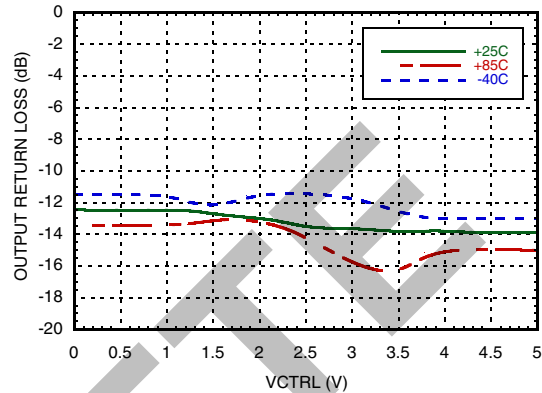


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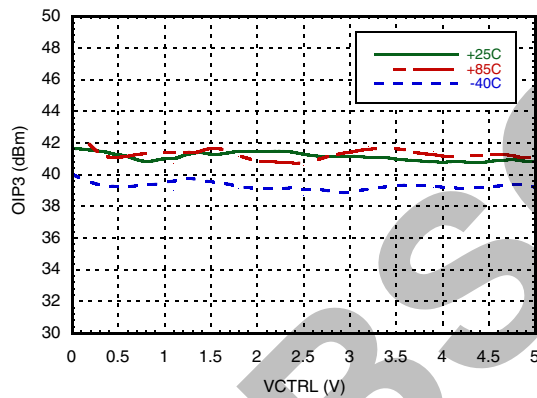
**Output Return Loss vs. VCTRL  
@ 800MHz<sup>[1]</sup>**



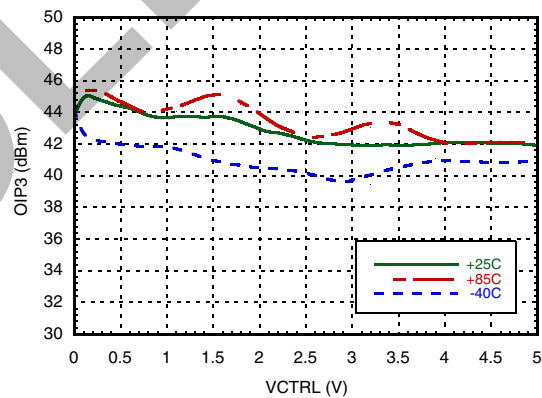
**Output Return Loss vs. VCTRL  
@ 800MHz<sup>[2]</sup>**



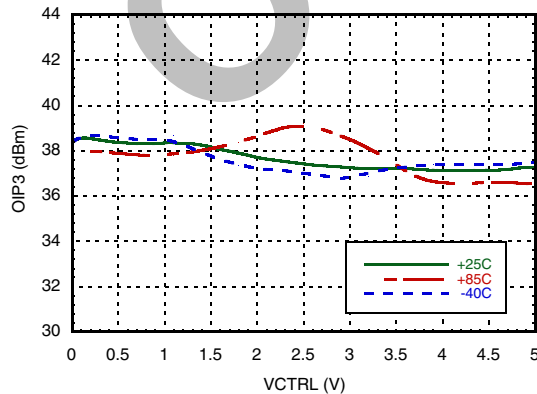
**Output IP3 vs. VCTRL @ 100MHz<sup>[1]</sup>**



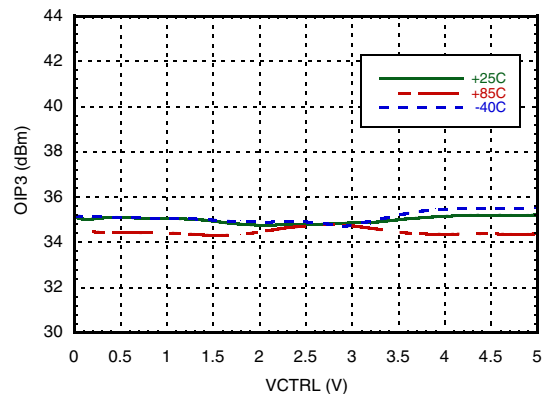
**Output IP3 vs. VCTRL @ 300MHz<sup>[1]</sup>**



**Output IP3 vs. VCTRL @ 500MHz<sup>[1]</sup>**



**Output IP3 vs. VCTRL @ 800MHz<sup>[1]</sup>**



[1] ATTN1 + AMP1 + AMP2, CT1=0V

[2] ATTN1 + ATTN2 + AMP1 + AMP2, CT1=0V

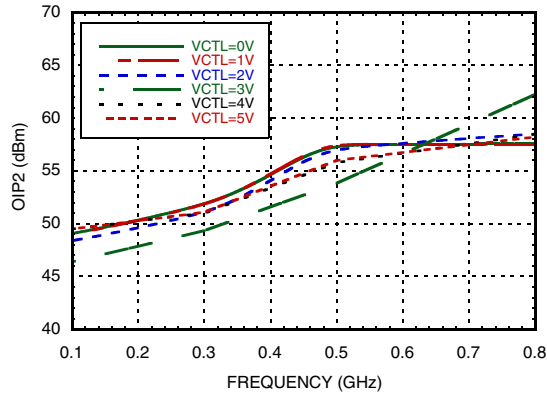
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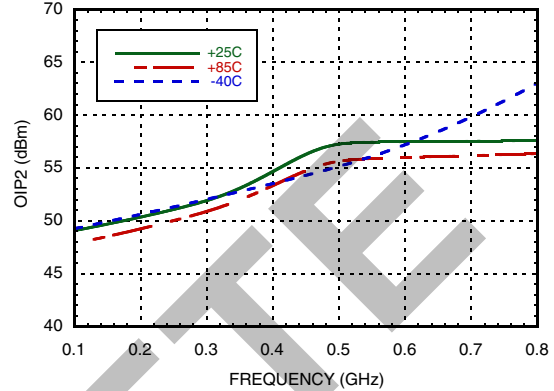


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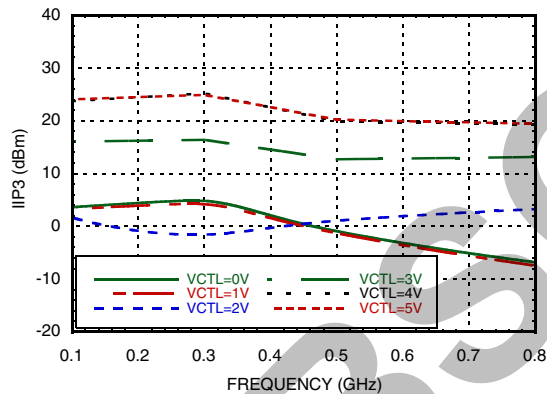
**Output IP2 vs. Frequency over VCTRL [1] [2]**



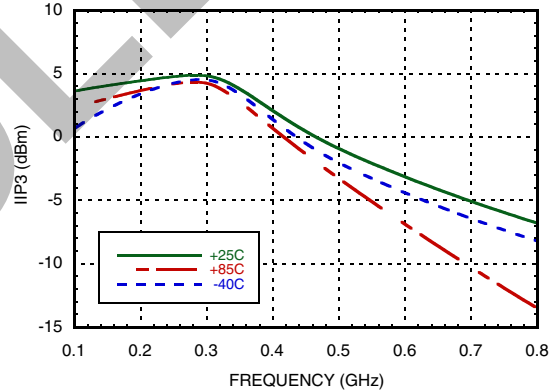
**Output IP2 vs. Frequency over Temperature [1] [3]**



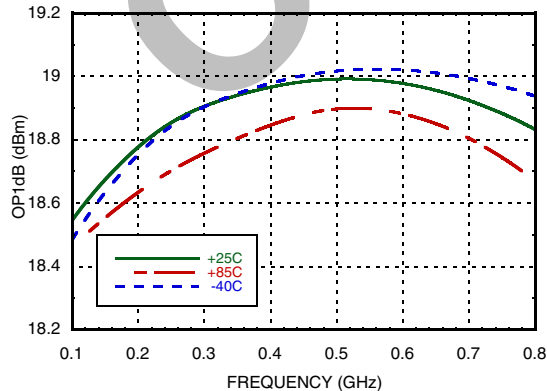
**Input IP3 vs. Frequency over VCTRL [1][2][5]**



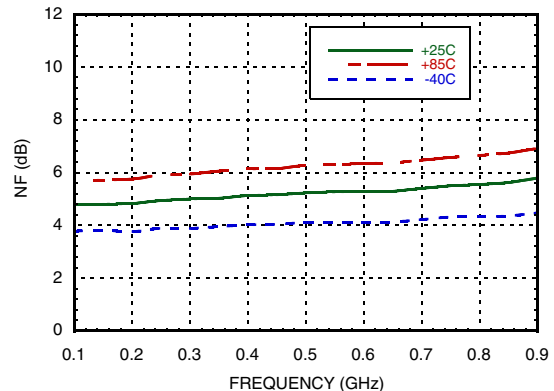
**Input IP3 vs. Frequency over Temperature [1][3][5]**



**Output P1dB vs. Frequency over Temperature [1] [4]**



**Noise Figure vs. Frequency over Temperature [1] [3]**



[1] ATTN1 + AMP1 + AMP2      [2] At 25°C  
 [3] VCTRL= 0V                      [4] VCTRL= 4V  
 [5] CT1=0V





## IF AUTOMATIC GAIN CONTROLLER (IF-AGC), 50 - 800 MHz

### Absolute Maximum Ratings

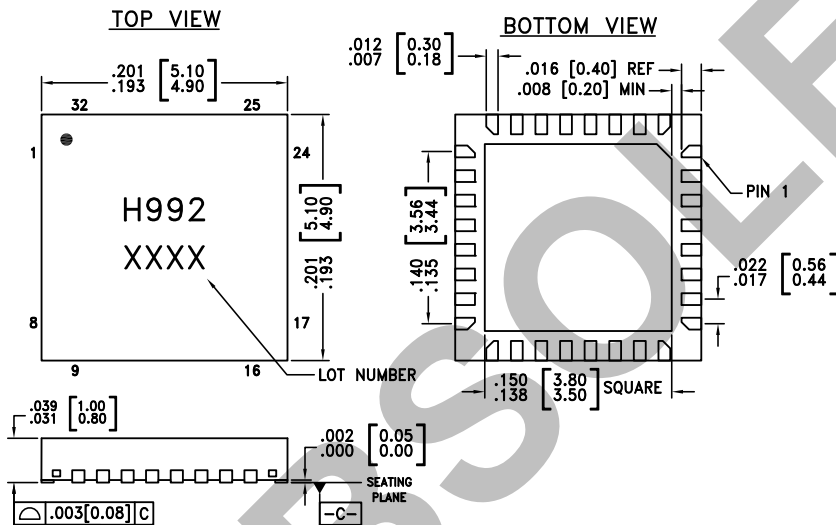
|   |                   |
|---|-------------------|
| VDD, DETVDD, DETEN, DETSET, DETRSSI, AMP1OUT, AMP2OUT | +5.6 V            |
| VCTRL   | -0.6V to VDD+0.6V |
| ATTN1IN, ATTN2IN Input Power                          | +20 dBm           |
| AMP1IN RF Input Power                                 | +10 dBm           |
| AMP2IN RF Input Power                                 | +15 dBm           |
| DETOUR Output Current                                 | 5 mA              |
| DETIN RF Input Power                                  | 12 dBm            |
| Junction Temperature                                  | 125°C             |

|  |                |
|--|----------------|
| Continuous P <sub>diss</sub> (T=85 °C)<br>Derate 78.88 mW/°C above 85 °C | 3.16 W         |
| Thermal Resistance (R <sub>th</sub> )<br>(junction to package bottom)    | 12.68°C/W      |
| Storage Temperature  | -65 to +150 °C |
| Operating Temperature  | -40 to +85 °C  |
| ESD Sensitivity (HBM)  | Class 1B       |



ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS

### Outline Drawing



NOTES:

- PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
- LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
- LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
- DIMENSIONS ARE IN INCHES [MILLIMETERS].
- LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
- CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
- PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
- PACKAGE WARP SHALL NOT EXCEED 0.05mm
- ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
- REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

### Package Information

| Part Number | Package Body Material                              | Lead Finish   | MSL Rating          | Package Marking <sup>[1]</sup> |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC992LP5E  | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 <sup>[2]</sup> | H992<br>XXXX                   |

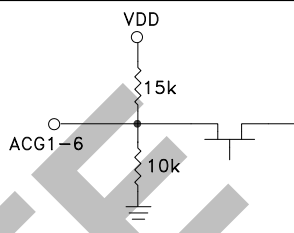
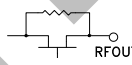
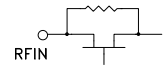
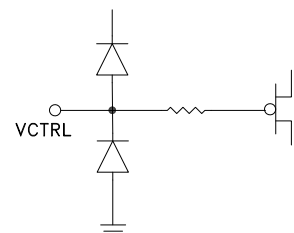
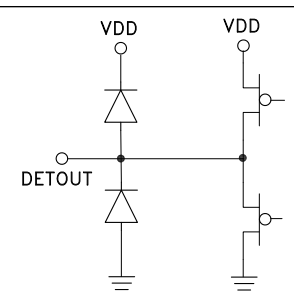
[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C

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**IF AUTOMATIC GAIN CONTROLLER  
(IF-AGC), 50 - 800 MHz**
**Pin Descriptions**

| Pin Number        | Function                                 | Description  | Interface Schematic   |
|-------------------|--|--|---|
| 1, 3, 5-6, 28, 30 | ACG1, ACG4,<br>ACG5, ACG6,<br>ACG3, ACG2 | AC ground capacitance connection pin.  |    |
| 2, 29             | ATTN2OUT,<br>ATTN1OUT                    | These ports are matched to 50 Ohms.<br>Blocking capacitor is required.   |    |
| 4, 9, 31          | VDD                                      | Power supply for the attenuator. External by pass capacitors are required. See application circuit.                                    |   |
| 7, 32             | ATTN2IN,<br>ATTN1IN                      | These ports are matched to 50 Ohms.<br>Blocking capacitor is required.   |    |
| 8                 | VCTRL                                    | Attenuation control voltage for the attenuator.<br>0V for minimum attenuation, 5V for maximum attenuation.                             |  |
| 10, 11, 26        | N/C                                      | No connection required. These pins may be connected to RF ground without affecting performance.  |   |
| 12                | CT1                                      | Reserved pin and should be connected to ground.  |   |
| 13                | DETOUT                                   | Logarithmic output that converts the input power to a DC level in controller mode. Output voltage increases with increasing amplitude. |  |



**IF AUTOMATIC GAIN CONTROLLER  
(IF-AGC), 50 - 800 MHz**

**Pin Descriptions (continued)**

| Pin Number     | Function            | Description  | Interface Schematic |
|----------------|---------------------|--|---------------------|
| 14             | DETVD               | Power supply for the attenuator. External by pass capacitors are required. See application circuit.                                      |                     |
| 15, 17, 22, 24 | GND                 | These pins must be connected to RF ground.   |                     |
| 16             | DETIN               | Detector RF input pin.   |                     |
| 18             | DETEN               | Enable pin.<br>Apply $V_{EN} > 0.8 \times V_{CC}$ for normal operation.<br>Apply $V_{EN} < 0.2 \times V_{CC}$ to disable the detector.   |                     |
| 19             | DETSET              | Set point input for controller mode.<br>Connect to DETOUT with the resistor network shown in evaluation board drawing for detector mode. |                     |
| 20             | DETRSSI             | Connection for ground referenced external lowpass filter capacitor.  |                     |
| 21, 25         | AMP2OUT,<br>AMP1OUT | These ports are mated to 50 Ohms. External Choke inductor and DC blocking capacitor are required. See application circuit.               |                     |
| 23, 27         | AMP2IN,<br>AMP1IN   | These ports are matched to 50 Ohms. Blocking capacitor is required.  |                     |

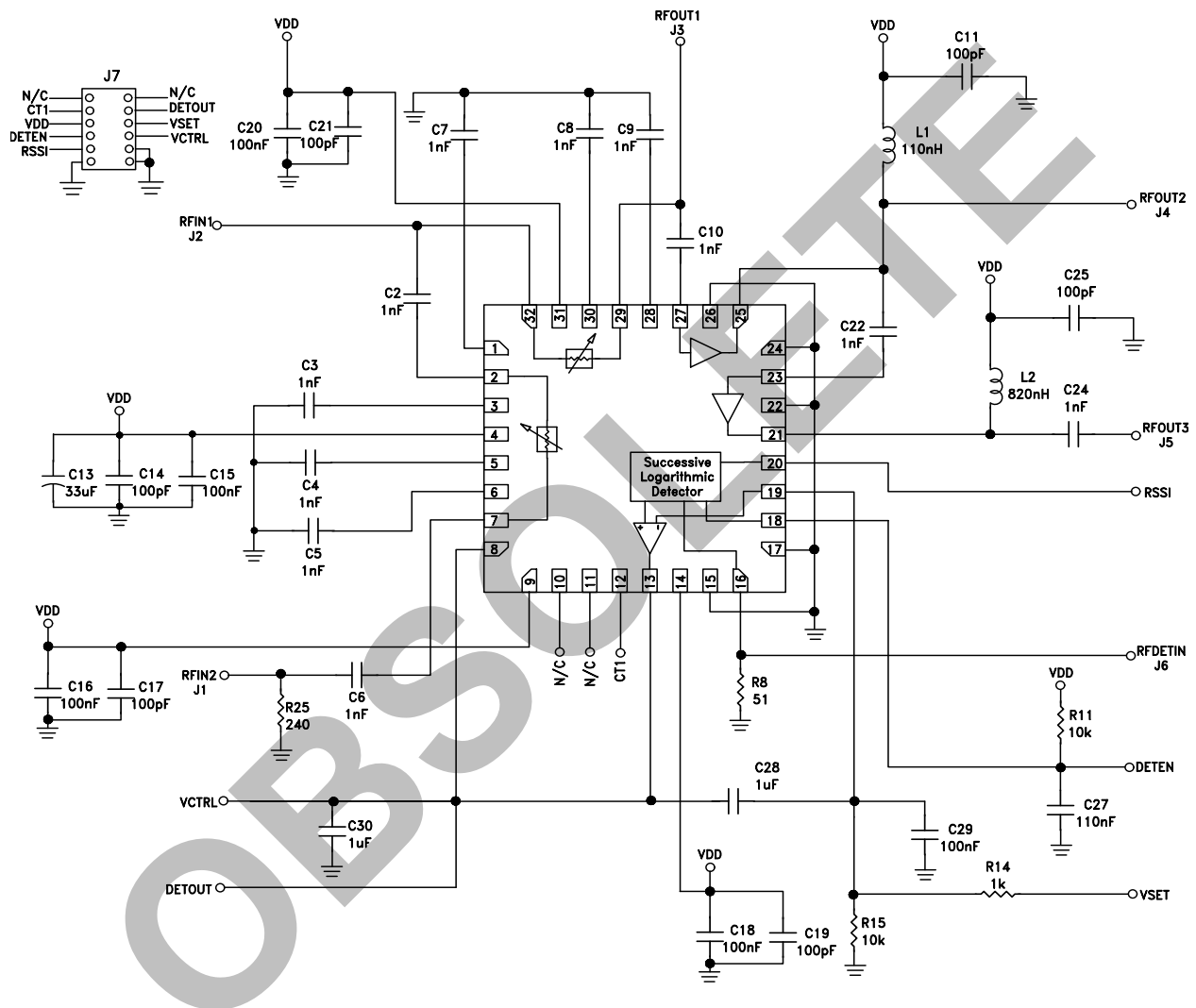
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**IF AUTOMATIC GAIN CONTROL (IF-AGC), 50 - 800 MHz**

**Application Circuit**



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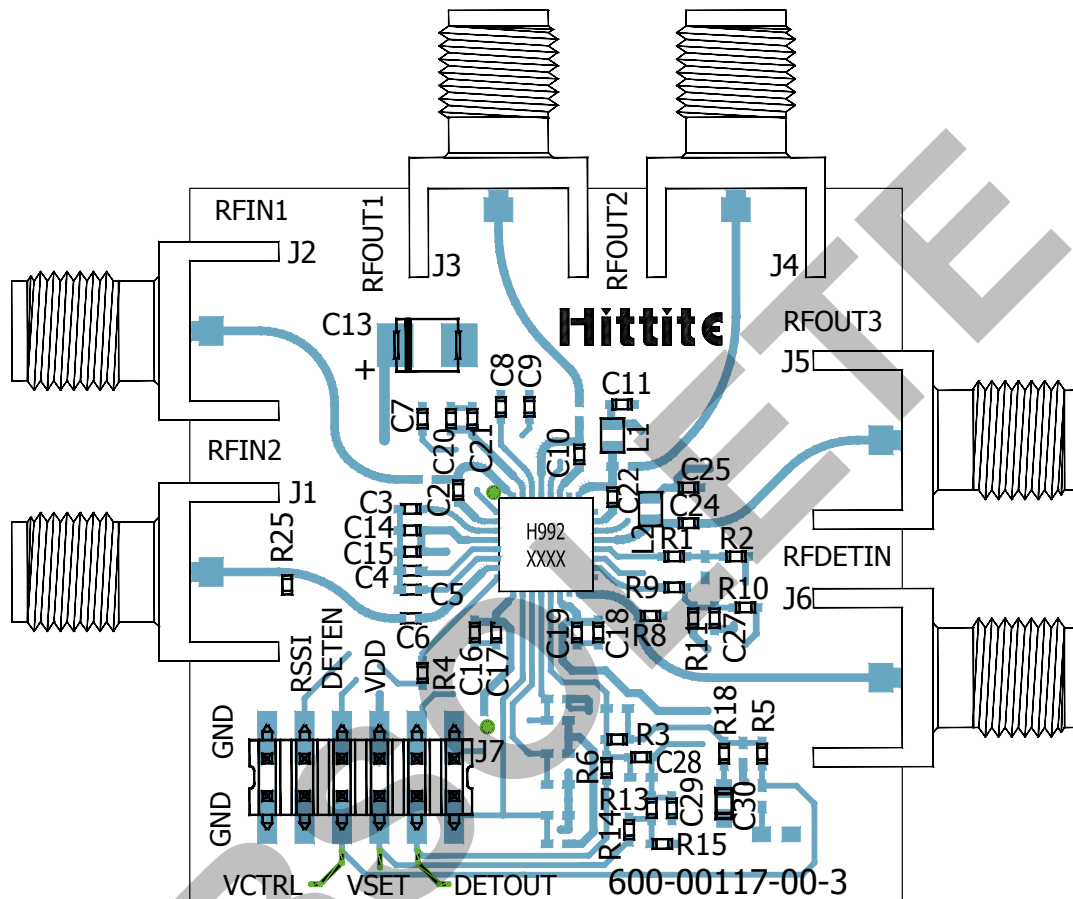
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**IF AUTOMATIC GAIN CONTROLLER (IF-AGC), 50 - 800 MHz**

**Evaluation PCB**

AUTOMATIC GAIN CONTROL - SMT



**List of Materials for Evaluation PCB EVAL01-HMC992LP5E<sup>[1]</sup>**

| Item                         | Description                  |
|------------------------------|------------------------------|
| J1-J6                        | SMA Connector                |
| J7                           | DC Connector Header          |
| C2-C10, C22, C24             | 1 nF Capacitor, 0402 Pkg.    |
| C11, C14, C17, C19, C21, C25 | 100 pF Capacitor, 0402 Pkg.  |
| C13                          | 33 μF Capacitor, Tantalum    |
| C15-C16, C18, C20, C27, C29  | 0.1 μF Capacitor, 0402 Pkg.  |
| C30                          | 1 μF Capacitor, 0603 Pkg.    |
| L1                           | 110 nH Inductor, 0603 Pkg.   |
| L2                           | 820 nH Inductor, 0603 Pkg.   |
| R1-R6, R9-R10, R13, R18      | 0 Ohm Resistor, 0402 Pkg.    |
| R8                           | 51 Ohms Resistor, 0402 Pkg.  |
| R11, R15                     | 10 kOhms Resistor, 0402 Pkg. |
| R14                          | 1 kOhms Resistor, 0402 Pkg.  |
| R25                          | 240 Ohms Resistor, 0402 Pkg. |

| Item    | Description                                |
|---------|--|
| U1      | HMC992LP5E<br>IF-Automatic Gain Controller |
| PCB [2] | 600-00117-00 Evaluation PCB                |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25 FR

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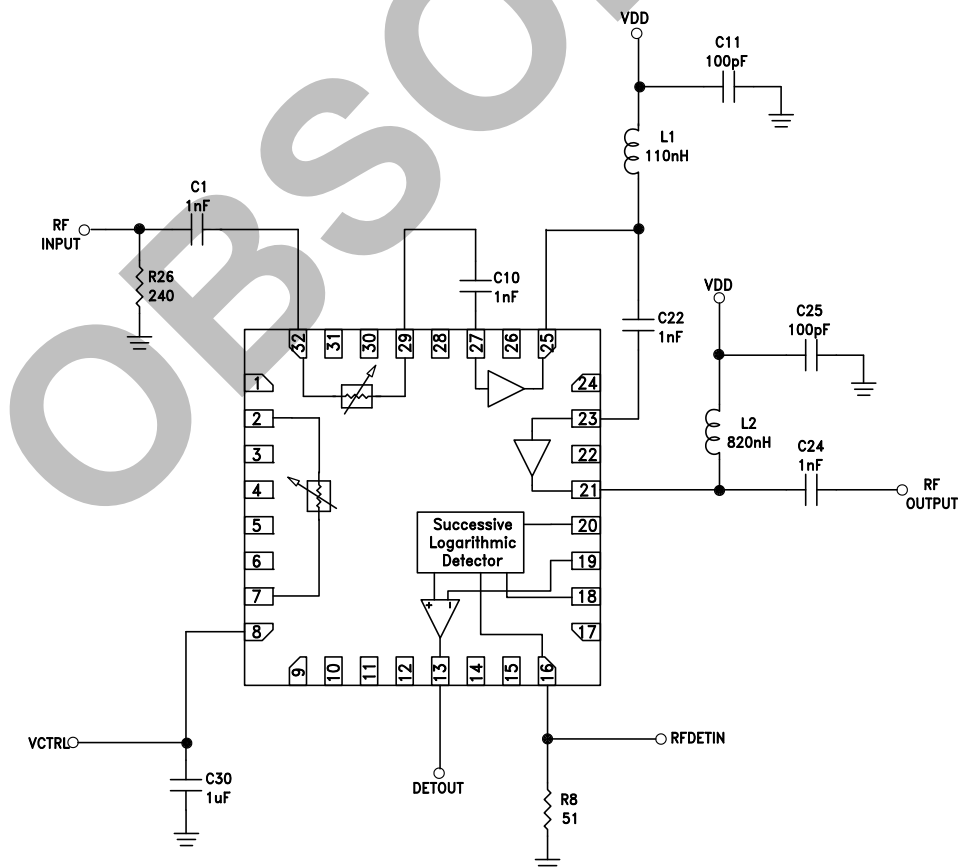
**Application Information**

**Introduction**

The HMC992LP5E is a complete high performance Automatic Gain Control (AGC) solution, housing a Variable Gain Amplifier (VGA) core and a control core in a single package. Its unique VVA technology provides constant OIP3 over the entire control voltage range. The HMC992LP5E greatly simplifies the design of gain control loops by increasing the integration level and reducing the number of required circuit elements. The VGA core of the HMC992LP5E is composed of two identical voltage variable attenuators followed by two gain block amplifiers which operate from 10 to 800 MHz. The HMC992LP5E's control core features a high accuracy log detector. As shown in the functional block diagram, the HMC992LP5E combines all of these cores in a highly compact 5 x 5 mm plastic package, and offers an easy-to-use, temperature stable AGC solution.

The HMC992LP5E's VGA core has a flexible structure where a single attenuator (23dB) or two attenuators (46dB) can be used depending upon the dynamic range requirement. The HMC992LP5E is designed to operate in a 50 Ohms impedance system. Inputs and outputs of the HMC992LP5E's attenuators and amplifiers (ATTIN1, ATTOUT1, ATTIN2, ATTOUT2, AMPIN1, AMPOUT1, AMPIN2, AMPOUT2) are broadband matched to 50 Ohms single-ended and require only external DC blocking capacitors over the entire frequency band of operation. The input of the HMC992LP5E's built in log detector (RFDETIN) is also broadband matched to 50 Ohms with a single-ended input interface and does not require any matching components.

The HMC992LP5E requires a single 5V supply with adequate power supply decoupling as recommended in the application schematic.



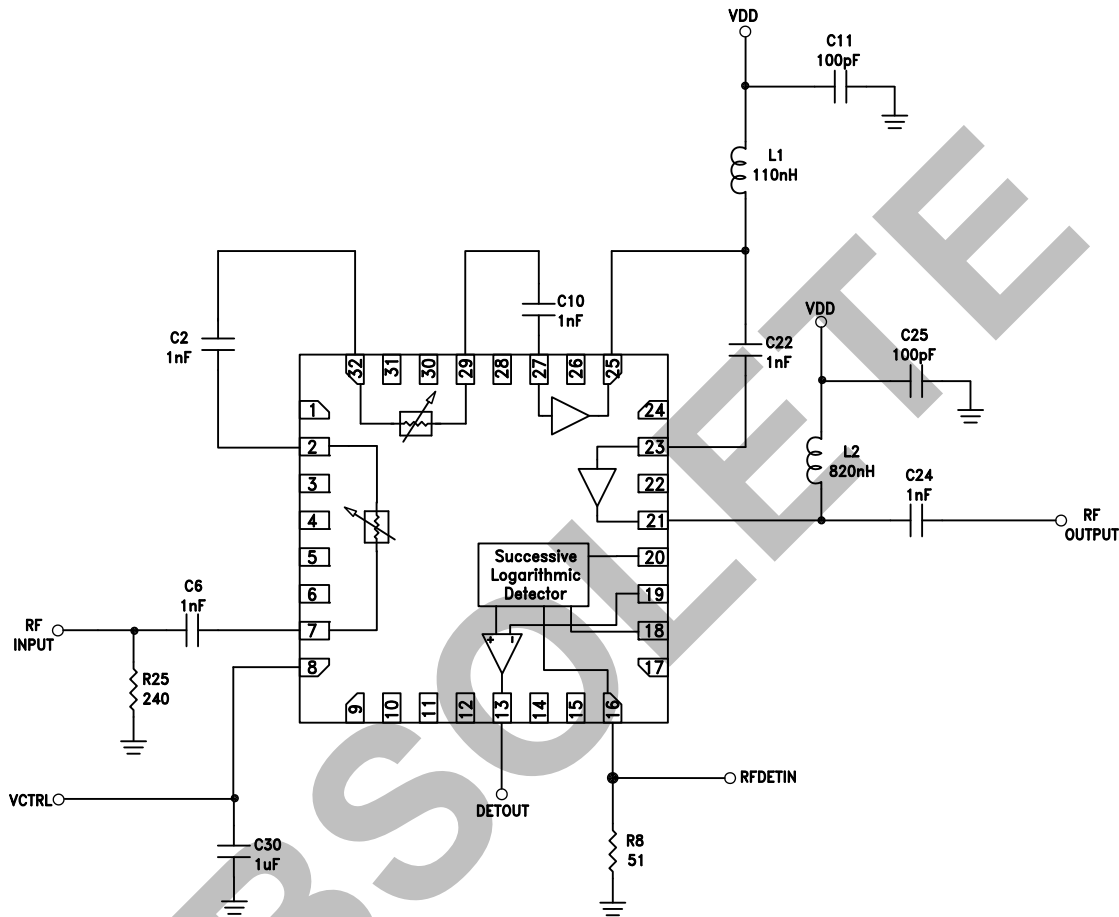
**Figure 1a:** The HMC992LP5E's VGA configuration with 1 attenuator.

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**Figure 1b:** The HMC992LP5E's VGA configuration with 2 attenuators.

**VGA Operation**

The HMC992LP5E's VGA core can be configured with one or two variable attenuators followed by two fixed gain amplifiers for different control ranges as shown in Figure 1a and Figure 1b (basic connections are not shown). The blocks require only external DC blocking capacitors at their inputs and outputs for interconnections. Note that the link between VCTRL and DETOUT pins must be broken for correct VGA Operation. The VCTRL pin should be used to set the attenuation of the HMC992LP5E.

**Gain Control Interface VCTRL**

The VCTRL pin is the gain control pin common to both of HMC992LP5E's identical voltage variable attenuators. The VCTRL gain control voltage ranges between 1V and 4V. A VCTRL control voltage of 1V provides the lowest attenuation, while 4V provides the highest attenuation.

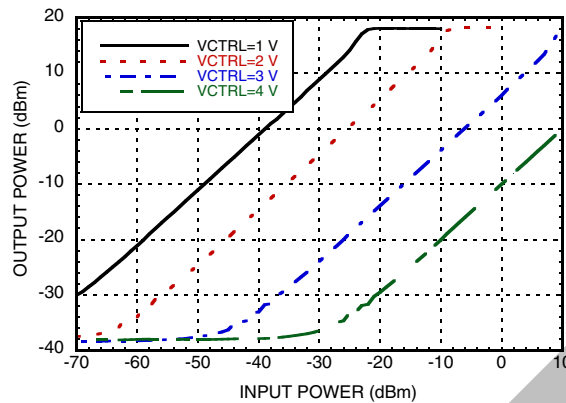
Figure 2 represents the VGA operation of HMC992LP5E with two attenuators and two amplifiers for different gain control voltages applied to the VCTRL pin. The output power increases linearly with the input power until the power saturation is reached when the VCTRL voltage is constant. The useable input power range of such a system is limited by the saturation level of the final stage amplifier. So the input power level required for power saturation and the dynamic range of the

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**Figure 2:** Pout vs. Pin at 100 MHz, 1 attenuator

HMC992LP5E's VGA is defined by the value of the gain control voltage applied to the VCTRL pin. Refer to the Figure 2 for the useable input power range at different VCTRL levels.

When VCTRL=1V, the gain of HMC992LP5E's VGA with 2 attenuators is 39 dB at 100 MHz. The input power required for 1 dB compression point at the output is given by:  $P_{in1dB} = P_{out1dB} - \text{Gain (dB)} = 18 - 39 = -21$  dB.

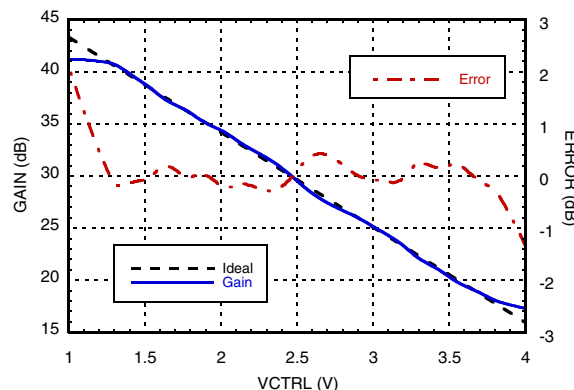
When VCTRL=2V, the gain of the HMC992LP5E's VGA with 2 attenuators is 25 dB at 100 MHz. The input power required for 1 dB compression point at the output is given by:  $P_{in1dB} = P_{out1dB} - \text{Gain (dB)} = 18 - 25 = -7$  dB.

Therefore, increasing the VCTRL pin voltage reduces the gain of the HMC992LP5E's VGA and increases input power level required for power saturation. When the input signal is weak, the attenuation level of the variable attenuators should be reduced. When the input signal is large; the attenuation level of the variable attenuators should be increased to achieve a constant output level.

The gain control performance of the HMC992LP5E at 300 MHz is shown in Figures 3a and 3b. The HMC992LP5E provides 24 dB of gain control range with a maximum gain of 41.2 dB when it is configured in 1 attenuator + 2 amplifiers mode, and similarly a 48 dB of gain control range with a maximum gain of 39 dB of gain when it is configured in 2 attenuators + 2 amplifiers mode. The HMC992LP5E's VGA has a very flat linear-in-dB gain control characteristic with a slope of -18.2 dB/V for the 2 attenuator configuration and -9.1 dB/V for the 1 attenuator configuration. The log-linearity error of the HMC992LP5 VGA is typically less than  $\pm 1$  dB over the entire gain control range as shown in Figure 3a and Figure 3b. The relation between the gain of HMC992LP5E's VGA and VCTRL pin voltage can be approximated as given in Equation (1).

Gain (dB) = 52.5 – 9.1 x VCTRL with one attenuator Equation (1a)

Gain (dB) = 61.0 – 18.2 x VCTRL with two attenuators Equation (1b)



**Figure 3a:** Gain & Gain Conformance Error vs. VCTRL at 300 MHz, 1 attenuator + 2 amplifiers configuration.

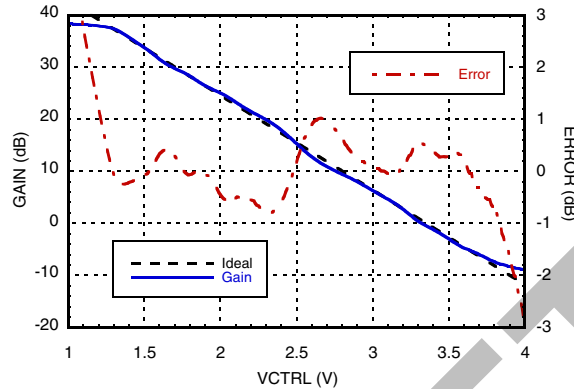
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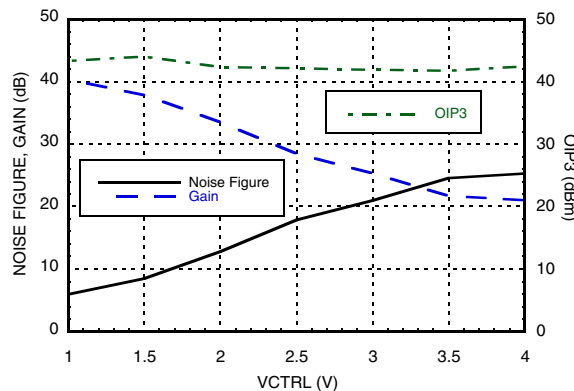
**Figure 3b:** Gain & Gain Conformance Error vs. VCTRL at 300 MHz, 2 attenuators + 2 amplifiers configuration.

**Noise and Distortion**

As with any multistage VGA consisting of voltage variable attenuators and gain blocks, the noise figure (NF) and input referred distortion (IIP3) characteristics of the HMC992LP5E's VGA are dependent on the gain control voltage VCTRL. When the attenuation level of the variable attenuators is set to minimum (maximum gain state), the noise figure of the HMC992LP5E's VGA is minimized; however the IIP3 is degraded to minimum as well. The noise figure and IIP3 of the HMC992LP5E's VGA increases with the attenuation level of the variable attenuators.

For low attenuation levels, the noise contribution from the VGA is important since the input signal is weak. For high attenuation levels of the variable attenuators, the noise contribution from the VGA is less important and the noise requirement of the VGA is relaxed since the input signal is high. The noise figure performance of the HMC992LP5E's VGA at 300 MHz is shown in Figure 4. The HMC992LP5E's VGA delivers a noise figure of 6 dB in its maximum gain state when it is configured in 1 attenuator + 2 amplifiers mode.

For low attenuation levels of the variable attenuators, IIP3 is less important since high gain of whole VGA improves distortion performance at its output (OIP3). For high attenuation levels of the variable attenuators, IIP3 is more important because of low gain of whole VGA. The distortion performance of the HMC992LP5E's VGA at 300 MHz is shown in Figure 4. The HMC992LP5E's VGA provides an almost constant OIP3 of up to +44 dBm in any state when it is configured in one attenuator and two amplifiers mode.



**Figure 4:** Noise Figure & Gain & OIP3 vs. VCTRL at 300 MHz, 1 attenuator.





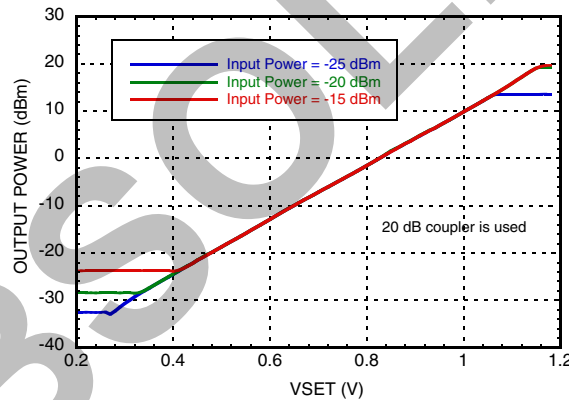
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**AGC Set point Interface VSET**

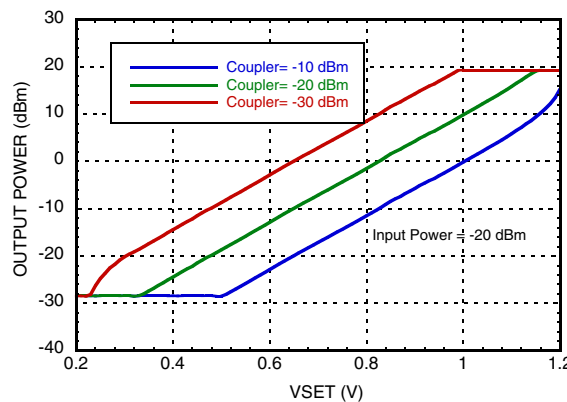
In closed loop AGC operation the output power level of the HMC992LP5E is controlled by the VSET pin. An input voltage between 0.2V and 1.2V should be applied to the VSET input pin to control the output power level. The VSET vs. the output power characteristic is shown in Figure 6a and Figure 6b for different input power levels and different coupler ratios used. The slope of the gain vs. VSET characteristic is 57dB/V and it is independent of the coupler ratio used.

In closed loop operation the HMC992LP5E is able to automatically adjust the RF gain over a gain adjustment range of up to 46 dB at 100 MHz. The HMC992LP5E's output dynamic range is a function of both input power level and the coupler ratio used to close the AGC loop. The combined effect of the input power and coupler ratio on the output power dynamic range is presented in Figures 6a and 6b.

For high input power levels, the maximum level of output dynamic range is limited by the Psat of the VGA or the highest detectable power level by the log detector. To eliminate any limitations that can arise due to highest detectable log detector, a high enough coupler ratio should be chosen to translate the maximum VGA output power level to a value lower than the highest detectable log detector power level.



**Figure 6a:** Output Power vs. VSET over Input Power, 2 attenuators @ 300 MHz.



**Figure 6b:** Output Power vs. VSET over coupler ratio, 2 attenuators @ 300 MHz.

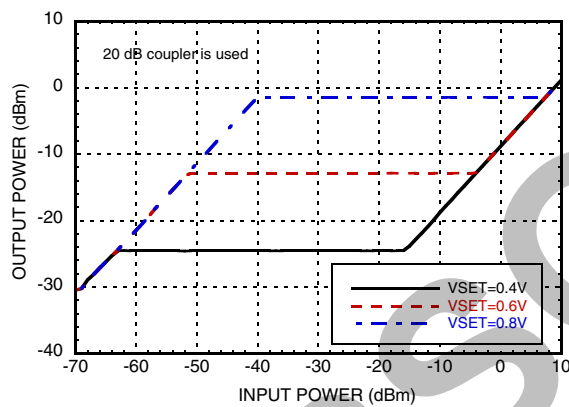


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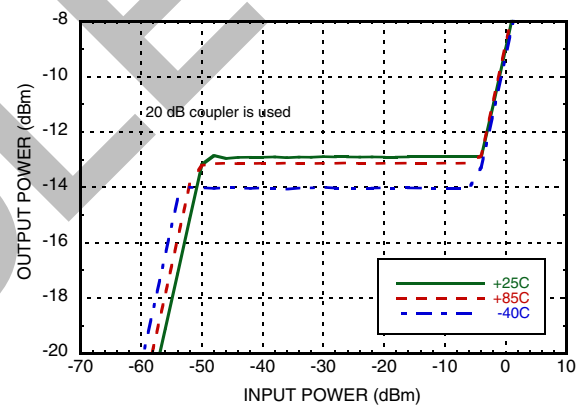
Similarly, the lower side of the dynamic range is limited by the noise floor of the VGA or the lowest power level detectable by the log detector. To eliminate any limitations on the lower side of the dynamic range, the coupler ratio should be low enough to translate the minimum VGA output power level to a value higher than the lowest detectable log detector power level.

Please also refer to the Log Detector section for more information.

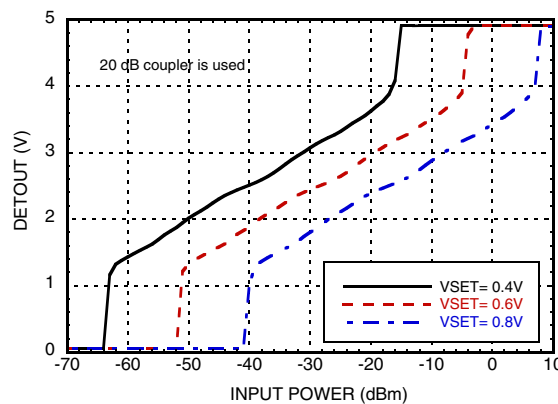
Figure 7a shows the output power vs. input power transfer characteristic of the HMC992LP5E over different VSET voltages for a closed AGC loop configuration. For low and high input power levels the HMC992LP5E attenuation range is saturated and the output is a linear function of the input. For input power levels within the dynamic range, the HMC992LP5E automatically adjusts the attenuation level as shown in Figure 7c to maintain a constant output power level. When Vset=0.6 V, the output power level is set to -13 dBm and the HMC992LP5E's AGC amplifier provides a gain control range of 46 dB from -51 dBm to -5 dBm with an excellent ripple within 0.06 dB.



**Figure 7a:** Output Power vs. input power over VSET, 2 attenuators @ 300 MHz.



**Figure 7b:** Output Power vs. input power, 2 attenuators @ 400 MHz & VSET=0.6V



**Figure 7c:** DETOUT vs. input power over VSET, 2 attenuators @ 300 MHz.



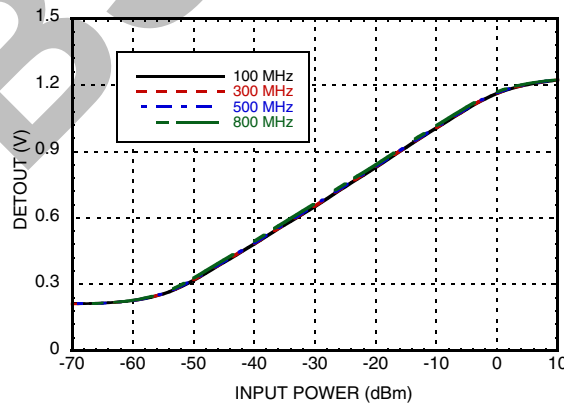
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(IF-AGC), 50 - 800 MHz**

**Log Detector**

The logarithmic detector of the HMC992LP5E converts the average envelope of RF input power to a proportional DC voltage at its output (DETOUT), as shown in Figure 8. In detection mode, the DETOUT pin should be connected to the VSET input. The HMC992LP5E's logarithmic detector employs a successive compression technology which delivers 50 dB of dynamic range ( $\pm 1$ dB) with high conversion accuracy over a wide input frequency range. Note that the link between DETOUT and VCTRL pins must be broken and DETOUT must be connected to VSET via 1k Ohms resistor for LOGAMP operation.

The HMC992LP5E's logarithmic detector can be used in the controller mode where an external voltage is applied to the VSET pin to create an AGC loop. The linear-in-dB behavior of the HMC992LP5E's VGA and logarithmic detector creates a linear AGC system. For linear operation, the signal fluctuations at the input of the log detector should remain within the dynamic range of the log detector. In closed loop AGC operation, the HMC992LP5E's response to large input level changes is not slew-rate limited, and the speed of the transient response can be adjusted through loop filter capacitors C28 and C30 (see Figure 5).

To achieve maximum gain adjustment range of the HMC992LP5E, the coupler ratio should be chosen based on the output power desired. A coupler ratio which translates the output power to the center (-25dBm) of the usable dynamic range of the log detector should be chosen. The gain adjustment range of the HMC992LP5E is maximized in this configuration. If the linear operation range of the HMC992LP5E is maximized by selecting the appropriate coupler ratio, the HMC992LP5E can handle larger changes in input level. For example, an input voltage of 0.6 V is applied to the Vset pin to set the constant output power level to -13 dBm. A coupler ratio of  $\sim 12$  dB can be chosen to provide a maximum dynamic range of 46 dBm.



**Figure 8:** DETOUT vs. input power over frequency.

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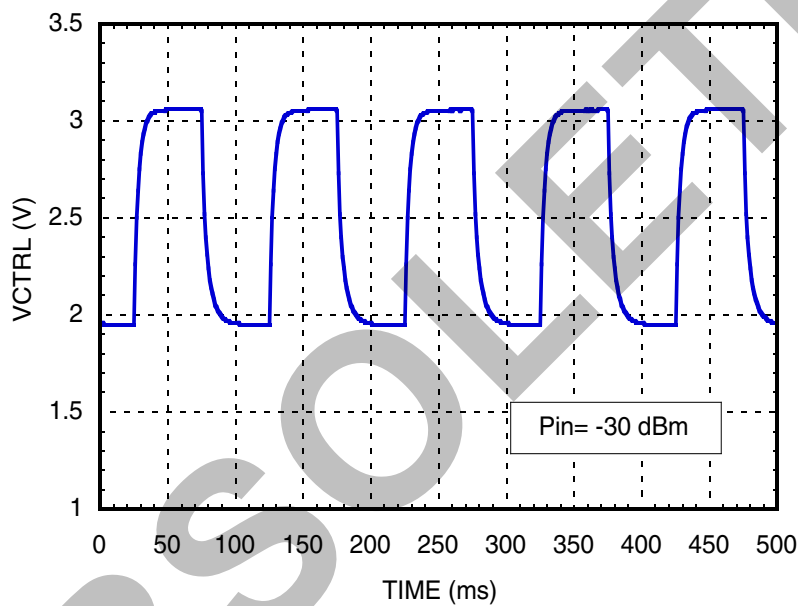
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**Loop Bandwidth and Response Time**

The AGC system has a response time to undesired input level fluctuations. Response time and the stability of the HMC992LP5E's AGC loop is determined by C28 and C30 in the application schematic. The HMC992LP5E's response to voltage changes in VSET with C28=C30=1μF when the input level is kept constant is shown in Figure 9.



**Figure 9:** HMC992LP5E's gain control voltage when VSET is toggled between 0.4V - 0.8V and input level is kept constant in closed loop.

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