

THC63LVDM87

LOW POWER / SMALL PACKAGE / 24Bit COLOR LVDS TRANSMITTER

General Description

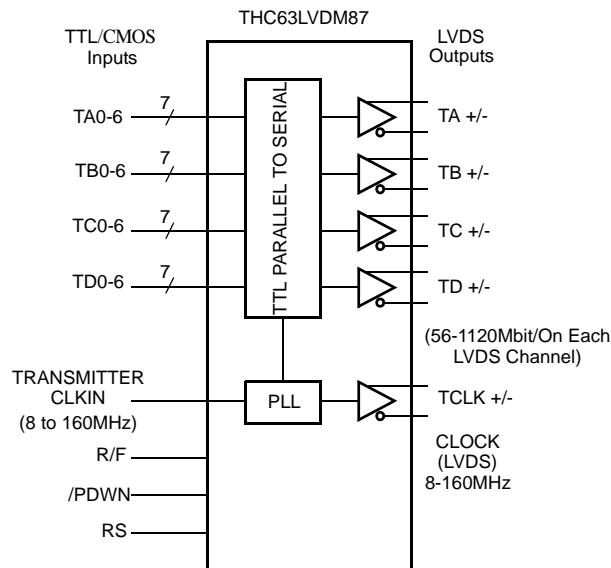
The THC63LVDM87 transmitter is designed to support pixel data transmission between Host and Flat Panel Display up to 1080p/WUXGA resolutions.

The THC63LVDM87 converts 28bits of CMOS/TTL data into LVDS(Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 160MHz, 24bits of RGB data and 4bits of timing and control data (HSYNC, VSYNC, DE, CONT1) are transmitted at an effective rate of 1120Mbps per LVDS channel.

Features

- Low power 1.8V CMOS design
- 5mm x 5mm/49pin/0.65mm pitch VFBGA Package applicable to non-HDI PCB
- Wide dot clock range, 8-160MHz suited for TV Signal: NTSC(12.27MHz) - 1080p(148.5MHz) PC Signal: QVGA(8MHz) - WUXGA(154MHz)
- Supports 1.8V single power supply
- 1.8V/2.5V/3.3V CMOS inputs are supported by setting IOVCC=1.8V/2.5V/3.3V
- LVDS swing is reducible by RS-pin to reduce EMI and power consumption
- PLL requires no external components
- Supports spread spectrum clock generator
- On chip jitter filtering
- Power down mode
- Input clock triggering edge is selectable by R/F-pin

Block Diagram



Pin Out

TOP VIEW

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |
|---|-----|-----|-----|------------|-------------|-------|-------|---|
| A | TA6 | TA5 | TA4 | TA3 | TA2 | TA1 | TA0 | A |
| B | TB4 | TD3 | TD2 | TD1 | TD0 | TA- | TA+ | B |
| C | TB5 | TB0 | GND | VCC | RS | TB- | TB+ | C |
| D | TB6 | TB1 | GND | IO VCC | LVDS VCC | TC- | TC+ | D |
| E | TC0 | TB2 | GND | PLL VCC | R/F | TCLK- | TCLK+ | E |
| F | TC1 | TB3 | TD4 | TD5 | TD6 | TD- | TD+ | F |
| G | TC2 | TC3 | TC4 | TC5 | TC6 | CLKIN | /PDWN | G |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |

Pin Description

| Pin Name | Pin # | Type | Description | | | | | | |
|--------------|---------------------------|----------|---|----|---------------------------|---|-------|---|-------|
| TA+, TA- | B7, B6 | LVDS OUT | LVDS Data Out. | | | | | | |
| TB+, TB- | C7, C6 | LVDS OUT | | | | | | | |
| TC+, TC- | D7, D6 | LVDS OUT | | | | | | | |
| TD+, TD- | F7, F6 | LVDS OUT | | | | | | | |
| TCLK+, TCLK- | E7, E6 | LVDS OUT | LVDS Clock Out. | | | | | | |
| TA0 ~ TA6 | A7,A6,A5,A4,A3,A2,A1 | IN | Pixel Data Inputs. | | | | | | |
| TB0 ~ TB6 | C2,D2,E2,F2,B1,C1,D1 | IN | | | | | | | |
| TC0 ~ TC6 | E1,F1,G1,G2,G3,G4,G5 | IN | | | | | | | |
| TD0 ~ TD6 | B5,B4,B3,B2,F3,F4,F5 | IN | | | | | | | |
| /PDWN | G7 | IN | H: Normal operation, L: Power down (All outputs are Hi-Z and all circuits are stand-by mode with minimum current(ITCCS)) | | | | | | |
| RS | C5 | IN | LVDS swing mode select. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>RS</th> <th>LVDS Swing(VOD, see Fig4)</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>350mV</td> </tr> <tr> <td>L</td> <td>200mV</td> </tr> </tbody> </table> | RS | LVDS Swing(VOD, see Fig4) | H | 350mV | L | 200mV |
| RS | LVDS Swing(VOD, see Fig4) | | | | | | | | |
| H | 350mV | | | | | | | | |
| L | 200mV | | | | | | | | |
| R/F | E5 | IN | Input Clock Triggering Edge Select. H: Rising edge, L: Falling edge | | | | | | |
| CLKIN | G6 | IN | Clock input. | | | | | | |
| IO VCC | D4 | Power | Power Supply Pin for IO Inputs. | | | | | | |
| VCC | C4 | Power | Power Supply Pin for digital circuitry. | | | | | | |
| LVDS VCC | D5 | Power | Power Supply Pin for LVDS Outputs. | | | | | | |
| PLL VCC | E4 | Power | Power Supply Pin for PLL circuitry. | | | | | | |
| GND | C3,D3,E3 | Ground | Ground Pins for Common. | | | | | | |

Absolute Maximum Ratings

| | |
|---|---------------------------|
| Supply Voltage (IO VCC) | -0.3V ~ +4.0V |
| Supply Voltage (VCC, PLL VCC, LVDS VCC) | -0.3V ~ +2.1V |
| CMOS/TTL Input Voltage | -0.3V ~ (IO VCC + 0.3V) |
| LVDS Transmitter Output Voltage | -0.3V ~ (LVDS VCC + 0.3V) |
| LVDS Total Output Current | -50mA ~ 50mA |
| Junction Temperature (Tj) | +125°C |
| Storage Temperature Range | -55°C ~ +125°C |
| Reflow Peak Temperature / Time | +260°C / 10sec. |
| Maximum Power Dissipation @+25°C | 1.3W |

Recommended Operating Conditions

| Parameter | | Min. | Typ | Max | Units |
|---|-------------|------|-------------|------|-------|
| Supply Voltage (IOVCC) | | 1.62 | 1.8/2.5/3.3 | 3.6 | V |
| Supply Voltage (PLL VCC / LVDS VCC / VCC) | | 1.62 | 1.8 | 1.98 | V |
| Operating Ambient Temperature (Ta) | | -40 | | 85 | °C |
| Clock Frequency | Input | 8 | | 160 | MHz |
| | LVDS Output | 8 | | 160 | MHz |

Electrical Characteristics

CMOS/TTL DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-------------------|--------------------------|----------------------------|------------|------|------------|-------|
| V _{IH18} | High Level Input Voltage | IOVCC=1.62~1.98V | 0.65 IOVCC | | IOVCC+0.3 | V |
| V _{IL18} | Low Level Input Voltage | | -0.3 | | 0.35 IOVCC | V |
| V _{IH25} | High Level Input Voltage | IOVCC=2.3~2.7V | 1.7 | | IOVCC+0.3 | V |
| V _{IL25} | Low Level Input Voltage | | -0.3 | | 0.7 | V |
| V _{IH33} | High Level Input Voltage | IOVCC=3.0~3.6V | 2.0 | | IOVCC+0.3 | V |
| V _{IL33} | Low Level Input Voltage | | -0.3 | | 0.8 | V |
| I _{INC} | Input Current | V _{IN} =GND~IOVCC | -10 | | 10 | μA |

LVDS Transmitter DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units | |
|-----------------|---|---|-----------------------|------|-------|-------|----|
| VOD | Differential Output Voltage | RL=100Ω | Normal swing RS=H | 250 | 350 | 450 | mV |
| | | | Reduced swing RS=L | 140 | 200 | 300 | mV |
| ΔVOD | Change in VOD between complementary output states | RL=100Ω | | | 35 | mV | |
| VOC | Common Mode Voltage | | 1.125 | 1.25 | 1.375 | V | |
| ΔVOC | Change in VOC between complementary output states | | | | 35 | mV | |
| I _{OS} | Output Short Circuit Current | V _{OUT} =GND, RL=100Ω | | | 100 | mA | |
| I _{OZ} | Output TRI-STATE Current | /PDWN=L, V _{OUT} =GND~LVDSVCC | -20 | | 20 | μA | |

Supply Current

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Condition(*) | | | Typ. | Max. | Units |
|-------------------|---------------------------------------|--------------------------------|----------------------------|----------|------|------|-------|
| I _{TCCW} | Transmitter Supply Current | RL=100Ω CL=5pF | RS=H Normal swing mode | f=37MHz | 25 | 33 | mA |
| | | | | f=71MHz | 30 | 46 | mA |
| | | | | f=160MHz | 44 | 79 | mA |
| | | | RS=L Reduced swing mode | f=37MHz | 19 | 27 | mA |
| | | | | f=71MHz | 24 | 40 | mA |
| | | | | f=160MHz | 38 | 73 | mA |
| I _{TCCS} | Transmitter Power Down Supply Current | /PDWN = L, All Inputs = L or H | | | 1 | 50 | μA |

(a) All Typ. values are at V_{cc}=1.8V, T_a=25°C . The 16 Grayscale Pattern (Fig1) inputs test for a typical display pattern.

(b) All Max. values are at V_{cc}=1.98V, T_a=85°C . LVDS Output Full Toggle Pattern (Fig2) produces maximum switching frequency for all the LVDS outputs.

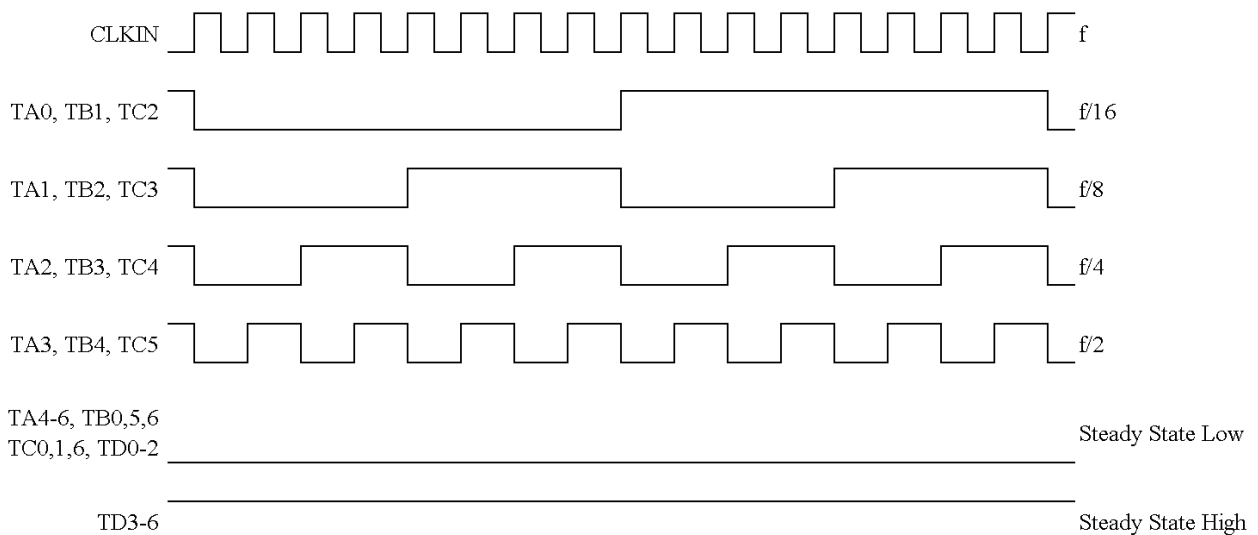


Fig1 16 Grayscale Pattern

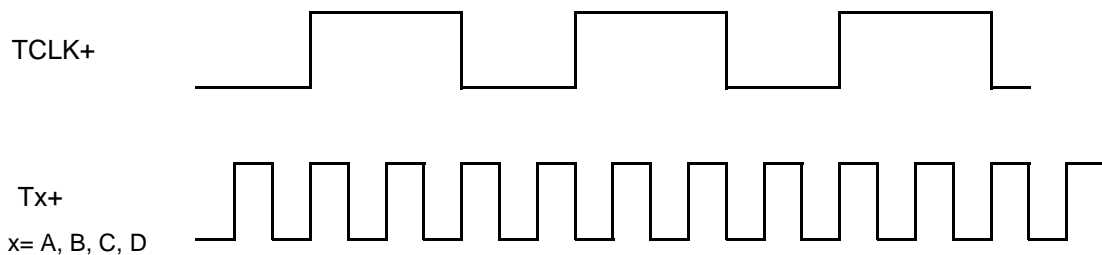


Fig2 LVDS Output Full Toggle Pattern

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|------------|---------------------------------------|-----------------------|----------------|-----------------------|-------|
| t_{TCP} | CLK IN Period | 6.25 | T | 125 | ns |
| t_{TCH} | CLK IN High Time | 0.35T | 0.5T | 0.65T | ns |
| t_{TCL} | CLK IN Low Time | 0.35T | 0.5T | 0.65T | ns |
| t_{TCD} | CLK IN to TCLK+/- Delay (Fig4) | 5T+3.1 | | 5T+8 | ns |
| t_{TS} | TTL Data Setup to CLK IN | 0.8 | | | ns |
| t_{TH} | TTL Data Hold from CLK IN | 0.8 | | | ns |
| t_{LVT} | LVDS Transition Time | | 0.6 | 1.5 | ns |
| t_{TOP1} | Output Data Position0 (T=6.25ns~15ns) | -0.15 | 0.0 | +0.15 | ns |
| t_{TOP0} | Output Data Position1 (T=6.25ns~15ns) | $\frac{T}{7} - 0.15$ | $\frac{T}{7}$ | $\frac{T}{7} + 0.15$ | ns |
| t_{TOP6} | Output Data Position2 (T=6.25ns~15ns) | $2\frac{T}{7} - 0.15$ | $2\frac{T}{7}$ | $2\frac{T}{7} + 0.15$ | ns |
| t_{TOP5} | Output Data Position3 (T=6.25ns~15ns) | $3\frac{T}{7} - 0.15$ | $3\frac{T}{7}$ | $3\frac{T}{7} + 0.15$ | ns |
| t_{TOP4} | Output Data Position4 (T=6.25ns~15ns) | $4\frac{T}{7} - 0.15$ | $4\frac{T}{7}$ | $4\frac{T}{7} + 0.15$ | ns |
| t_{TOP3} | Output Data Position5 (T=6.25ns~15ns) | $5\frac{T}{7} - 0.15$ | $5\frac{T}{7}$ | $5\frac{T}{7} + 0.15$ | ns |
| t_{TOP2} | Output Data Position6 (T=6.25ns~15ns) | $6\frac{T}{7} - 0.15$ | $6\frac{T}{7}$ | $6\frac{T}{7} + 0.15$ | ns |
| t_{TPLL} | Phase Lock Loop Set | | | 10.0 | ms |

AC Timing Diagrams

LVDS Output

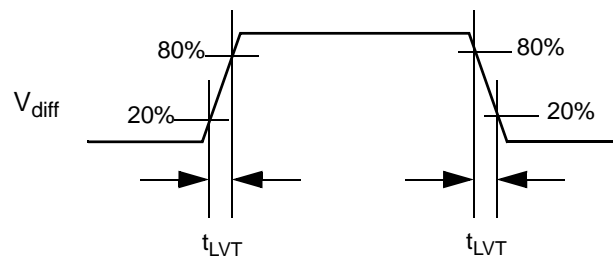
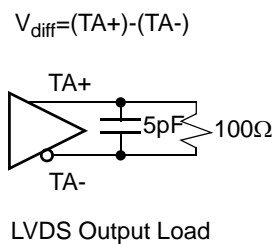


Fig3. LVDS Output Load and Transition Time

AC Timing Diagrams

TTL Inputs

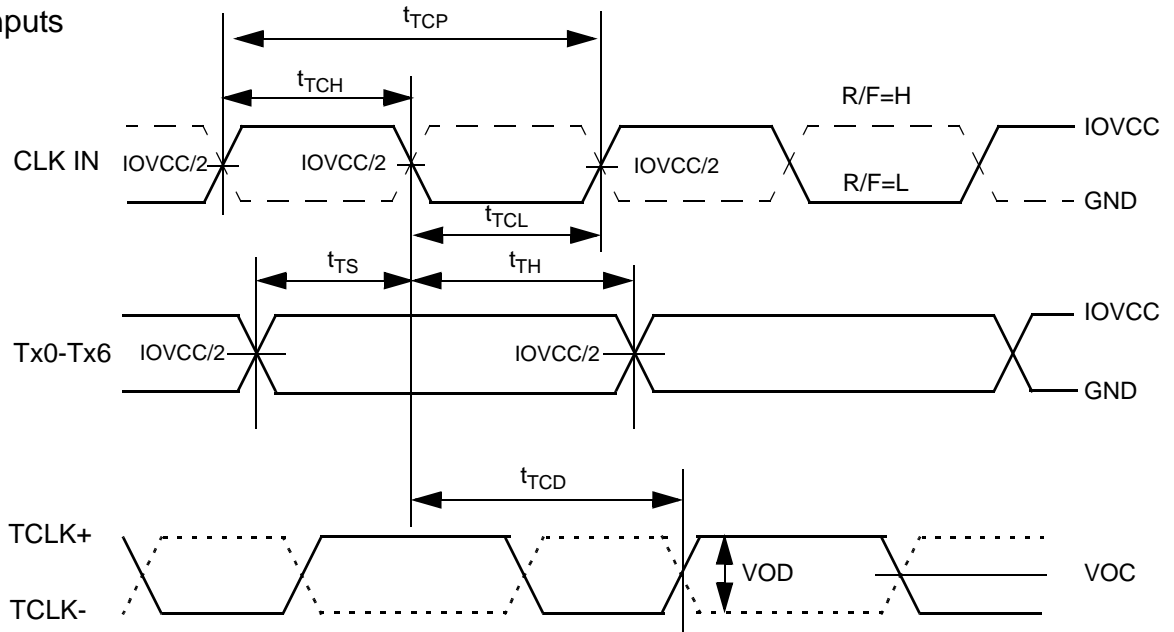


Fig4. CLKIN Period, High/Low Time, Setup/Hold Timing

AC Timing Diagrams

LVDS Output

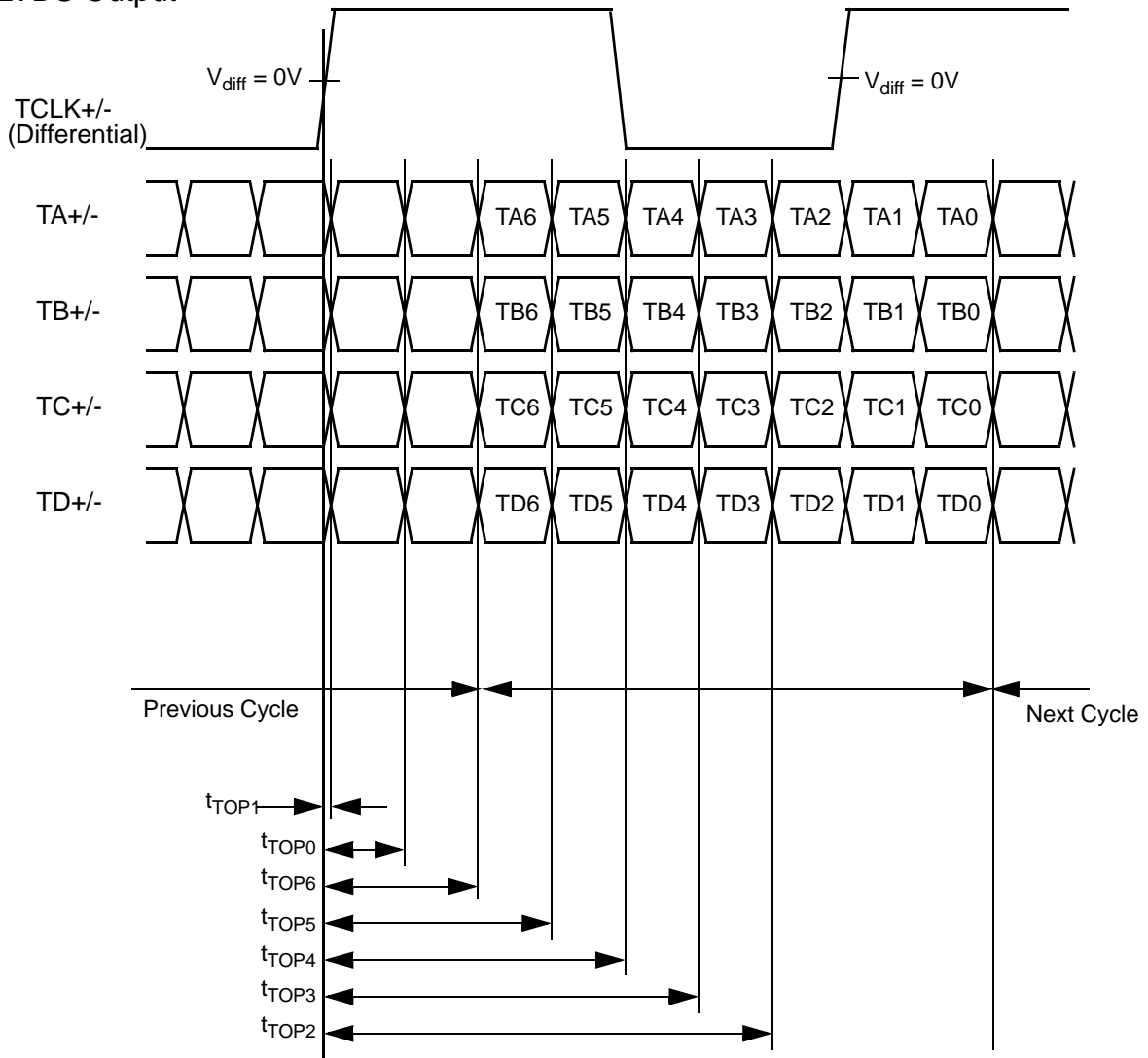


Fig5. LVDS Output Data Position

Phase Lock Loop Set Time

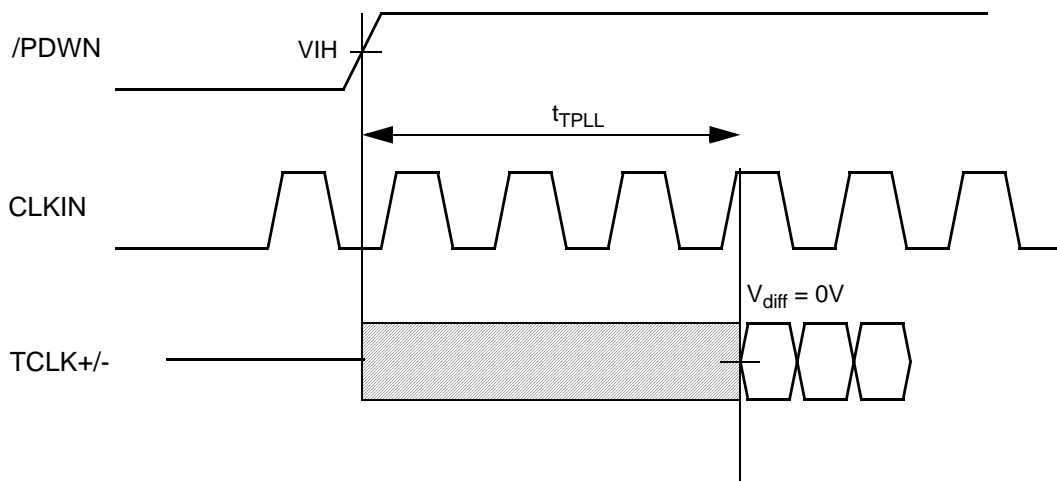


Fig6. PLL Lock Time

Note

1)Cable Connection and Disconnection

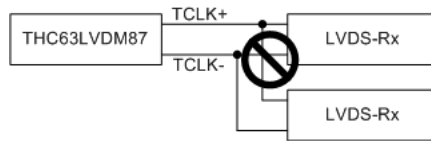
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

2)GND Connection

Connect the each GND of the PCB which THC63LVDM87 and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

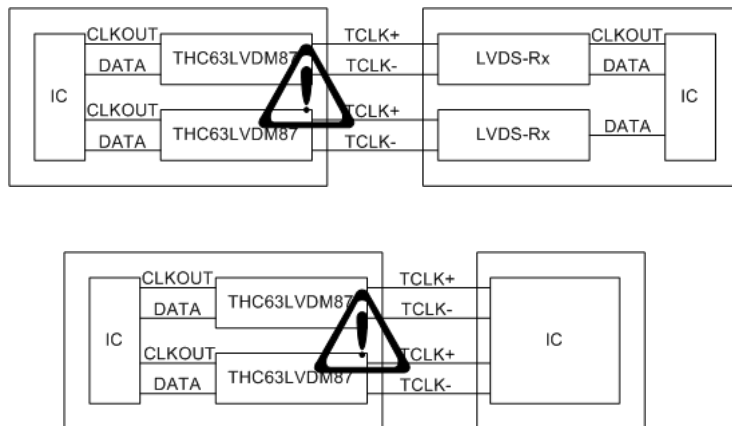
3)Multi Drop Connection

Multi drop connection is not recommended.



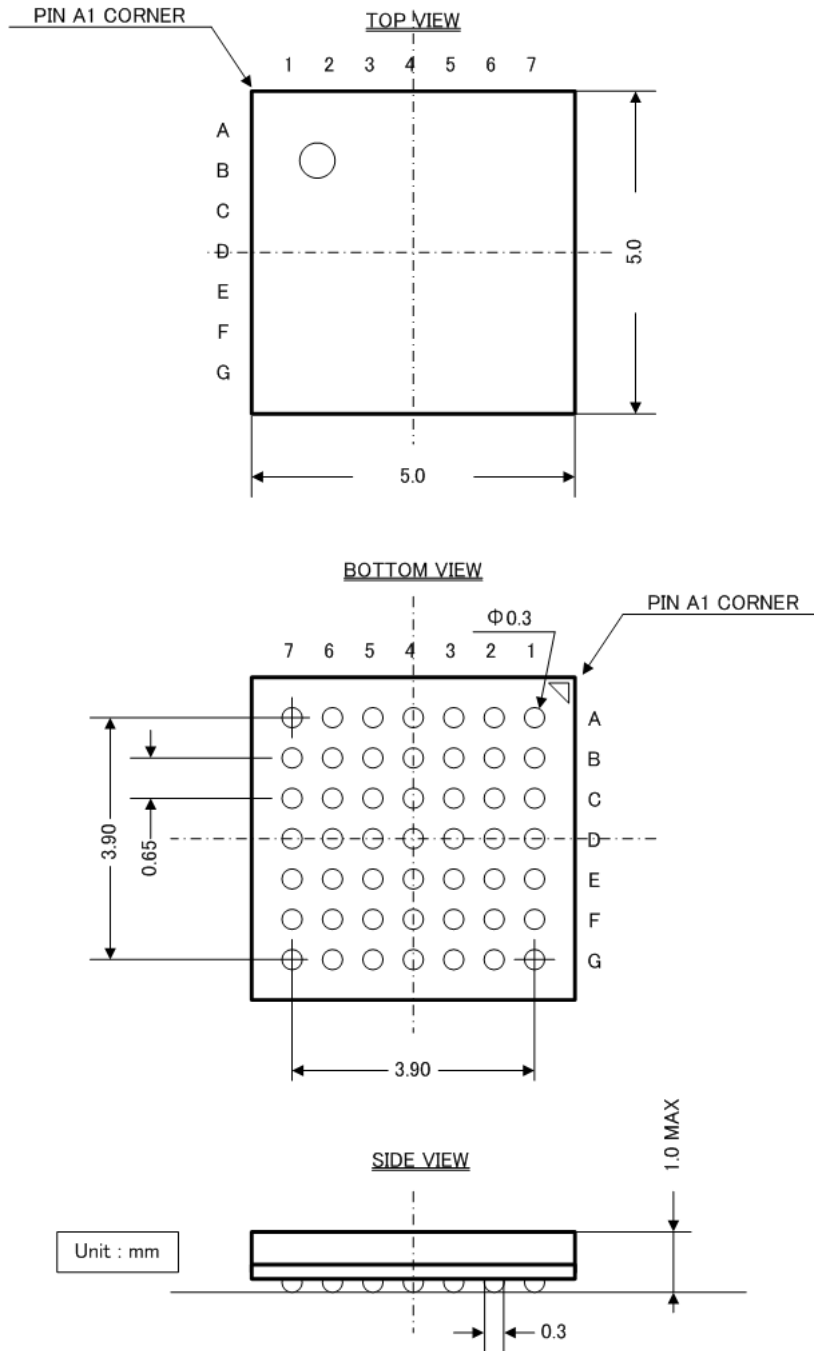
4)Asynchronous use

Asynchronous use such as following systems are not recommended.



Package

VFBGA



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