8-Bit Addressable Latches

The MC14099B is an 8-bit addressable latch. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. For the MC14099B the input is a unidirectional write only port.

The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, $Write/\overline{Read}$ or Chip Enable.

A Master Reset capability is available on both parts.

Features

- Serial Data Input
- Parallel Output
- Master Reset
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P _D	Power Dissipation, per Package (Note 1)	500	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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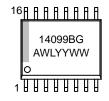


SOIC-16 WD DW SUFFIX CASE 751G

PIN ASSIGNMENT

Q7 [1 ●	16] V _{DD}
RESE [2	15] Q6
DATĀ [3	14] Q5
WRITE DISABLE	4	13] Q4
A0 [5	12] Q3
A1 [6	11	Q2
A2 [7	10] Q1
V _{SS} [8	9] Q0

MARKING DIAGRAM



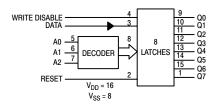
A = Assembly Location
WL = Wafer Lot

WL = Water Lot
YY = Year
WW = Work Week
G = Pb-Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MC14099B



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

				-55	5°C	25°C		125°C			
Characteristic		Symbol	V _{DD} Vdc	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Unit
Output Voltage V _{in} = V _{DD} or 0	"0" Level	V _{OL}	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
V _{in} = 0 or V _{DD}	"1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
Input Voltage $(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$ $(V_O = 9.0 \text{ or } 1.0 \text{ Vdc})$ $(V_O = 13.5 \text{ or } 1.5 \text{ Vdc})$	"0" Level	V _{IL}	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	"1" Level	V _{IH}	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	- - -	Vdc
Output Drive Current $ (V_{OH} = 2.5 \text{ Vdc}) $ $ (V_{OH} = 4.6 \text{ Vdc}) $ $ (V_{OH} = 9.5 \text{ Vdc}) $ $ (V_{OH} = 13.5 \text{ Vdc}) $	Source	I _{OH}	5.0 5.0 10 15	-3.0 -0.64 -1.6 -4.2		-2.4 -0.51 -1.3 -3.4	-4.2 -0.88 -2.25 -8.8		-1.7 -0.36 -0.9 -2.4	- - -	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	I _{OL}	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
Input Current		I _{in}	15	_	±0.1	_	±0.00001	±0.1	_	±1.0	μAdc
Input Capacitance (V _{in} = 0))	C _{in}	-	_	-	_	5.0	7.5	_	_	pF
Input Capacitance MC14599B — Data (pir (V _{in} = 0)	າ 3)	C _{in}	-	-	-	-	15	22.5	-	-	pF
Quiescent Current (Per Package)		I _{DD}	5.0 10 15	- - -	5.0 10 20	- - -	0.005 0.010 0.015	5.0 10 20	- - -	150 300 600	μAdc
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)		I _T	5.0 10 15			$I_T = (3)$	I.5 μΑ/kHz) f 3.0 μΑ/kHz) f I.5 μΑ/kHz) f	+ I _{DD}			μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
 The formulas given are for the typical characteristics only at 25°C.
 To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

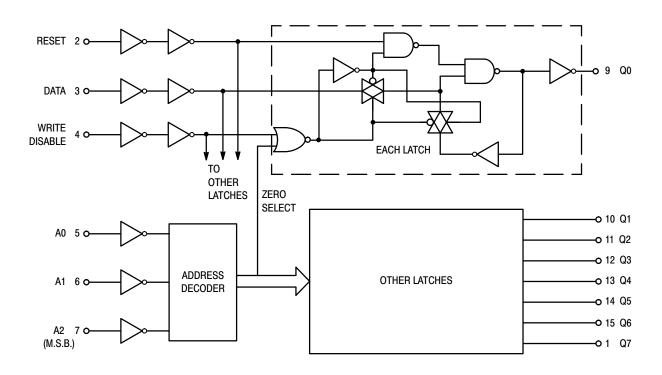
where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}, T_A = 25^{\circ}C$)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time	t _{TLH} ,					ns
t_{TLH} , $t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$	t _{THL}	5.0	_	100	200	
t_{TLH} , $t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$		10	_	50	100	
t_{TLH} , $t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$		15	_	40	80	
Propagation Delay Time	t _{PHL} ,					ns
Data to Output Q	t _{PLH}	5.0	_	200	400	
		10	_	75	150	
		15	_	50	100	
Write Disable to Output Q		5.0	_	200	400	ns
		10	_	80	160	
		15	_	60	120	
Reset to Output Q		5.0	_	175	350	ns
		10	_	80	160	
		15	_	65	130	
CE to Output Q (MC14599B only)		5.0	_	225	450	ns
		10	_	100	200	
		15	_	75	150	
Propagation Delay Time, MC14599B only	t _{PHL} ,					ns
Chip Enable, Write/Read to Data	t _{PLH}	5.0	_	200	400	
		10	_	80	160	
		15	_	65	130	
Address to Data		5.0	_	200	400	ns
		10	_	90	180	
		15	_	75	150	
Pulse Widths	t _{w(H)}					ns
Reset	t _{w(L)}	5.0	150	75	_	
		10	75	40	_	
		15	50	25	-	
Write Disable		5.0	320	160	_	ns
		10	160	80	_	
		15	120	60	-	
Set Up Time	t _{su}					ns
Data to Write Disable		5.0	100	50	_	
		10	50	25	_	
		15	35	20	_	
Hold Time	t _h	5 ^	450	75		ns
Write Disable to Data		5.0	150	75	_	
		10 15	75 50	40 25	_	
Outly Too						
Set Up Time	t _{su}	5.0	100	45	_	ns
Address to Write Disable		10 15	80 40	30 10	_	
					_	
Removal Time	t _{rem}	5.0	0	- 80	_	ns
Write Disable to Address		10	0	- 40 40	_	
		15	0	- 40	_	

^{5.} The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FUNCTION DIAGRAM



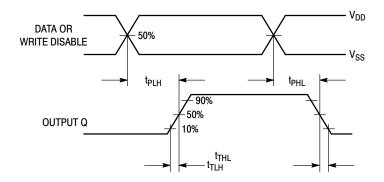
TRUTH TABLE

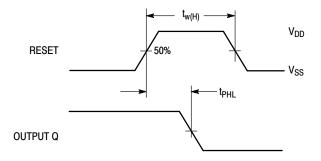
Write Disable	Reset	Addressed Latch	Unaddressed Latches
0	0	Data	Q _n *
0	1	Data	Reset †
1	0	Q _n *	Q _n *
1	1	Reset	Reset

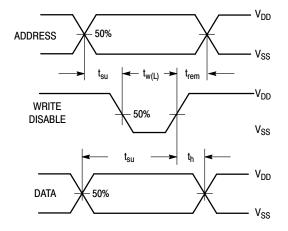
^{*}Q_n is previous state of latch. †Reset to zero state.

CAUTION: To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

SWITCHING WAVEFORMS







ORDERING INFORMATION

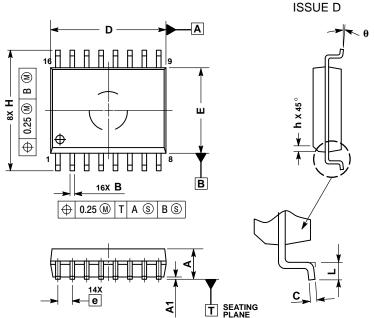
Device	Package	Shipping [†]
MC14099BDWG	SOIC-16 WB (Pb-Free)	47 Units / Rail
MC14099BDWR2G	SOIC-16 WB (Pb-Free)	1000 Units / Tape & Reel
NLV14099BDWR2G*	SOIC-16 WB (Pb-Free)	1000 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP

Capable.

PACKAGE DIMENSIONS

SOIC-16 WB CASE 751G-03



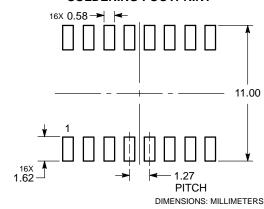
NOTES

- DIMENSIONS ARE IN MILLIMETERS.
- INTERPRET DIMENSIONS AND TOLERANCES
 PER ASME Y14.5M, 1994.
 DIMENSIONS D AND E DO NOT INLCUDE
 MOLD PROTRUSION.

- MAXIMUM MOLD PROTRUSION 0.15 PER SIDE. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS				
DIM	MIN	MAX			
Α	2.35	2.65			
A1	0.10	0.25			
В	0.35	0.49			
С	0.23	0.32			
D	10.15	10.45			
Е	7.40 7.60				
е	1.27 BSC				
Н	10.05	10.55			
h	0.25	0.75			
L	0.50	0.90			
а	0 °	7 °			

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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