

1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT54 plastic package intended for interfacing with low power drivers including microcontrollers.

2. Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits and microcontrollers
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

3. Applications

- Air conditioner indoor fan control
- General purpose motor control
- General purpose switching

4. Quick reference data

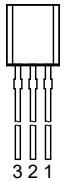
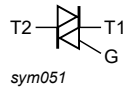
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 51\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	12.5	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	-	13.7	A
T_j	junction temperature		-	-	125	°C
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	-	0.4	3	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7	-	1.3	3	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7	-	1.4	3	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	3.8	7	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	1.3	5	mA
V_T	on-state voltage	$I_T = 1.4\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	1.2	1	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; $R_{GT1(ext)} = 1\text{ k}\Omega$; Fig. 12	10	20	-	V/ μs
dV_{com}/dt	rate of change of commutating voltage	$V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $dI_{com}/dt = 0.5\text{ A/ms}$; $I_T = 1\text{ A}$; gate open circuit	2	-	-	V/ μs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2	 <p>TO-92 (SOT54)</p>	 <p>sym051</p>
2	G	gate		
3	T1	main terminal 1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT131-600	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 51\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	12.5	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	13.7	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	0.78	A ² s
di_T/dt	rate of rise of on-state current	$I_G = 6\text{ mA}$	-	50	A/ μ s
		$I_G = 14\text{ mA}$	-	50	A/ μ s
		$I_G = 6\text{ mA}$	-	10	A/ μ s
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	125	°C

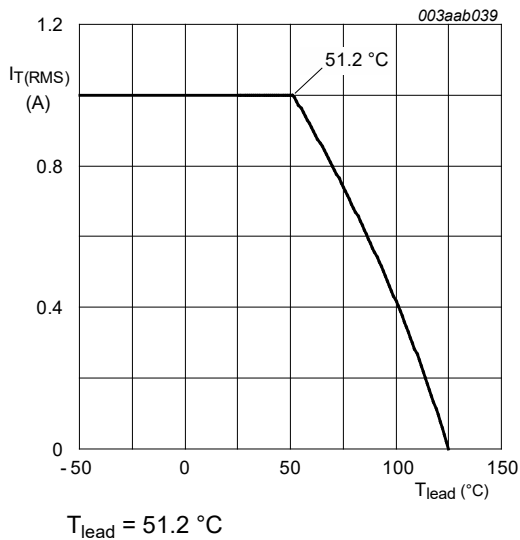


Fig. 1. RMS on-state current as a function of lead temperature; maximum values

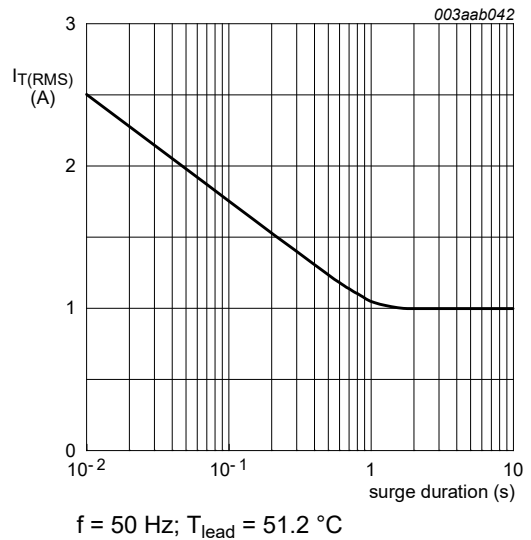


Fig. 2. RMS on-state current as a function of surge duration; maximum values

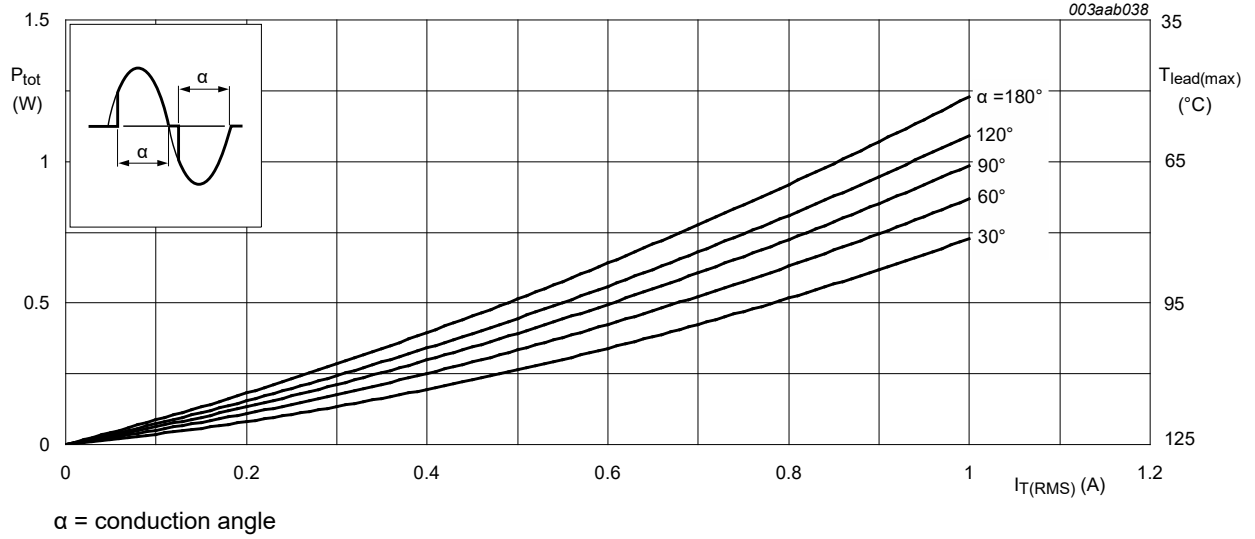


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

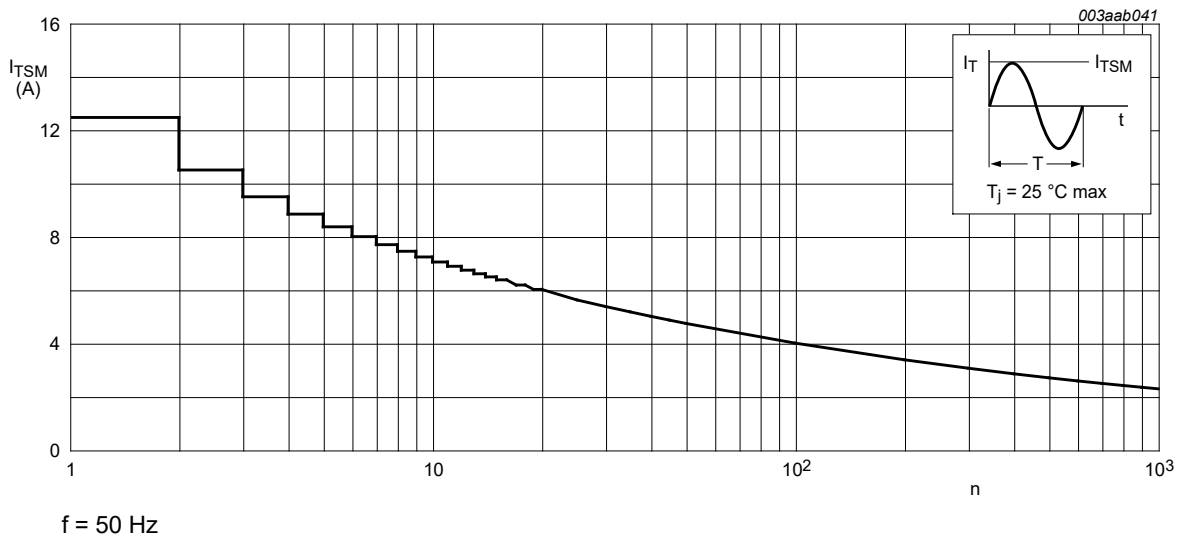
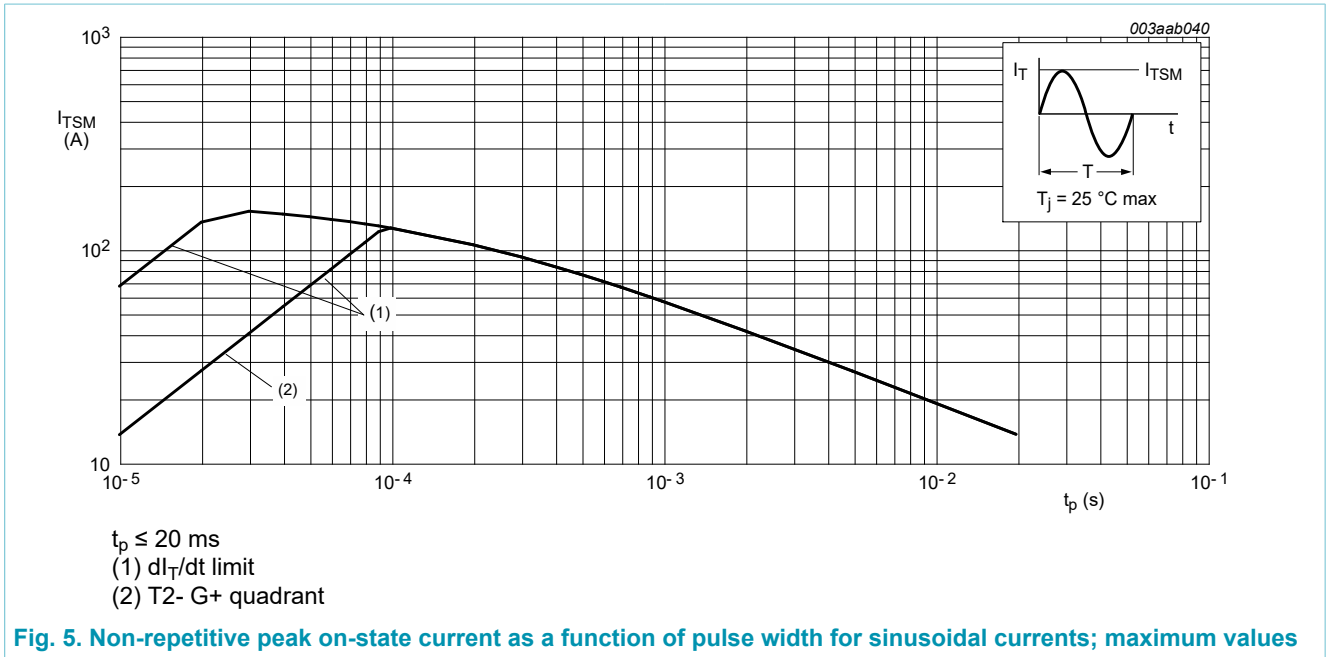


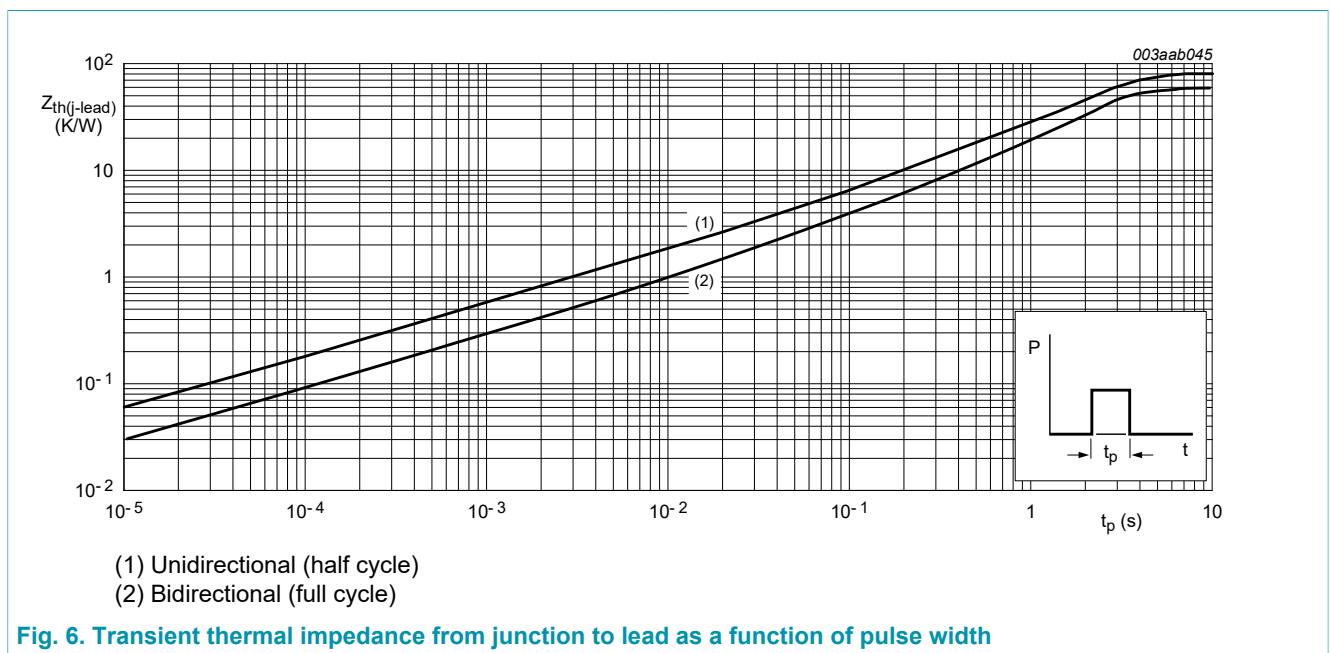
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{th(j-lead)}	thermal resistance from junction to lead	full cycle; Fig. 6	-	-	60	K/W
		half cycle; Fig. 6	-	-	80	K/W
R _{th(j-a)}	thermal resistance from junction to ambient free air	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ G+;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 7	-	0.4	3	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 7	-	1.3	3	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2- G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 7	-	1.4	3	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2- G+;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 7	-	3.8	7	mA
I_L	latching current	$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2+ G+;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	1.2	5	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2+ G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	4	8	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2- G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	1	5	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2- G+;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	2.5	8	mA
I_H	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 9	-	1.3	5	mA
V_T	on-state voltage	$I_T = 1.4\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 10	-	1.2	1	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 11	-	0.7	1	V
		$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 125\text{ }^\circ\text{C};$ Fig. 11	0.2	0.3	-	V
I_D	off-state current	$V_D = 600\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}; T_j = 125\text{ }^\circ\text{C}; (V_{DM} = 67\%$ $\text{of } V_{DRM}); \text{exponential waveform};$ $R_{GT1(\text{ext})} = 1\text{ k}\Omega;$ Fig. 12	10	20	-	V/ μ s
dV_{com}/dt	rate of change of commutating voltage	$V_D = 400\text{ V}; T_j = 125\text{ }^\circ\text{C}; dI_{com}/$ $dt = 0.5\text{ A/ms}; I_T = 1\text{ A}; \text{gate open}$ circuit	2	-	-	V/ μ s
t_{gt}	gate-controlled turn-on time	$I_{TM} = 1.5\text{ A}; V_D = 600\text{ V}; I_G = 0.1\text{ A}; dI_G/$ $dt = 5\text{ A}/\mu\text{s}$	-	2	-	μ s

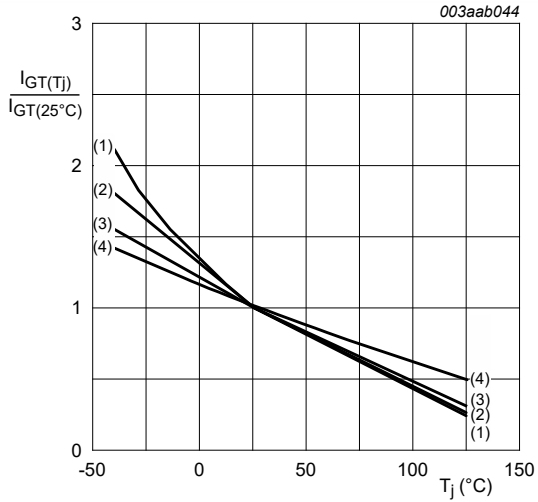


Fig. 7. Normalized gate trigger current as a function of junction temperature

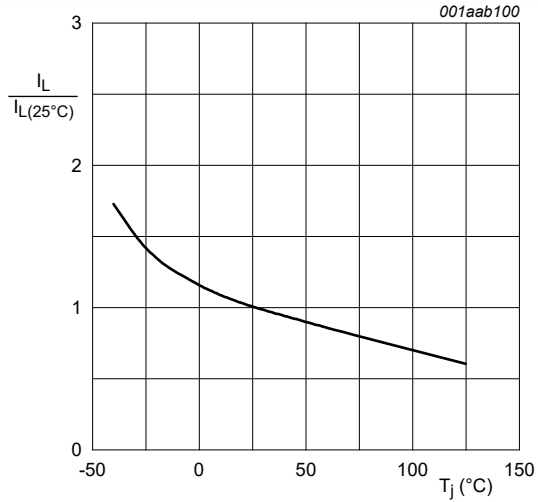


Fig. 8. Normalized latching current as a function of junction temperature

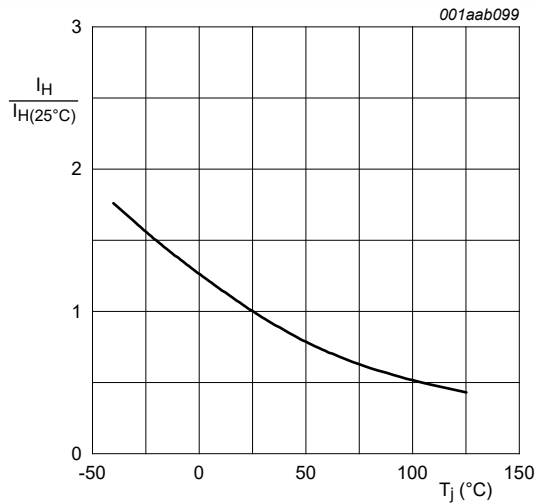
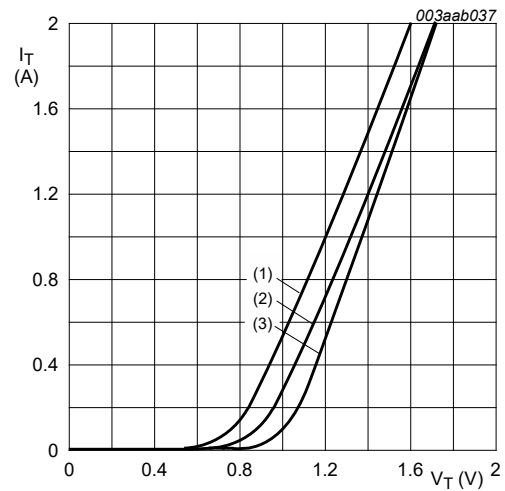


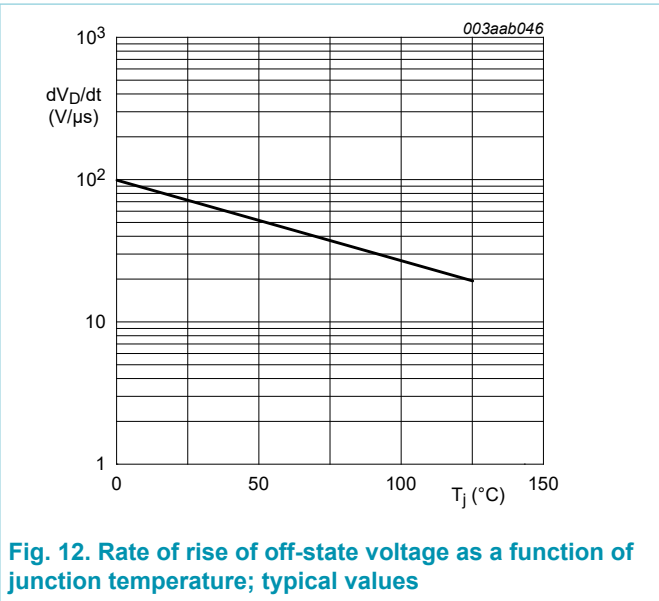
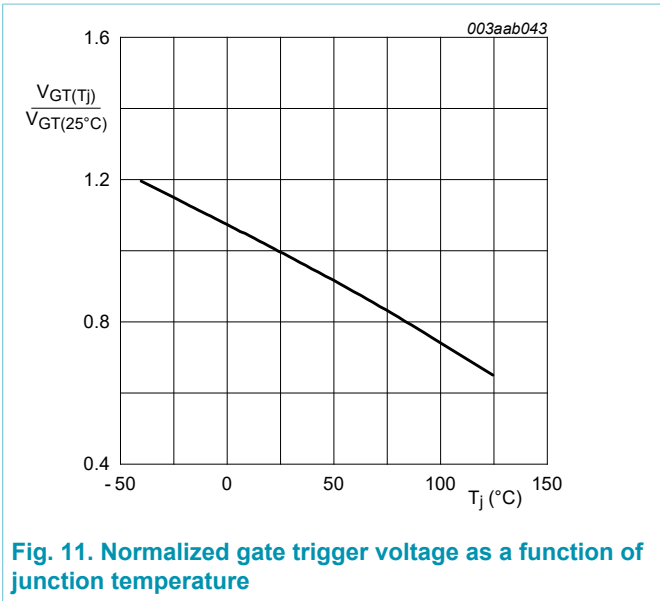
Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 0.92 \text{ V}; R_s = 0.4 \Omega$

- (1) $T_j = 125^\circ\text{C}$; typical values
- (2) $T_j = 125^\circ\text{C}$; maximum values
- (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage



10. Package outline

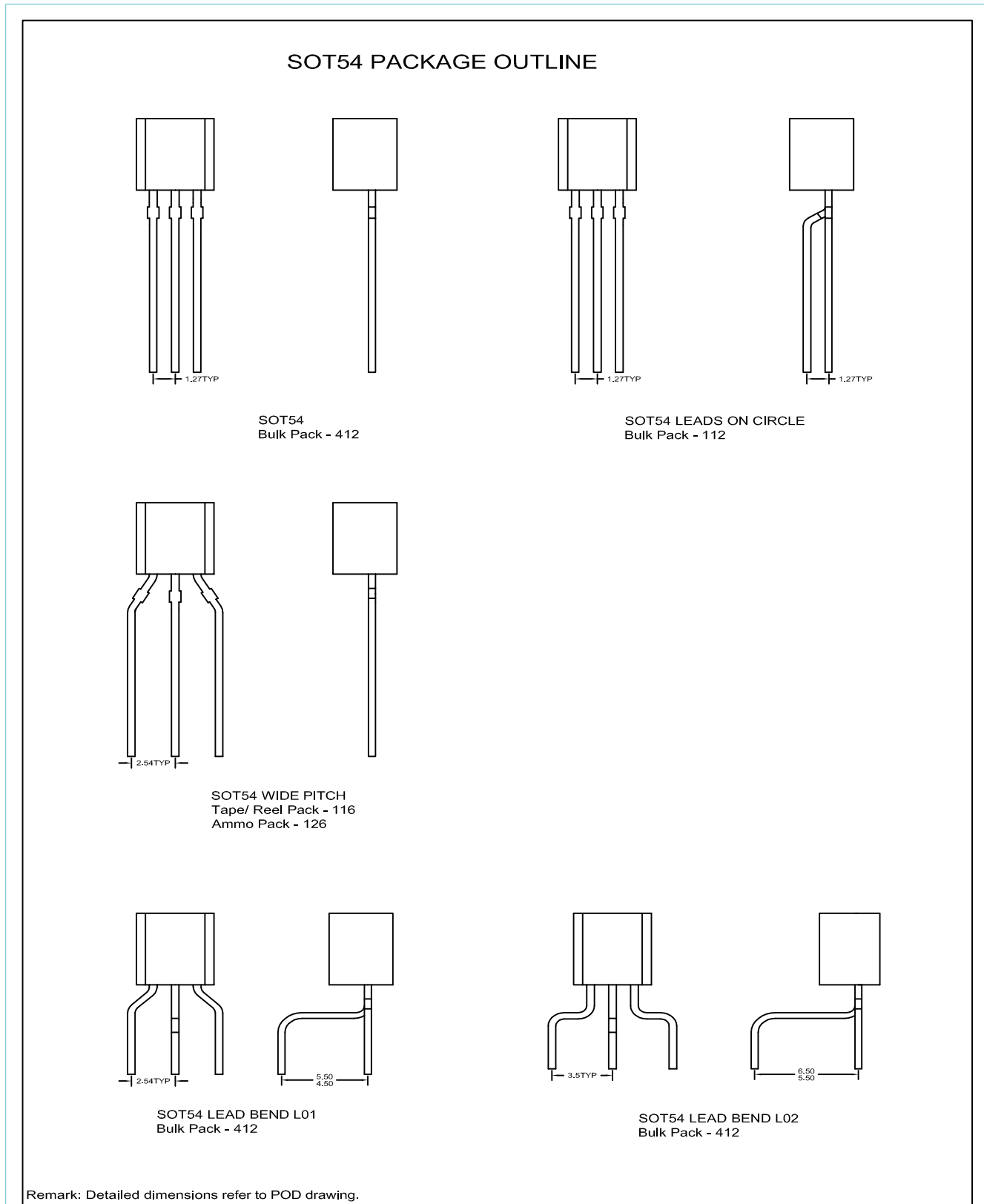


Fig. 13. Package outline TO-92 (SOT54)

11. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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