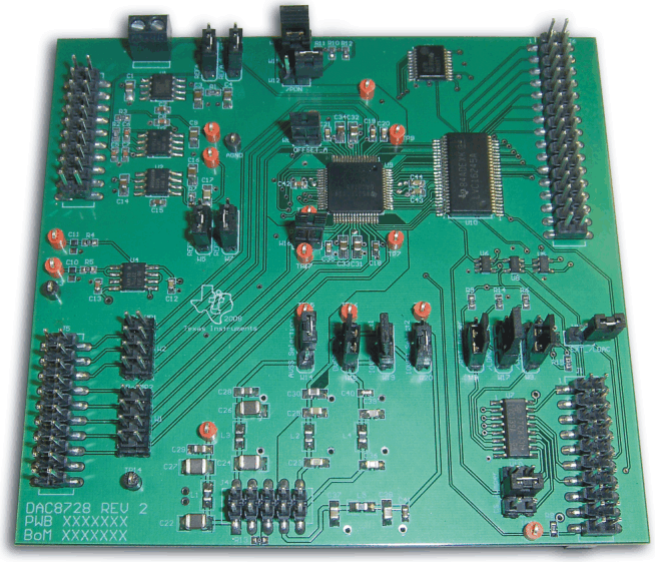
User's Guide
SBAU161–February 2010

DAC8728EVM



DAC8728EVM

This user's guide describes the characteristics, operation, and use of the DAC8728EVM, an evaluation board for the DAC8728. The DAC8728 is a low-power, octal, ±15V output, parallel input, 16-bit digital-to-analog converter (DAC). This evaluation module (EVM) allows evaluation of all aspects of the DAC8728 and gives control over every pin on the device. Complete circuit descriptions, schematic diagrams, and bills of material are included in this document.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Related Documentation

Device	Literature Number
DAC8728	SBAS466
OPA277	SBOS079A
REF5050	SBOS410C
REF02	SBVS003B
SN74LVC16245A	SCES062O
SN74LVC139	SCAS341O
SN74LVC374A	SCAS296N
5-6k Interface Board	SLAU104
DAP Signal Conditioning Board	SLAU105

Contents

List of Figures

List of Tables

1 EVM Overview

1.1 Features

DAC8728EVM:

- Full-featured evaluation board for the DAC8728, a 16-bit, parallel input, octal output digital-to-analog converter
- Onboard or external reference selection
- Onboard 5V or 2.5V reference voltage selection
- Configurable for single-supply or dual-supply operation
- Wide selection of digital and I/O voltages
- Parallel interface compatible with the 5-6k Interface Card for use with a wide variety of DSP starter kits
- Hardware or software control of control logic

1.2 Introduction

The DAC8728 is a 16-bit, octal, low-power, ±15V DAC that operates from independent AV_{DD}, AV_{SS}, and DV_{DD} supplies. A separate IOV_{DD} supply powers the parallel I/O buffers and eliminates the need for a level-shifting device between the DAC8728 and the external host controller.

As a result of the complexity of the parallel interface, the DAC8728 is not directly compatible with most of TI's processor families (that is, it is *not* compatible with the Modular EVM format). Therefore, this EVM was designed to support a wide variety of processors. Consequently, access to the parallel interface is achieved through external logic controlled by the host processor parallel interface.

Throughout this document, the acronym *EVM* and the phrase *evaluation module* are synonymous with the DAC8728EVM.

2 Analog Interface

Samtec part numbers SSW-110-22-S-D-VS and TSM-110-01-T-DV provide a convenient, 10-pin, dual-row header/socket combination at J5. This header/socket provides access to the analog output pins of the DAC. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 1 shows the pinout of the analog output connector, J5.

Table 1. J5: Analog Output Connector Pinout

Pin Number	Signal	Description
J5.2	VOUT_3	DAC Analog Output 3
J5.4	VOUT_2	DAC Analog Output 2
J5.6	VOUT_1	DAC Analog Output 1
J5.8	VOUT_0	DAC Analog Output 0
J5.10	VOUT_7	DAC Analog Output 7
J5.12	VOUT_6	DAC Analog Output 6
J5.14	VOUT_5	DAC Analog Output 5
J5.16	VOUT_4	DAC Analog Output 4
J5.18 - J5.20	Unused	Pins are unused and should be left open for use with future amplifier and sensor input modules.
J1.1- J1.19 (odd)	AGND	Analog ground connections

The analog interface is populated on the top and the bottom of the evaluation board. All of the output pins are routed directly from the DAC8728 to the J5 connector. Additionally, they can be routed through an OPA277 buffer circuit using JP1 and JP2. The output of the buffer circuit is routed to TP3 and TP4.

The output of the DAC8728 internal offset DAC is routed to test points TP10 and TP17.

The DAC8728EVM has two external reference voltage options. J2.2 controls the external reference voltage for the REF-A input. J2.1 controls the reference for the REF-B input. When an external reference is used, jumpers JP4-JP7 must be configured properly. Test points TP8 and TP7 can be used to verify that the jumpers are configured properly and the correct reference voltage is applied to the DAC.

The V_{MON} output allows the user to relay any of the DAC outputs, as well as A_{IN}-0 or A_{IN}-1, to a single pin. V_{MON} is routed to test point TP9 and is connected to a 0.1μF capacitor.

3 Digital Interface

The DAC8728EVM is designed for easy interfacing to multiple control platforms. To achieve this host processor flexibility, an unconventional way of controlling this EVM had to be developed. Therefore, the 16-bit data bus from the host processor is shared between the 16-bit data bus and the 5-bit A0–A4 address bus on the DAC8728. This configuration is accomplished with the use of the SN74LVC374 8-bit Rising-Edge Triggered Latch (U11 on EVM). As a result, every write or read operation to the DAC8728 is a two-step process. The first step writes the appropriate A0–A4 address to the first five bits of the data bus and latches it into the SN74LVC374; this process sets up the appropriate address for the DAC8728. The second step writes to (or reads from) the selected address data with all 16 bits of the parallel data bus.

The four address bits from the host processor are used to control the SN74LVC139, a two-channel, two-to-four line decoder/demultiplexer (U7 on EVM). This device is used to create eight control bits from the processor address that are used around the board to control various signals such as the LATCH input to the SN74LVC374 and the DC_$\overline{CS}$ (daughter card chip select). For every write or read operation, the appropriate signals must be selected; therefore, specific address combinations are used to achieve different results. These combinations are explored further in the next section.

Jumper options are provided on the board to allow direct hardware control over the digital control pins: $\overline{LDAC}$, $\overline{CLR}$, $\overline{RST}$, $\overline{RSTSEL}$, and USB/BTC. Jumpers JP3, JP9 to JP11, JP13, and JP17 can be set to allow the outputs of the SN74LVC139 to control the LATCH_CTRL, R/$\overline{W}$, $\overline{CLR}$, $\overline{RST}$, DC_$\overline{CS}$, and LDAC_CTRL signals on the EVM.

Onboard digital logic is used to control the DAC8728 $\overline{CS}$ pin. The $\overline{WE}$ and $\overline{RE}$ pins and the DC_$\overline{CS}$ output of the SN74LVC139 (U7) are used to derive the appropriate DAC8728 $\overline{CS}$ signal. JP10 allows the user to choose between three addresses to control the DC_$\overline{CS}$ signal on the EVM. Having this ability to select the address of the DAC8728 enables the possibility of *stacking* other EVM boards on top of the DAC8728EVM.

Jumpers JP17, JP9, and JP3 control the $\overline{LDAC}$, $\overline{RST}$, and $\overline{CLR}$ pins, respectively. The default state of all these jumpers is a shunt across pins 1 and 2 of the header. This shunt routes the software-controlled outputs from the SN74LVC139 (U7) to the DAC8728. By removing the shunts on these jumpers, the default hardware state for these pins is selected: high for $\overline{CLR}$ and $\overline{RST}$, and low for $\overline{LDAC}$. By shunting pins 2 and 3 of these headers, the opposite hardware states for these pins are selected. Alternatively, with the jumpers removed, the user can apply external signals to pin 2 of these jumpers to control the signals via an external source.

Jumper JP11 and JP13 control the USB/BTC and $\overline{RSTSEL}$ pins on the DAC8728. Applying a shunt across these jumpers ties the respective pin to GND. By removing the shunt, the pin is connected to IOV_{DD} through a pull-up resistor.

4 Parallel Control

Samtec part numbers SSW-110-22-S-D-VS and TSM-110-01-T-DV provide a convenient, 10-pin, dual-row header/socket combination at J1. This header/socket provides access to the digital control pins of the EVM. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 2 describes the parallel interface pins.

Table 2. J2: Parallel Interface Pins

Pin Number	Signal	Description
J2.1	$\overline{CE}$	DSP Chip Enable Strobe: Signal is driven low by the DSP each time a parallel bus write or read occurs and is driven high once it completes
J2.3	$\overline{WE}$	DSP Write Strobe: Signal is cycled low to high within the $\overline{CE}$ strobe when a parallel bus write occurs
J2.5	$\overline{RE}$	DSP Read Strobe: Signal is cycled low to high within the $\overline{CE}$ strobe when a parallel bus read occurs
J2.7	EVM_A0	DSP Address line 0: Used in conjunction with U8 to control LATCH, R/$\overline{W}$, $\overline{CLR}$ and $\overline{RST}$ signals
J2.9	EVM_A1	DSP Address line 1: Used in conjunction with U8 to control LATCH, R/$\overline{W}$, $\overline{CLR}$ and $\overline{RST}$ signals
J2.11	EVM_A2	DSP Address line 2: Used in conjunction with U8 to control DC_$\overline{CS}$ and $\overline{LDAC}$
J2.13	EVM_A3	DSP Address line 3: Used in conjunction with U8 to control DC_$\overline{CS}$ and $\overline{LDAC}$
J2.15	Unused	—
J2.17	Unused	—
J2.19	INT	DSP Interrupt Input: Connects to $\overline{BUSY}$ output of the DAC8728

Figure 1 shows the parallel control header and the connections to the SN74LVC139.

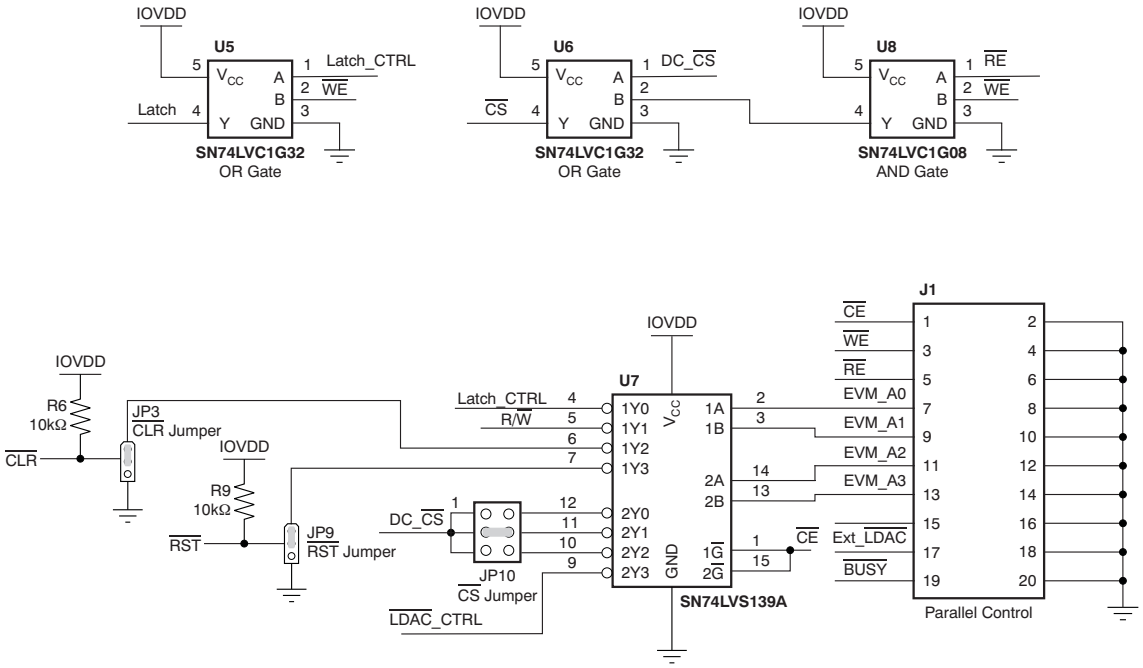


Figure 1. Parallel Control Header and SN74LVC139

4.1 Required External Logic

Most of TI's host processors do not have a hardware chip select that meets the timing requirements of the DAC8728. Therefore, external logic was added to the EVM to create an acceptable $\overline{CS}$ signal for the DAC using the $\overline{WE}$, $\overline{RE}$, and DC_$\overline{CS}$ signals. This circuit and related truth table are shown in this section. Figure 2 and Table 3 illustrate the external logic behavior.

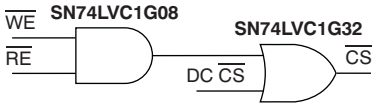


Figure 2. Chip-Select External Logic

As you can see from the timing diagram, the $\overline{CS}$ line never goes low unless the DC_$\overline{CS}$ signal and either $\overline{WE}$ or $\overline{RE}$ is low as well.

Table 3. External Logic Behavior

DC_$\overline{CS}$	$\overline{WE}$	$\overline{RE}$	$\overline{CS}$
0	0	0	Not a valid DSP output
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Also, in order to appropriately control the CLK input to the SN74LVC374 (U11), the LATCH_CTRL output of the SN74LVC139 (U7) had to be logic ORed with the $\overline{WE}$ signal. This configuration ensures that the data are latched into the SN74LVC374 while it is still valid from the DSP. This circuit and related truth table (Figure 3 and Table 4, respectively) can be seen below.

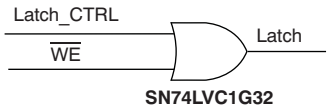


Figure 3. LATCH External Logic

Table 4. SN74LVC374 Control

LATCH_CTRL	$\overline{WE}$	LATCH
0	0	0
0	1	1
1	0	1
1	1	1

The final piece of external logic gives the EVM user the ability to control the $\overline{LDAC}$ signal from both the processor I/O pins and the SN74LVC139 (U7) output. This control is achieved through an AND gate that uses the $\overline{EXT\_LDAC}$ signal and the $\overline{LDAC\_CTRL}$ signal to drive the input on the DAC8728. The interrupt service routine toggles the $\overline{EXT\_LDAC}$ signal and then waits for the next interrupt. Table 5 displays the behavior of the logic.

Table 5. $\overline{LDAC}$ Control

EXT_$\overline{LDAC}$	$\overline{LDAC\_CTRL}$	$\overline{LDAC}$
0	0	0
0	1	0
1	0	0
1	1	1

4.2 DC_$\overline{CS}$ Signals

The DC_$\overline{CS}$ signal is used as a *board select* for the EVM. It is an active low signal that controls the output enable bit on the SN74LVC16245 and, in conjunction with the external logic, is used to create the $\overline{CS}$ signal for the DAC8728. The user selects one of the three possible addresses using JP10. By default, the DC_$\overline{CS}$ signal is set to the 2Y1 output of the SN74LVC139. When accessing the parallel bus, if the appropriate address is not selected to pull the DC_$\overline{CS}$ signal on the EVM low, then the SN74LVC16245 (U10) is not active and the DAC8728 does not see the activity on the bus.

4.3 $\overline{CS}$ Signal

The $\overline{CS}$ signal is formed from the output of the logic circuit. The DAC8728 uses the $\overline{CS}$ signal in combination with the R/$\overline{W}$ signal to enable the input and output buffers. When the $\overline{CS}$ signal is high, the data input lines to the DAC8728 are HI-Z. On the falling edge of $\overline{CS}$, data on the parallel bus are passed into the DAC8728; on the rising edge, data are latched into the appropriate register.

4.4 R/$\overline{W}$ Signal

The R/$\overline{W}$ signal is located on the 1Y1 output of the SN74LVC139 (U7). During read and write commands to the EVM, the appropriate address must be selected to set the R/$\overline{W}$ bit either high for a read or low for a write. The DAC8728 uses the R/$\overline{W}$ signal to enable and disable the input and output buffers inside the chip. When the R/$\overline{W}$ signal is high and $\overline{CS}$ is low, the output buffers are activated sending the register data from the DAC8728 to the parallel bus. When R/$\overline{W}$ is low and $\overline{CS}$ is low, the input buffers are activated and the data present on the bus are passed into the DAC.

4.5 LATCH, LATCH_CTRL Signals

The LATCH_CTRL signal is located on the 1Y0 output of the SN74LVC139 (U7). The LATCH_CTRL signal is logic ORed with the $\overline{WE}$ signal to create the LATCH signal that is used to control the CLK input to the SN74LVC374 on the EVM. During the first stage of a read or write operation, the LATCH_CTRL bit is taken low while the DAC8728 register address is placed on the first five bits of the parallel data bus. When the $\overline{WE}$ signal goes low during this write, the LATCH signal also transitions low. When the $\overline{WE}$ signal returns high, the LATCH signal also goes high, which then locks the DAC8728 register address to the A0–A4 address bus on the DAC8728.

4.6 $\overline{LDAC}$, LDAC_CTRL, $\overline{EXT\_LDAC}$ Signals

The $\overline{LDAC}$ signal is driven by the external logic and is used to update the DAC outputs with the data present in the V_{OUT} registers. This signal is active low and can be triggered synchronously or asynchronously. The LDAC_CTRL signal is located on the 2Y3 output of the SN74LVC139 (U7). The $\overline{EXT\_LDAC}$ signal is driven from pin J1.17 on the parallel control header.

4.7 $\overline{CLR}$ Signal

The $\overline{CLR}$ signal is located on the 1Y2 output of the SN74LVC139 (U7). When set low, the DAC analog outputs are tied to GND through an internal 20kΩ resistor and the output buffers are disabled. For normal operation, this signal must remain high.

4.8 $\overline{RST}$ Signal

The $\overline{RST}$ signal is located on the 1Y3 output of the SN74LVC139 (U7). When set low, the device is in a full hardware reset. The analog outputs are connected to GND through the internal low impedance, while the input registers and OFFSET and DAC latches are loaded with the value defined by the $\overline{RSTSEL}$ pin on the DAC8728. The gain registers and zero registers are loaded with the respective default values and the communication bus is disabled. For normal operation, the $\overline{RST}$ signal must remain high.

4.9 SN74LVC139 Outputs

Table 6 through Table 8 show the truth tables for the outputs of the SN74LVC139. Note that *A3 to A0* correspond to the signals from the J1 header.

Table 6. A0 and A1 Address Combinations

A1	A0	$\overline{RST}$	$\overline{CLR}$	R/$\overline{W}$	LATCH_CTRL
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

Table 7. A2 and A3 Address Combinations

A3	A2	$\overline{LDAC}$	DC_$\overline{CS}$2	DC_$\overline{CS}$1	DC_$\overline{CS}$0
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

Table 8. Commonly-Used Address Combinations

	A3 to A0 (Hex)
Open1 + LATCH_CTRL	0x0
DC_$\overline{CS}$ + R/$\overline{W}$	0x5
$\overline{LDAC}$ + LATCH_CTRL	0xC
DC_$\overline{CS}$ + Open2	0x7

4.10 $\overline{BUSY}$ Signal

The $\overline{BUSY}$ signal is routed to an interrupt on the host processor; this allows the user to monitor the state of the correction engine. The $\overline{BUSY}$ pin is pulled low when the correction engine runs, and is pulled high by an external pull-up when the correction process completes.

4.11 Parallel Data

The DAC8728EVM uses Samtec part numbers SSW-116-22-S-D-VS and TSM-116-01-T-DV to provide a convenient, 16-pin, dual row header/socket combination at J6. This header/socket combination provides access to the parallel data pins of the DAC8728 and the inputs to the SN74LVC374. Data lines D0 to D15 are located on the odd numbered pins 1 through 31 on the J6 header. Even pin numbers 2 to 32 are connected to digital ground. Additionally, data lines D0 to D4 are shared between the DAC8728 and the SN74LVC374; this configuration can be seen in Figure 4.

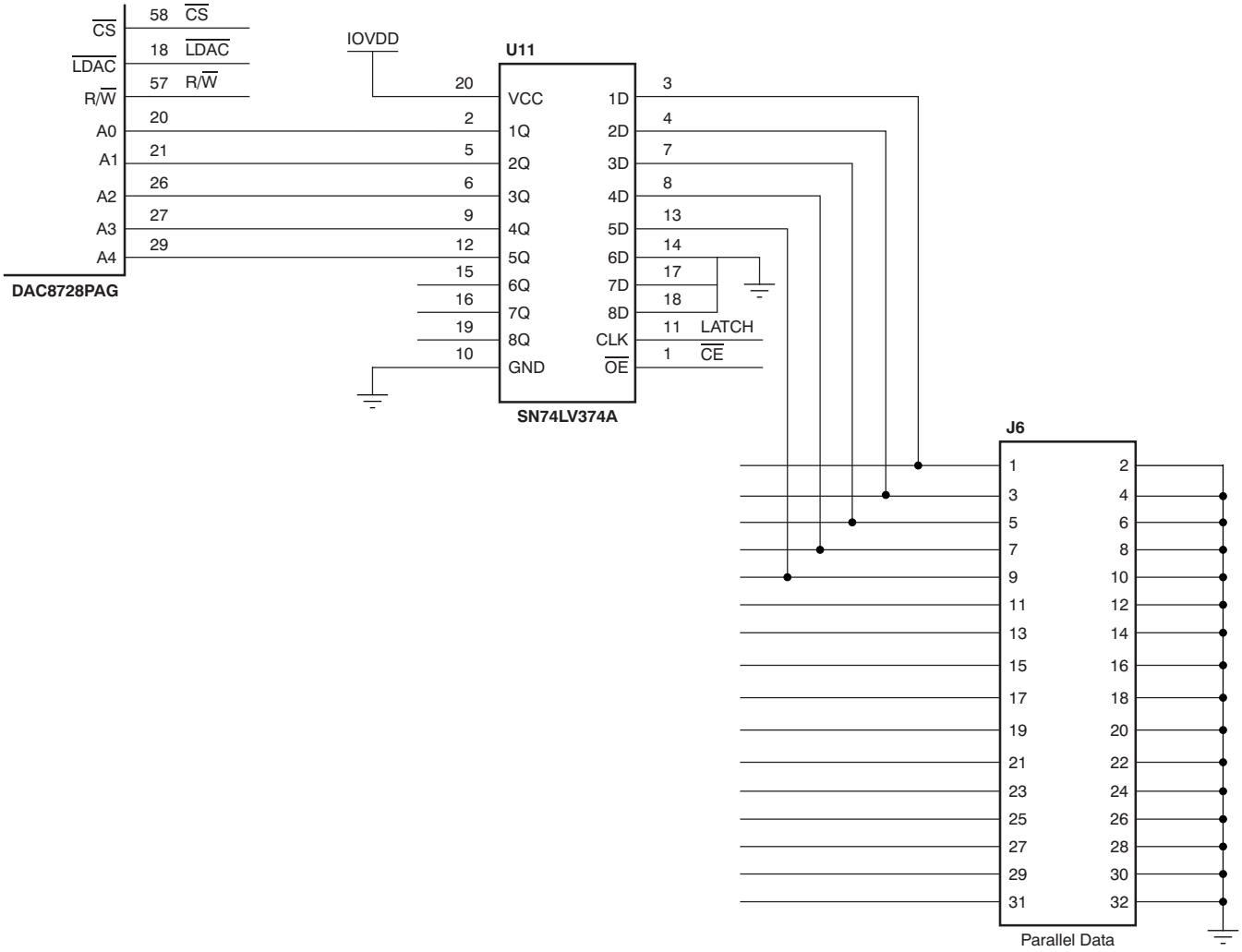


Figure 4. Shared 16-Bit Parallel Bus

5 Power Supplies

J4 is the power-supply input connector. Table 9 lists the configuration details for J4. The voltage inputs to the DAC can be applied directly to the device. The DAC8728 requires multiple power supplies to operate. AV_{DD}, AV_{SS}, DV_{DD}, and IOV_{DD} are required to properly power the DAC. The power should be applied in this order: IOV_{DD}, DV_{DD}, then AV_{DD} and AV_{SS}, followed by the reference voltage.

CAUTION

This sequence must be followed in order to prevent damage to the device.

Table 9. J4 Configuration: Power-Supply Input

Pin No.	Pin Name	Function	Required
J4.1	+VA	+8V to +36V analog supply	Yes
J4.2	-VA	–18V to –4.5V analog supply	Yes
J4.3	+5VA	+5V analog supply	No
J4.4	-5VA	-5V analog supply	No
J4.5	DGND	Digital ground input	Yes
J4.6	AGND	Analog ground input	Yes
J4.7	+1.8VD	1.8V digital supply	Optional
J4.8	+3.3VD	3.3V digital supply	Optional
J4.9	VD1	Not used	No
J4.10	+5VD	+5V digital supply	Optional

NOTE: To avoid damage to the DAC8728, DV_{DD} must stay greater than or equal to IOV_{DD}.

The DAC8728EVM board analog section can be powered from either a single-supply or dual supply. In unipolar mode, AV_{SS} is tied to AGND and AV_{DD} is powered from +VA, a +8 to +36V analog supply range. When the DAC8728 is run in bipolar mode, AV_{SS} and AV_{DD} are required. AV_{SS} can range from –4.5V to –18V, and AV_{DD} can range from +4.5V to +18V. The DAC8728 AV_{DD} (+VA) supply can be as low as +4.5V, but in order to properly power the REF02, +VA must be at least +8V. Jumper JP14 allows the user to select between bipolar and unipolar modes. AV_{SS} is either routed to the –VA (pin J4.2) or is connected to AGND.

DV_{DD} powers the digital core of the DAC8728 and can vary from V_{REF} to +5.5V. Care must be taken to ensure that the EVM is not set up in a state where V_{REF} is greater than DV_{DD}. Jumper JP15 allows the user to select between +3.3V and +5V for DV_{DD}.

The IOV_{DD} supply sets the voltage of the digital interface and should be configured to match the I/O voltage of the host processor. Jumpers JP19 and JP20 allow the user to select between +1.8V, +3.3V, and +5V for IOV_{DD}. To avoid damaging the DAC8728, DV_{DD} must stay greater than or equal to IOV_{DD}.

Alternate power sources can be applied via various test points located on the EVM. Refer to the schematic at the end of this document for details.

NOTE: While filters are provided for all power-supply inputs, optimal performance of the EVM requires a clean, well-regulated power source.

6 Reference Voltage

The DAC8728EVM is configured with two different onboard precision references. The evaluation module has both a +2.5V and +5V reference using the REF5025 and the REF02, respectively. By using the screw terminal J2, the user can also apply external reference voltages to the board. Any external voltage applied to J2 must be within the +1.0 to +5.5V reference voltage range specification for the DAC8728. The DAC8728 has two different references, REF_A for $V_{OUT}0$–$V_{OUT}3$ and REF_B for $V_{OUT}4$–$V_{OUT}7$, respectively. Using jumpers JP4 to JP7, both REF_A and REF_B can be individually configured to either +2.5V, +5V, or the external reference input voltage. Jumpers JP6 (REF-A) and JP7 (REF-B) are used to select between using an onboard reference or an external reference. If an onboard reference is selected, jumpers JP4 (REF-A) and JP5 (REF-B) are used to select between the 2.5V or the 5.0V reference. The reference circuits can be seen in the schematic at the end of this document.

7 EVM Operation

CAUTION

Before power is applied to J4 on the EVM, be sure that the jumpers on the board are configured according to the factory default settings described below.

This section provides information on the analog input and digital control of the DAC8728EVM, as well as the default settings.

7.1 Analog Output

The DAC8728 has eight analog outputs that are available at the J5 header or the JP1 and JP2 jumper headers. Each of these outputs is referenced to the board ground.

Jumpers JP1 and JP2 allow the user to route the DAC outputs to the input of a voltage-follower amplifier that drives an RC low-pass filter. The capacitor is not installed and a 0Ω resistor connects the op amp output to the test-points. A filter can be installed by replacing the 0Ω resistor and installing a capacitor.

CAUTION

Only *one* shunt may be placed across each header. If more than one shunt is placed across either JP1 or JP2, it will directly short two of the DAC analog outputs together, possibly causing irreversible damage to the DAC8728.

The OFFSET-A and OFFSET-B analog outputs are routed to TP10 and TP17. The OFFSET feature can only be used in bipolar mode. In unipolar mode, a shunt must be placed across JP8 and JP16 to connect the OFFSET-x pins to the board ground.

V_{MON} is the channel monitor output. It can relay any of the eight analog output signals, the OFFSET-A/B, and the Ref Buffer A/B. The output pin has a 0.1μF capacitor connected. By default, the V_{MON} pin is in 3-state mode.

7.2 Digital Control

The digital control signals can be applied directly to J1 (top or bottom side). The DAC8728EVM can also be connected directly to a DSP or microcontroller interface board.

No specific evaluation software is provided with this EVM; however, various code examples are available that show how to use this EVM with a variety of digital signal processors from Texas Instruments. Check the specific device product folders on the TI web site or send an e-mail to dataconvapps@list.ti.com for a listing of available code examples. The EVM Gerber files are also available on request.

7.3 Default Jumper Settings and Switch Positions

The default configuration of the DAC8728EVM is summarized in Table 10.

Table 10. DAC8718EVM Factory Default Configuration

Reference	Jumper-position (s)	Function
JP1	Open	Can be used to route any of the V_{OUT}-0 to V_{OUT}-3 signals to the input of the OPA2277 to be low-pass filtered and buffered
JP2	Open	Can be used to route any of the V_{OUT}-4 to V_{OUT}-7 signals to the input of the OPA2277 to be low-pass filtered and buffered
JP3	1-2	$\overline{CLR}$ is controlled by the 1Y2 output of the SN74LVC139
JP4	1-2	The REF2.5V output of the REF5025 is routed to JP6
JP5	1-2	The REF2.5V output of the REF5025 is routed to JP7
JP6	1-2	The output of the JP4 jumper (REF2.5V Default) is routed to the REF_A input of the DAC8728
JP7	1-2	The output of the JP5 jumper (REF2.5V Default) is routed to the REF_B input of the DAC8728
JP8	Closed	Routes the OFFSET_A pin directly to AGND which is required for single-supply operation
JP9	1-2	$\overline{RST}$ is controlled by the 1Y3 output of the SN74LVC139
JP10	3-4	DC_$\overline{CS}$ is set to the 2Y1 output of the SN74LVC139 which is controlled with the A2 and A3 address bits
JP11	Closed	Pulls RSTSEL to GND. Sets the output value to negative full-scale on resets
JP13	Closed	Pulls USB/BTC to GND. Sets the input format for the DAC to straight binary
JP14	2-3	Sets the DAC8728 to unipolar operation by routing the AV_{SS} pin to AGND.
JP15	1-2	Sets the DV_{DD} input to the DAC8728 to +3.3V from pin-10 on the J4 header
JP16	Closed	Routes the OFFSET_B pin directly to AGND which is required for single-supply operation
JP17	1-2	$\overline{LDAC}$ is controlled by the output of the U12 AND gate.
JP18	Open	U12 AND gate is only controlled by LDAC_CTRL from the 2Y3 output of the SN74LVC139
JP19	1-2	+3.3V is routed to JP20
JP20	1-2	The output for the JP19 jumper (3.3V default) is routed to the IOV_{DD} input of the DAC8728.

After confirming that jumpers are installed correctly on the EVM, power can be applied to the board. Power must be applied in this order: IOV_{DD}, then DV_{DD}, then AV_{DD} and AV_{SS}. Even though the EVM incorporates some basic power-supply filtering, a clean, well-regulated power supply is ***required*** to obtain the performance results described in the product data sheet.

Once the EVM is powered, the user can apply the appropriate parallel data and control signals to the EVM using J1 and J6. The DAC8728EVM can also be connected directly to the 5-6k Interface Board for use with a variety of C5000 and C6000 series DSP Starter Kits (DSKs), available from Texas Instruments. The parallel control and data connectors are designed to allow pattern generators and/or logic analyzers to be connected to the EVM using standard ribbon type cables on 0.1” centers.

7.4 Unipolar/Single-Supply Setup (Default)

Follow the configuration given in Table 11 and illustrated in Figure 5 to set up the board for single-supply operation.

NOTE: The OFFSET_A and OFFSET_B pins must be shorted directly to GND for unipolar/single-supply operation.

Table 11. Unipolar/Single-Supply Configuration

Jumper	Position
JP3, JP4, JP5, JP6, JP7, JP9, JP15, JP17, JP19, JP20	1-2
JP14	2-3
JP1, JP2, JP18	Open
JP8, JP16, JP11, JP13	Closed
JP10	3-4

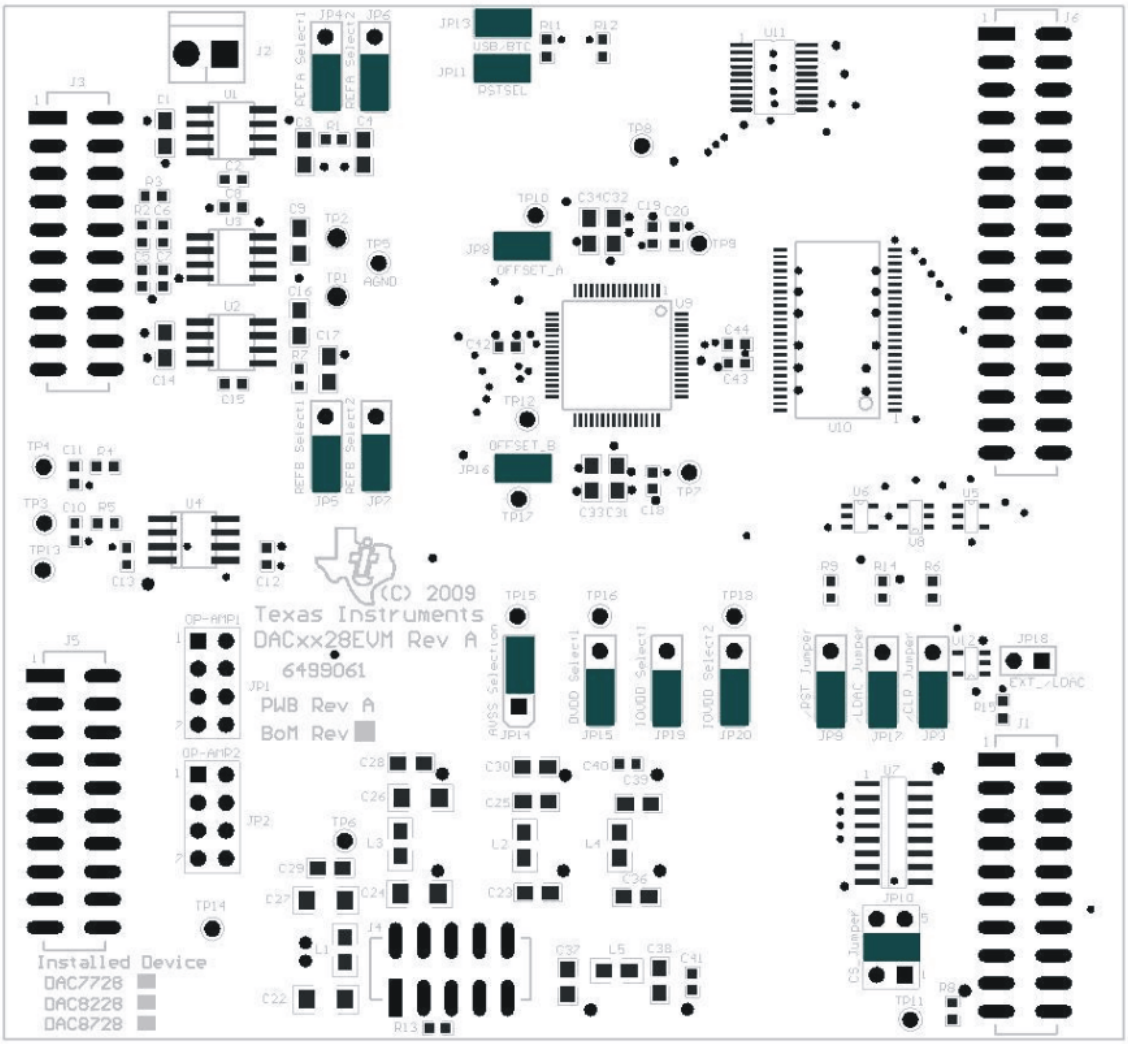


Figure 5. DAC8728EVM Unipolar/Single-Supply Setup

7.5 Bipolar/Dual-Supply Setup

Follow the configuration shown in Table 12 and Figure 6 to set up the board for bipolar/dual-supply operation.

Table 12. Bipolar/Dual-Supply Configuration

Jumper	Position
JP3, JP4, JP5, JP6, JP7, JP9, JP14, JP15, JP17, JP19, JP20,	1-2
JP1, JP2, JP8, JP13, JP16, JP18	Open
JP11	Closed
JP10	3-4

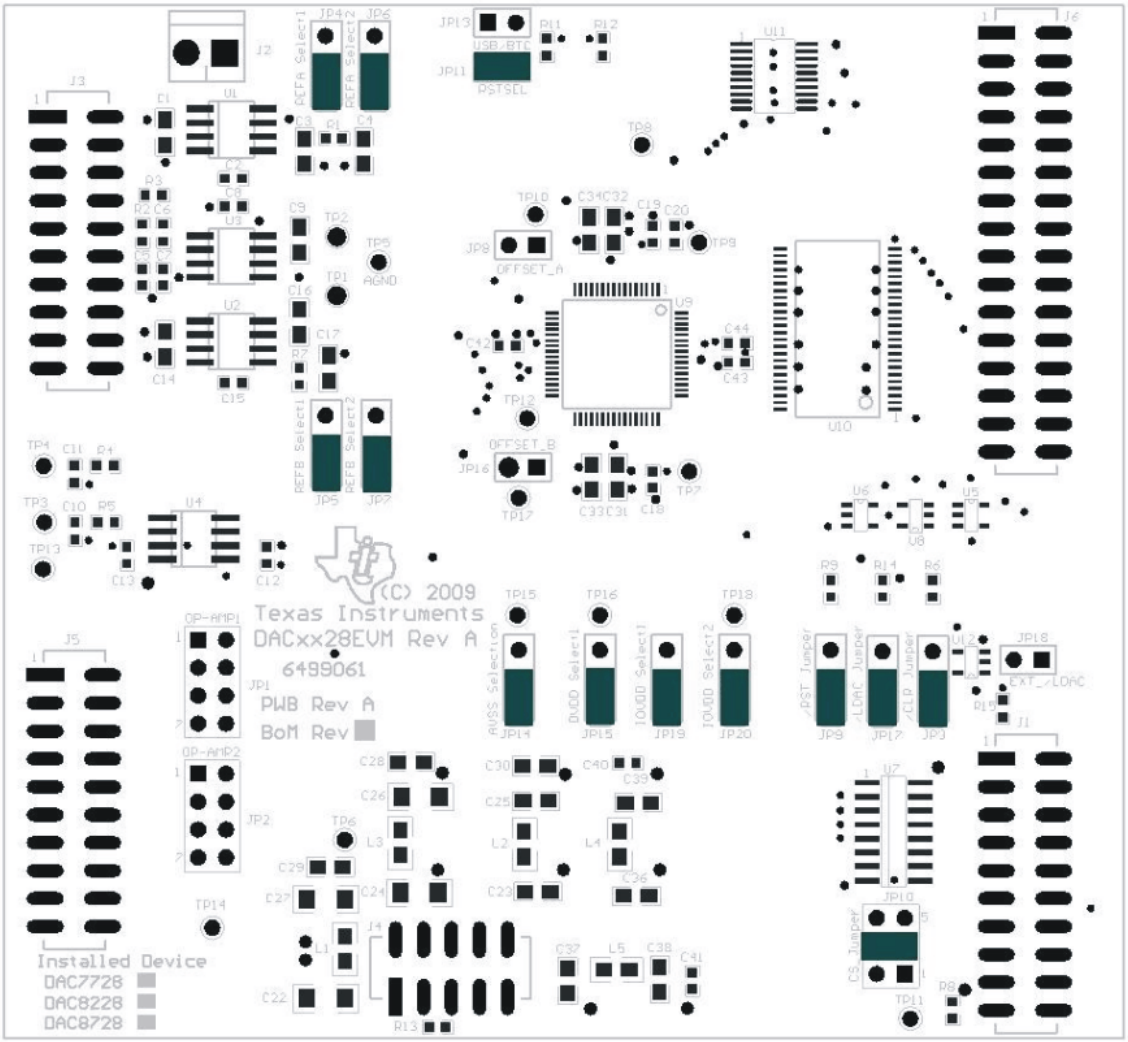


Figure 6. Bipolar/Dual-Supply Configuration

8 Schematics and Layout

Schematics for the DAC8728EVM are appended to this user's guide. The bill of materials is provided in Table 13.

8.1 Bill of Materials

NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see the TI web site.)

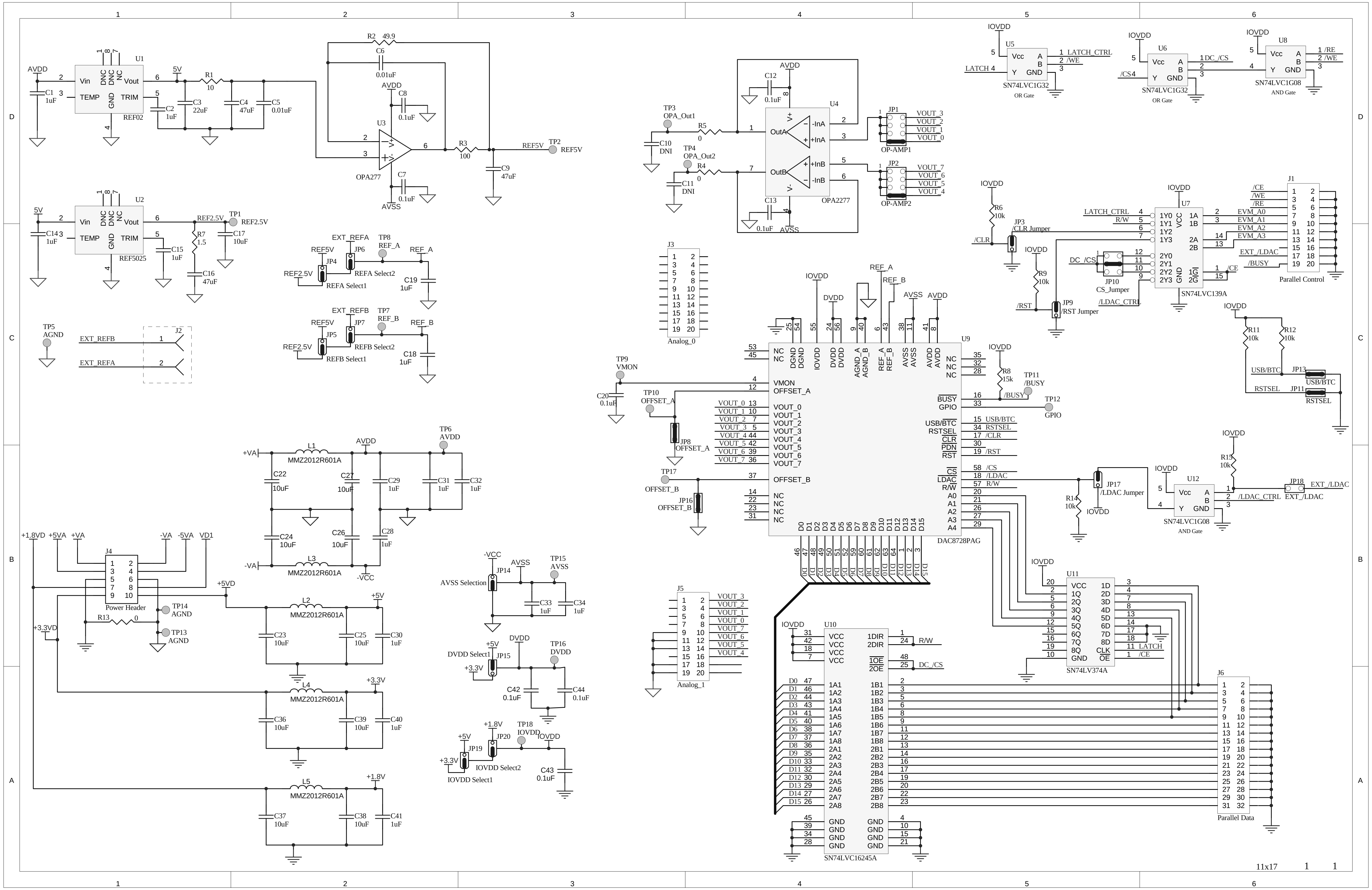
Table 13. DAC8728EVM Bill of Materials[1]

Item No.	Qty	Ref Des [2]	Description	Manufacturer	Mfr Part Number
1	1	N/A	Printed wiring board	TI	6499061
2	9	C1, C14, C28, C29, C30, C31, C32, C33, C34	Capacitor, Ceramic 1μF 50V X7R 0805	MuRata	GRM21BR71H105KA12L
3	6	C2, C15, C18, C19, C40, C41	Capacitor, Ceramic 1.0μF 16V X5R 10% 0603	TDK	C1608X5R1C105K
4	1	C3	Capacitor, Ceramic 22μF 6.3V X5R 20% 0805	TDK	C2012X5R0J226M
5	3	C4, C9, C16	Capacitor, Ceramic 47μF 6.3V X5R 0805	Taiyo Yuden	JMK212BJ476MG-T
6	2	C5, C6	Capacitor, Ceramic 10000pF 50V X7R 10% 0603	TDK	C1608X7R1H103K
7	8	C7, C8, C12, C13, C20, C42, C43, C44	Capacitor, Ceramic 0.10μF 50V X7R 10% 0603	TDK	C1608X7R1H104K
8	0	C10, C11	Do not install		
9	7	C17, C23, C25, C36, C37, C38 , C39	Capacitor, Ceramic 10μF 16V X5R 0805	Taiyo Yuden	EMK212BJ106KG-T
10	4	C22, C24, C26, C27	Capacitor, Ceramic 10μF 50V X7S 1210	Taiyo Yuden	UMK325C7106MM-T
11	3	J1, J3, J5 Top	20-pin header	Samtec	TSM-110-01-T-DV
12	3	J1, J3, J5 Bottom	20-pin socket	Samtec	SSW-110-22-S-D-VS
13	1	J2	TERMINAL BLOCK 3.5MM 2POS PCB	On Shore	ED555/2DS
14	1	J4 Top	10-pin header	Samtec	TSM-105-01-T-DV
15	1	J4 Bottom	10-pin socket	Samtec	SSW-105-22-S-D-VS
16	1	J6 Top	32-pin header	Samtec	TSM-116-01-T-DV
17	1	J6 Bottom	32-pin socket	Samtec	SSW-116-22-S-D-VS
18	2	JP1, JP2	2-position, dual row header	Samtec	TSW-104-22-T-D
19	11	JP3, JP4, JP5, JP6, JP7, JP9, JP14, JP15, JP17, JP19, JP20	3-position header	Samtec	TSW-103-22-T-S
20	5	JP8, JP11, JP13, JP16, JP18	2-position header	Samtec	TSW-102-22-T-S
21	1	JP10	3-position, dual row header	Samtec	TSW-103-22-T-D
22	5	L1 - L5	Ferrite bead	TDK	MMZ2012R601A
23	1	R1	Resistor, 10.0Ω 1/10W 1% 0603 SMD	Yageo	RC0603FR-0710RL
24	1	R2	Resistor, 49.9Ω 1/10W 1% 0603 SMD	Yageo	RC0603FR-0749R9L
25	1	R3	Resistor, 100Ω 1/10W 1% 0603 SMD	Yageo	RC0603FR-07100RL
26	1	R4, R5, R13	Resistor, 0.0Ω 1/10W 5% 0603 SMD	Yageo	RC0603JR-070RL
27	6	R6, R9, R11, R12, R14, R15	Resistor, 10.0kΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-0710KL
28	1	R7	Resistor, 1.5Ω 1/10W 5% 0603 SMD	Yageo	RC0603JR-071R5L
29	1	R8	Resistor, 15.0kΩ 1/10W 1% 0603 SMD	Yageo	RC0603FR-0715KL

(1) Manufacturer and part number for items may be substituted with electrically equivalent items.
(2) Reference designators C21, C35, and JP12 are not used.

Table 13. DAC8728EVM Bill of Materials[1] (continued)

Item No.	Qty	Ref Des [2]	Description	Manufacturer	Mfr Part Number
30	15	TP1-TP4, TP6 - TP12, TP15-TP18	Test Point: sSingle .025 Pin, Red	Keystone	5000
31	3	TP5, TP13, TP14	Test Point: single .025 Pin, Black	Keystone	5001
32	1	U1	5V Reference 8-SOP	TI	REF02BU
33	1	U2	2.5V Reference 8-SOP	TI	REF5025ID
34	1	U3	Precision Op-Amp 8-SOP	TI	OPA227UA
35	1	U4	Dual Precision Op-Amp 8-SOP	TI	OPA2277U
36	2	U5, U6	Little Logic OR Gate SOT23 - 5	TI	SN74LVC1G32DBV
37	1	U7	Dual 2-4 Line Decoder 16-SOP	TI	SN74LVC139AD
38	2	U8, U12	Little Logic AND Gate SOT23 - 5	TI	SN74LVC1G08DBV
39	1	U9	Octal DAC 64-TQFP(PAG)	TI	DAC8728SPAG
40	1	U10	16-Bit Buffer/Driver 48-SSOP	TI	SN74LVC16245ADL
41	1	U11	Octal Edge Triggered D-FF 20-TSSOP	TI	SN74LV374ADB
Additional Components					
42	6	N/A	0.100 Shunt, Black	Samtec	SNT-100-BK-T



REF02
REF5025
OPA277
OPA2277
DAC8728PAG
SN74LVC1G32
OR Gate
SN74LVC1G08
AND Gate
SN74LVC139A
SN74LV374A
SN74LVC16245A
Parallel Control
Parallel Data
Power Header
Analog_0
Analog_1
OP-AMP1
OP-AMP2
MMZ2012R601A
REFA Select1
REFA Select2
REFB Select1
REFB Select2
AVSS Selection
DVDD Select1
IOVDD Select1
IOVDD Select2
CS_Jumper
/CLR Jumper
/RST Jumper
/LDAC Jumper
OFFSET_A
OFFSET_B
USB/BTC
RSTSEL
EXT_/LDAC
EXT_REFA
EXT_REFB
REF5V
REF2.5V
REF_A
REF_B
AVDD
AVSS
DVDD
IOVDD
11x17

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of –16.5V to +21V and the output voltage range of –15V to +15V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +30° C. The EVM is designed to operate properly with certain components above +60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265