

SNx4AHCT245 Octal Bus Transceivers With 3-State Outputs

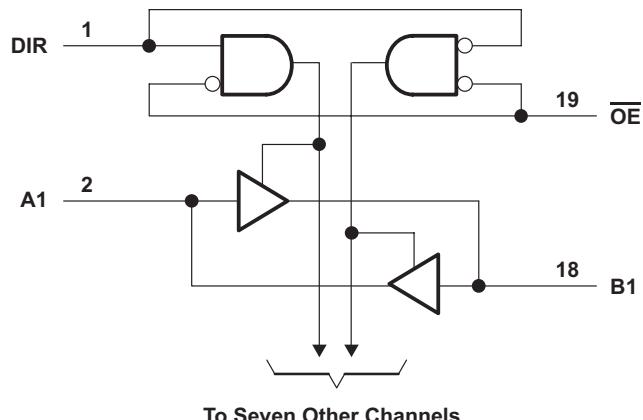
1 Features

- Inputs Are TTL-Voltage Compatible
 - Latch-Up Performance Exceeds 250 mA Per JESD 17
 - ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
 - On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Servers
 - PCs and Notebooks
 - Network Switches
 - Wearable Health and Fitness Devices
 - Telecom Infrastructures
 - Electronic Points of Sale

4 Simplified Schematic



3 Description

The SNx4AHCT245 octal bus transceivers are designed for asynchronous two-way communication between data buses. These parts operate from 4.5 V to 5.5 V.

Device Information⁽¹⁾

| DEVICE INFORMATION | | |
|--------------------|------------|-----------------|
| Part Number | Package | Body Size (Nom) |
| SNx4AHCT245 | PDIP (20) | 25.40 x 6.35 mm |
| | SOP (20) | 12.60 x 5.30 mm |
| | SSOP (20) | 7.50 x 5.30 mm |
| | TVSOP (20) | 5.00 x 4.40 mm |
| | SOIC (20) | 12.80 x 7.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

| | | | | | |
|----------|--|----------|-----------|---|-----------|
| 1 | Features | 1 | 9.1 | Overview | 8 |
| 2 | Applications | 1 | 9.2 | Functional Block Diagram | 8 |
| 3 | Description | 1 | 9.3 | Feature Description | 8 |
| 4 | Simplified Schematic | 1 | 9.4 | Device Functional Modes | 8 |
| 5 | Revision History | 2 | 10 | Application and Implementation | 9 |
| 6 | Pin Configuration and Functions | 3 | 10.1 | Application Information | 9 |
| 7 | Specifications | 4 | 10.2 | Typical Application | 9 |
| 7.1 | Absolute Maximum Ratings | 4 | 11 | Power Supply Recommendations | 10 |
| 7.2 | Handling Ratings | 4 | 12 | Layout | 10 |
| 7.3 | Recommended Operating Conditions | 4 | 12.1 | Layout Guidelines | 10 |
| 7.4 | Thermal Information | 5 | 12.2 | Layout Example | 10 |
| 7.5 | Electrical Characteristics | 5 | 13 | Device and Documentation Support | 11 |
| 7.6 | Switching Characteristics | 6 | 13.1 | Related Links | 11 |
| 7.7 | Noise Characteristics | 6 | 13.2 | Trademarks | 11 |
| 7.8 | Operating Characteristics | 6 | 13.3 | Electrostatic Discharge Caution | 11 |
| 7.9 | Typical Characteristics | 6 | 13.4 | Glossary | 11 |
| 8 | Parameter Measurement Information | 7 | 14 | Mechanical, Packaging, and Orderable Information | 11 |
| 9 | Detailed Description | 8 | | | |

5 Revision History

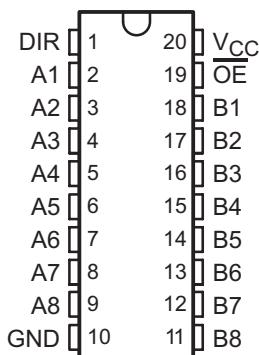
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision O (August 2013) to Revision P | Page |
|--|-------------|
| • Updated document to new TI data sheet format. | 1 |
| • Added Military Disclaimer to Features list. | 1 |
| • Added Applications. | 1 |
| • Added Pin Functions table. | 3 |
| • Added Handling Ratings table. | 4 |
| • Added Thermal Information table. | 5 |
| • Added Typical Characteristics. | 6 |
| • Added Detailed Description section. | 8 |
| • Added Application and Implementation section. | 9 |

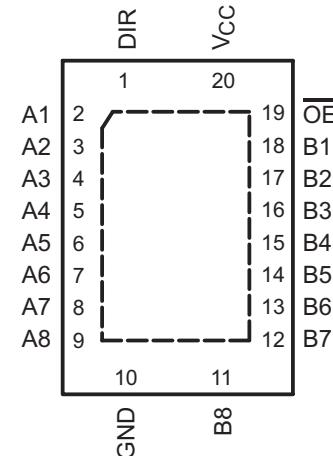
| Changes from Revision N (March 2005) to Revision O | Page |
|---|-------------|
| • Removed Ordering Information table. | 1 |
| • Extended operating temperature range to 125°C. | 4 |

6 Pin Configuration and Functions

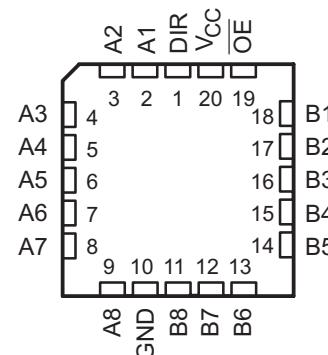
SN54AHCT245 . . . J OR W PACKAGE
SN74AHCT245 . . . DB, DGV, DW, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74AHCT245 . . . RGY PACKAGE
(TOP VIEW)



SN54AHCT245 . . . FK PACKAGE
(TOP VIEW)



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|------|-----|-----------------|
| NO. | NAME | | |
| 1 | DIR | — | Direction Pin |
| 2 | A1 | I/O | A1 Input/Output |
| 3 | A2 | I/O | A2 Input/Output |
| 4 | A3 | I/O | A3 Input/Output |
| 5 | A4 | I/O | A4 Input/Output |
| 6 | A5 | I/O | A5 Input/Output |
| 7 | A6 | I/O | A6 Input/Output |
| 8 | A7 | I/O | A7 Input/Output |
| 9 | A8 | I/O | A8 Input/Output |
| 10 | GND | — | Ground Pin |
| 11 | B8 | I/O | B8 Input/Output |
| 12 | B7 | I/O | B7 Input/Output |
| 13 | B6 | I/O | B6 Input/Output |
| 14 | B5 | I/O | B5 Input/Output |
| 15 | B4 | I/O | B4 Input/Output |
| 16 | B3 | I/O | B3 Input/Output |
| 17 | B2 | I/O | B2 Input/Output |
| 18 | B1 | I/O | B1 Input/Output |
| 19 | OE | I | Output Enable |
| 20 | VCC | — | Power Pin |

7 Specifications

7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|--|---|----------------|------|----------------|------|
| V_{CC} | Supply voltage range | | -0.5 | 7 | V |
| V_I | Input voltage range ⁽²⁾ | Control inputs | -0.5 | 7 | V |
| V_O | Output voltage range ⁽²⁾ | | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current $V_I < 0$ | Control inputs | | -20 | mA |
| I_{OK} | Output clamp current $V_O < 0$ or $V_O > V_{CC}$ | | | ± 20 | mA |
| I_O | Continuous output current $V_O = 0$ to V_{CC} | | | ± 25 | mA |
| Continuous current through V_{CC} or GND | | | | ± 75 | mA |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|-------------|---------------------------|--|-----|------|------|
| T_{stg} | Storage temperature range | | -65 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 0 | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 0 | 1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | SN54AHCT245 | | SN74AHCT245 | | UNIT |
|---------------------|-------------------------------------|-------------|----------|-------------|----------|------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level Input voltage | | 0.8 | | 0.8 | V |
| V_I | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V_O | Output voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | | -8 | | -8 | mA |
| I_{OL} | Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ | Input Transition rise and fall rate | | 20 | | 20 | ns/V |
| T_A | Operating free-air temperature | -55 | 125 | -40 | 125 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN74AHCT245 | | | | | | | UNIT |
|-------------------------------|--|------|-------|------|------|------|-------|------|
| | DB | DGV | DW | N | NS | PW | RGY | |
| | 20 PINS | | | | | | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 96.0 | 116.1 | 79.8 | 51.5 | 77.1 | 102.8 | 35.1 |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 57.7 | 31.3 | 45.8 | 38.2 | 43.6 | 36.8 | 43.3 |
| R _{θJB} | Junction-to-board thermal resistance | 51.2 | 57.6 | 47.4 | 32.4 | 44.6 | 53.8 | 12.9 |
| Ψ _{JT} | Junction-to-top characterization parameter | 19.4 | 1.0 | 18.5 | 24.6 | 17.2 | 2.5 | 0.9 |
| Ψ _{JB} | Junction-to-board characterization parameter | 50.8 | 56.9 | 47.0 | 32.3 | 44.2 | 53.3 | 12.9 |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | n/a | n/a | n/a | 7.9 |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54AHCT245 –55°C TO 125°C | | SN74AHCT245 –40°C TO 85°C | | Recommended SN74AHCT245 –40°C TO 125°C | | |
|---------------------------------|------------------------------|---|-----------------------|------|------|-------------------------------|-------------------|------------------------------|------|--|------|----|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = –50 µA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | 4.4 | | V |
| | I _{OH} = –8 mA | | 3.94 | | | 3.8 | | 3.8 | | 3.7 | | |
| V _{OL} | I _{OL} = 50 µA | 4.5 V | | 0.1 | | 0.1 | | 0.1 | | 0.1 | | V |
| | I _{OH} = 8 mA | | | 0.36 | | 0.44 | | 0.44 | | 0.44 | | |
| I _I | OE or DIR | V _I = 5.5 V or GND | 0 to 5.5 V | | ±0.1 | | ±1 ⁽¹⁾ | | ±1 | | ±1 | µA |
| I _{OZ} | A or B inputs ⁽²⁾ | V _O = V _{CC} or GND | 5.5 V | | ±.25 | | ±2.5 | | ±2.5 | | ±2.5 | µA |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | 4 | | 40 | | 40 | | 40 | µA |
| ΔI _{CC} ⁽³⁾ | | One input at 3.4 V, Other inputs at V _{CC} or GND | 5.5 V | | 1.35 | | 1.5 | | 1.5 | | 1.5 | mA |
| C _i | OE or DIR | V _I = V _{CC} or GND | 5 V | 2.5 | 10 | | | 10 | | | | pF |
| C _{io} | A or B inputs | V _I = V _{CC} or GND | 5 V | | 4 | | | | | | | pF |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(3) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

7.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see [Figure 2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | SN54AHCT245 –55°C TO 125°C | | SN74AHCT245 –40°C TO 85°C | | Recommended SN74AHCT245 –40°C TO 125°C | | UNIT |
|-------------|-----------------|----------------|-----------------------|--------------------------|---------------------|-------------------------------|---------------------|------------------------------|------|--|------|------|
| | | | | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A or B | B or A | $C_L = 15 \text{ pF}$ | 4.5 ⁽¹⁾ | 7.7 ⁽¹⁾ | 1 ⁽¹⁾ | 10 ⁽¹⁾ | 1 | 8.5 | 1 | 10 | ns |
| t_{PHL} | | | | 4.5 ⁽¹⁾ | 7.7 ⁽¹⁾ | 1 ⁽¹⁾ | 10 ⁽¹⁾ | 1 | 8.5 | 1 | 10 | |
| t_{PZH} | \overline{OE} | A or B | $C_L = 15 \text{ pF}$ | 8.9 ⁽¹⁾ | 13.8 ⁽¹⁾ | 1 ⁽¹⁾ | 16 ⁽¹⁾ | 1 | 15 | 1 | 16 | ns |
| t_{PZL} | | | | 8.9 ⁽¹⁾ | 13.8 ⁽¹⁾ | 1 ⁽¹⁾ | 16 ⁽¹⁾ | 1 | 15 | 1 | 16 | |
| t_{PHZ} | \overline{OE} | A or B | $C_L = 15 \text{ pF}$ | 9.2 ⁽¹⁾ | 14.4 ⁽¹⁾ | 1 ⁽¹⁾ | 16.5 ⁽¹⁾ | 1 | 15.5 | 1 | 16.5 | ns |
| t_{PLZ} | | | | 9.2 ⁽¹⁾ | 14.4 ⁽¹⁾ | 1 ⁽¹⁾ | 16.5 ⁽¹⁾ | 1 | 15.5 | 1 | 16.5 | |
| t_{PLH} | A or B | B or A | $C_L = 50 \text{ pF}$ | 5.3 | 8.7 | 1 | 11 | 1 | 9.5 | 1 | 11 | ns |
| t_{PHL} | | | | 5.3 | 8.7 | 1 | 11 | 1 | 9.5 | 1 | 11 | |
| t_{PZH} | \overline{OE} | A or B | $C_L = 50 \text{ pF}$ | 9.7 | 14.8 | 1 | 17 | 1 | 16 | 1 | 17 | ns |
| t_{PZL} | | | | 9.7 | 14.8 | 1 | 17 | 1 | 16 | 1 | 17 | |
| t_{PHZ} | \overline{OE} | A or B | $C_L = 50 \text{ pF}$ | 10 | 15.4 | 1 | 17.5 | 1 | 16.5 | 1 | 17.5 | ns |
| t_{PLZ} | | | | 10 | 15.4 | 1 | 17.5 | 1 | 16.5 | 1 | 17.5 | |
| $t_{sk(o)}$ | | | $C_L = 50 \text{ pF}$ | | 1 ⁽²⁾ | | | | 1 | | | ns |

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

7.7 Noise Characteristics

 $V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

| PARAMETER | SN74AHCT245 | | | UNIT |
|-------------|-------------|-----|-----|------|
| | MIN | TYP | MAX | |
| $V_{OH(V)}$ | 4 | | | V |
| $V_{IH(D)}$ | 2 | | | V |
| $V_{IL(D)}$ | 0.8 | | | V |

- (1) Characteristics are for surface-mount packages only.

7.8 Operating Characteristics

 $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----------|---|-----|------|
| C_{pd} | Power dissipation capacitance No load, $f = 1 \text{ MHz}$ | 13 | pF |

7.9 Typical Characteristics

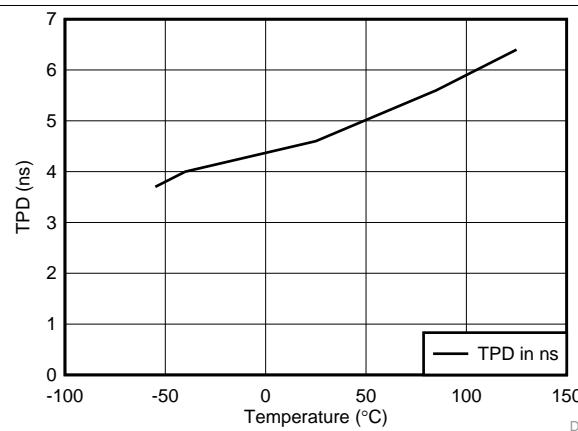
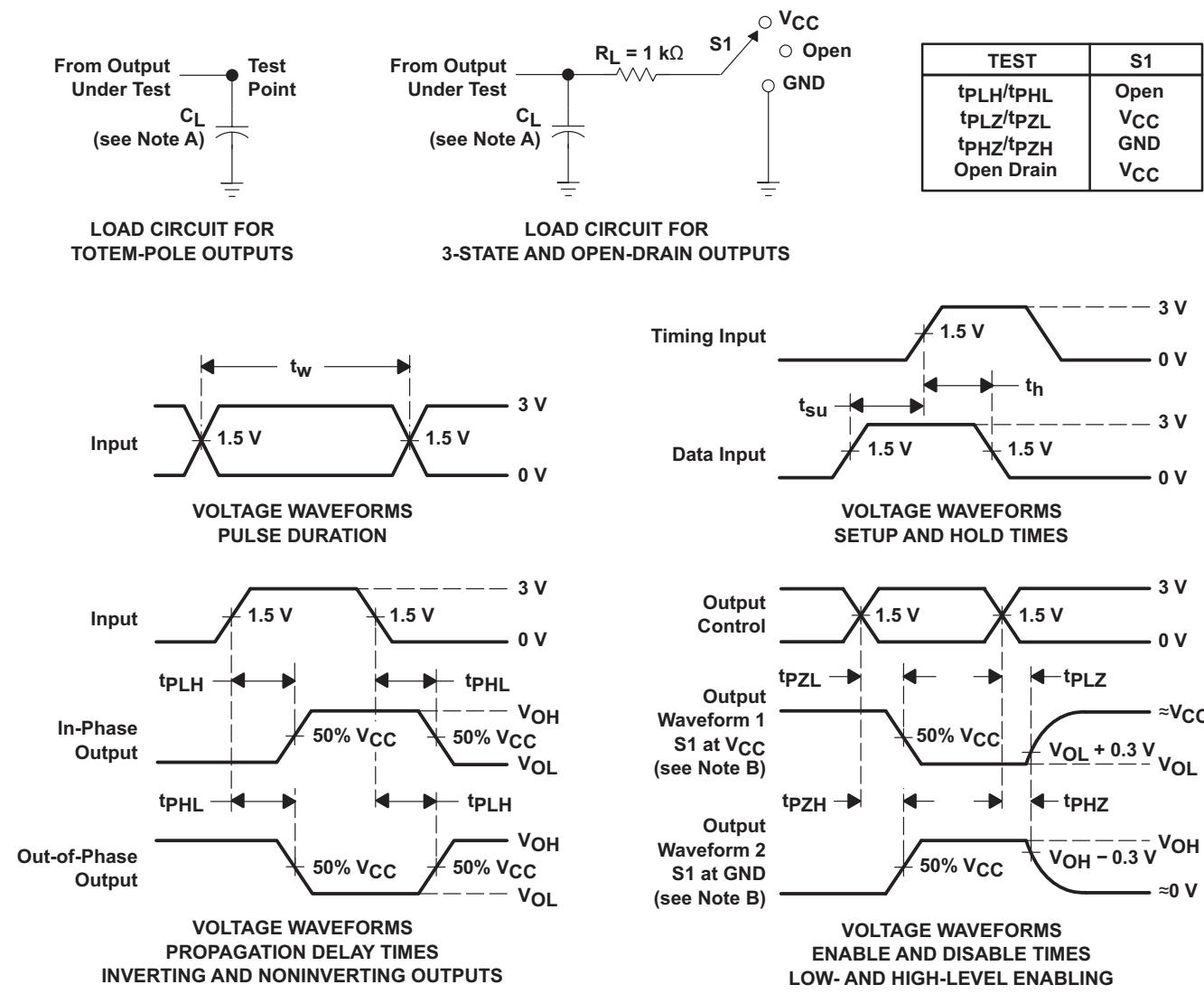


Figure 1. SN74AHCT245 TPD vs Temperature, 15 pF Load

8 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SNx7ACHT245 octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements. The SNx4AHCT245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses effectively are isolated. To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

9.2 Functional Block Diagram

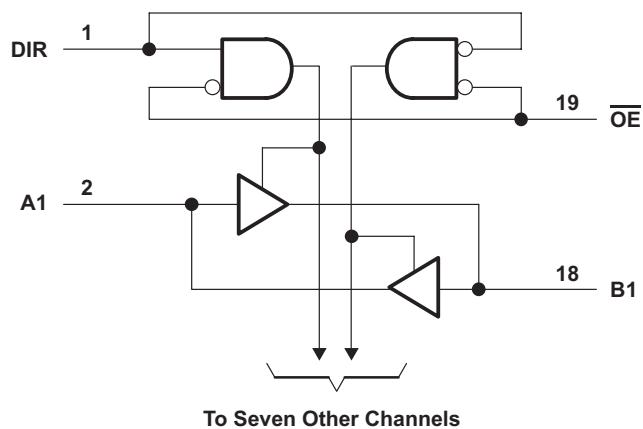


Figure 3. Logic Diagram (Positive Logic)

9.3 Feature Description

- V_{CC} is optimized at 5 V
- Allows up voltage translation from 3.3 V to 5 V
 - Inputs Accept V_{IH} levels of 2 V
- Slow edge rates minimize output ringing

9.4 Device Functional Modes

Table 1. Function Table
(Each Transceiver)

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

10 Application and Implementation

10.1 Application Information

The SN74AHCT245 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8 V V_{IL} and 2 V V_{IH} . This feature makes it ideal for translating up from 3.3 V to 5 V. The figure below shows this type of translation.

10.2 Typical Application

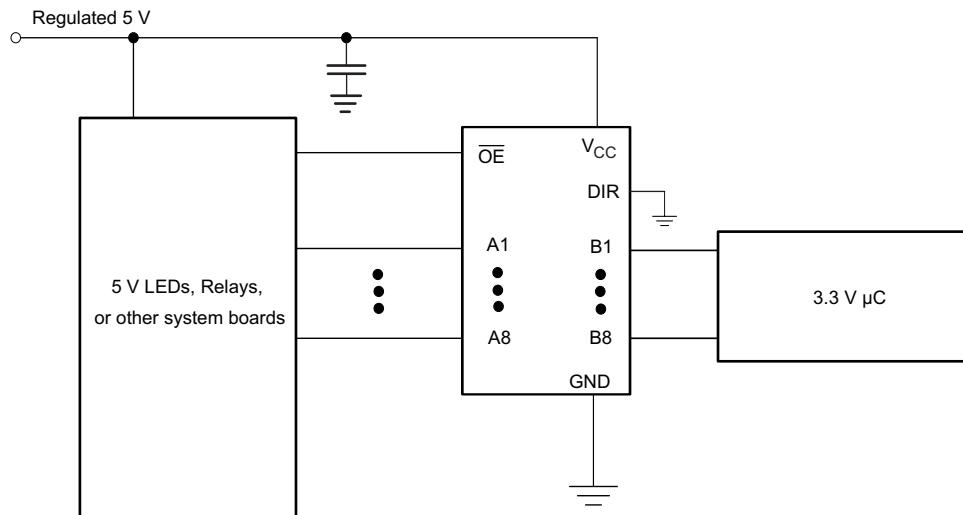


Figure 4. Typical Application Diagram

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

- Recommended input conditions
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
- Recommend output conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part
 - Outputs should not be pulled above V_{CC}

Typical Application (continued)

10.2.3 Application Curves

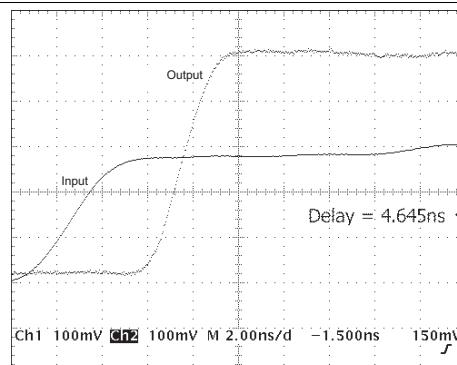


Figure 5. Typical Application Curve

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended; if there are multiple VCC pins, then 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and a 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. **Figure 6** specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

12.2 Layout Example

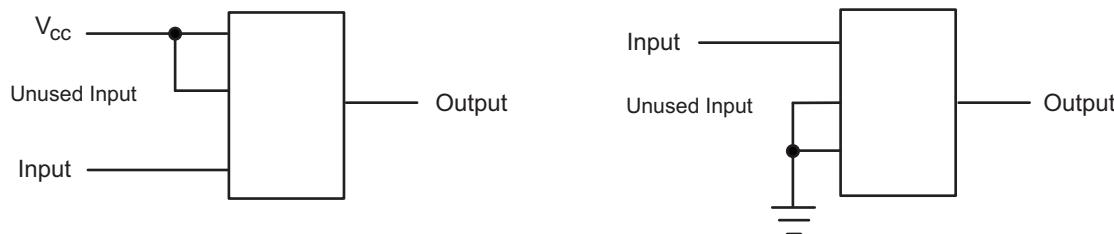


Figure 6. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54AHCT245 | Click here |
| SN74AHCT245 | Click here |

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022 — TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|--------------------------------------|----------------------|--------------|---|---|
| 5962-9681901Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9681901Q2A SNJ54AHCT 245FK | Samples |
| 5962-9681901QRA | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9681901QR A SNJ54AHCT245J | Samples |
| 5962-9681901QSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9681901QS A SNJ54AHCT245W | Samples |
| SN74AHCT245DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB245 | Samples |
| SN74AHCT245DBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB245 | Samples |
| SN74AHCT245DGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB245 | Samples |
| SN74AHCT245DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT245 | Samples |
| SN74AHCT245DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT245 | Samples |
| SN74AHCT245N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | -40 to 125 | SN74AHCT245N | Samples |
| SN74AHCT245NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT245 | Samples |
| SN74AHCT245PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB245 | Samples |
| SN74AHCT245PWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB245 | Samples |
| SN74AHCT245PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | HB245 | Samples |
| SN74AHCT245PWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB245 | Samples |
| SN74AHCT245PWRG3 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | HB245 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|--------------------------------------|----------------------|--------------|---|-------------------------|
| SN74AHCT245PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB245 | Samples |
| SN74AHCT245RGYR | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HB245 | Samples |
| SNJ54AHCT245FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9681901Q2A SNJ54AHCT 245FK | Samples |
| SNJ54AHCT245J | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9681901QR A SNJ54AHCT245J | Samples |
| SNJ54AHCT245W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9681901QS A SNJ54AHCT245W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHCT245, SN74AHCT245 :

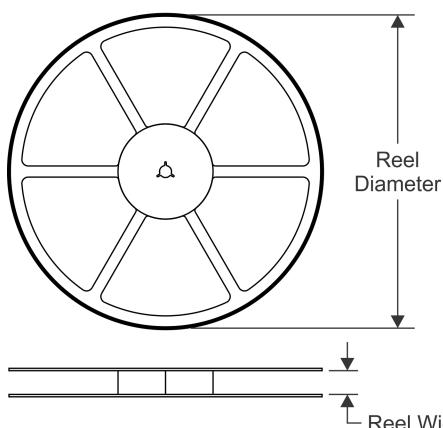
- Catalog: [SN74AHCT245](#)
- Military: [SN54AHCT245](#)

NOTE: Qualified Version Definitions:

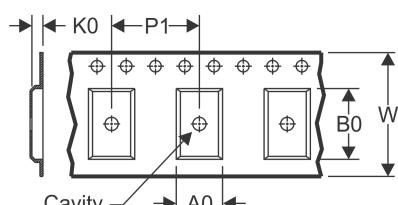
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

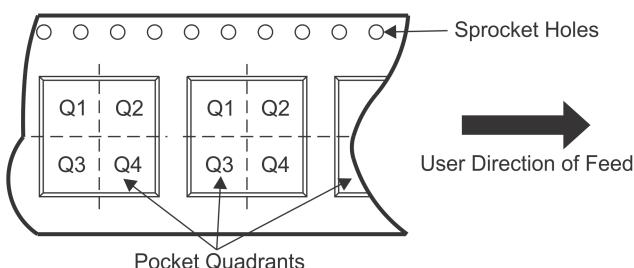


TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHCT245DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHCT245DGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHCT245DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHCT245NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AHCT245PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AHCT245PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74AHCT245PWRG3 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74AHCT245PWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AHCT245RGYR | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.8 | 4.8 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

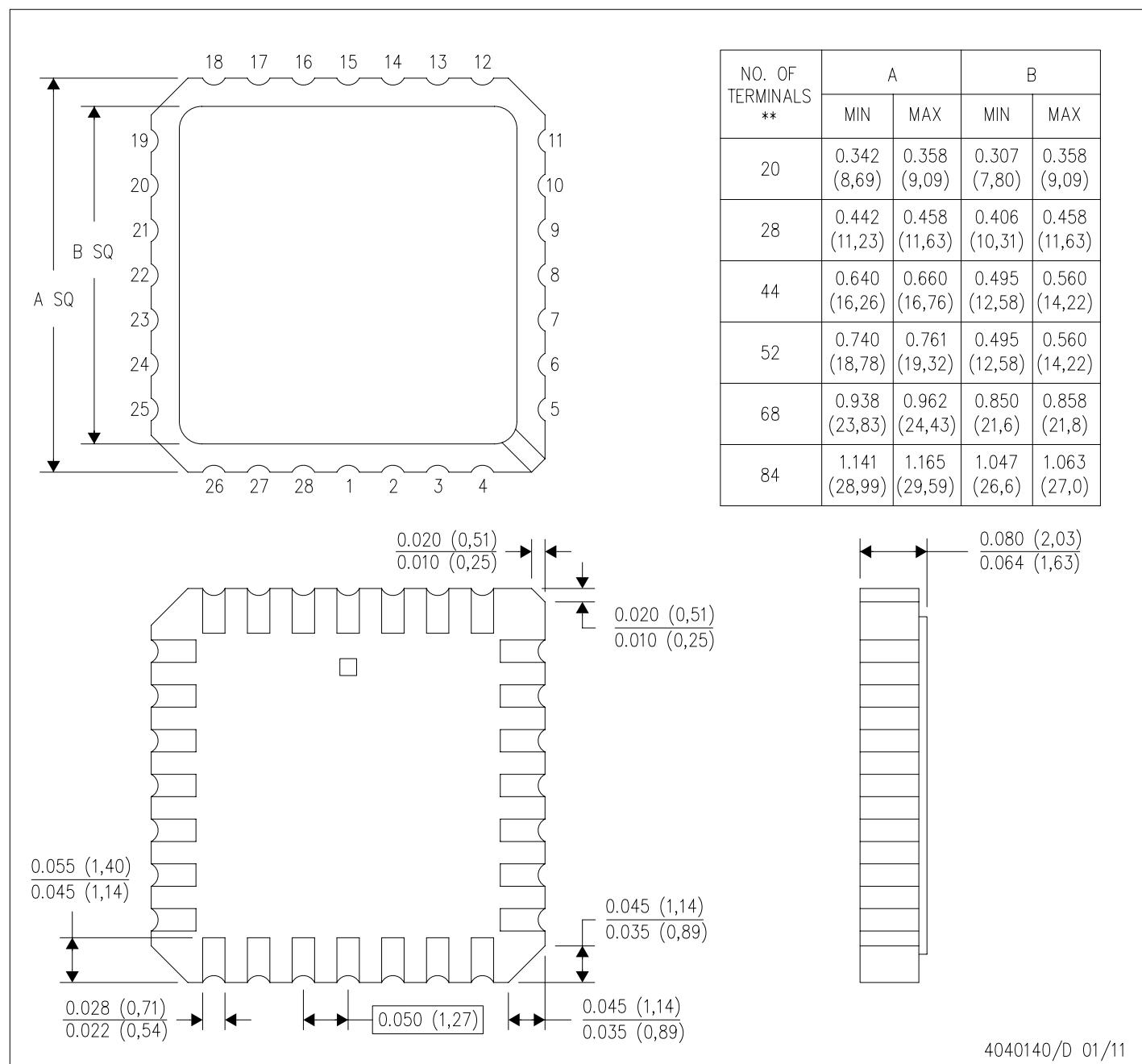

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHCT245DBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AHCT245DGVR | TVSOP | DGV | 20 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74AHCT245DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHCT245NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHCT245PWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AHCT245PWR | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74AHCT245PWRG3 | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74AHCT245PWRG4 | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AHCT245RGYR | VQFN | RGY | 20 | 3000 | 367.0 | 367.0 | 35.0 |

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. Falls within JEDEC MS-004

4040140/D 01/11

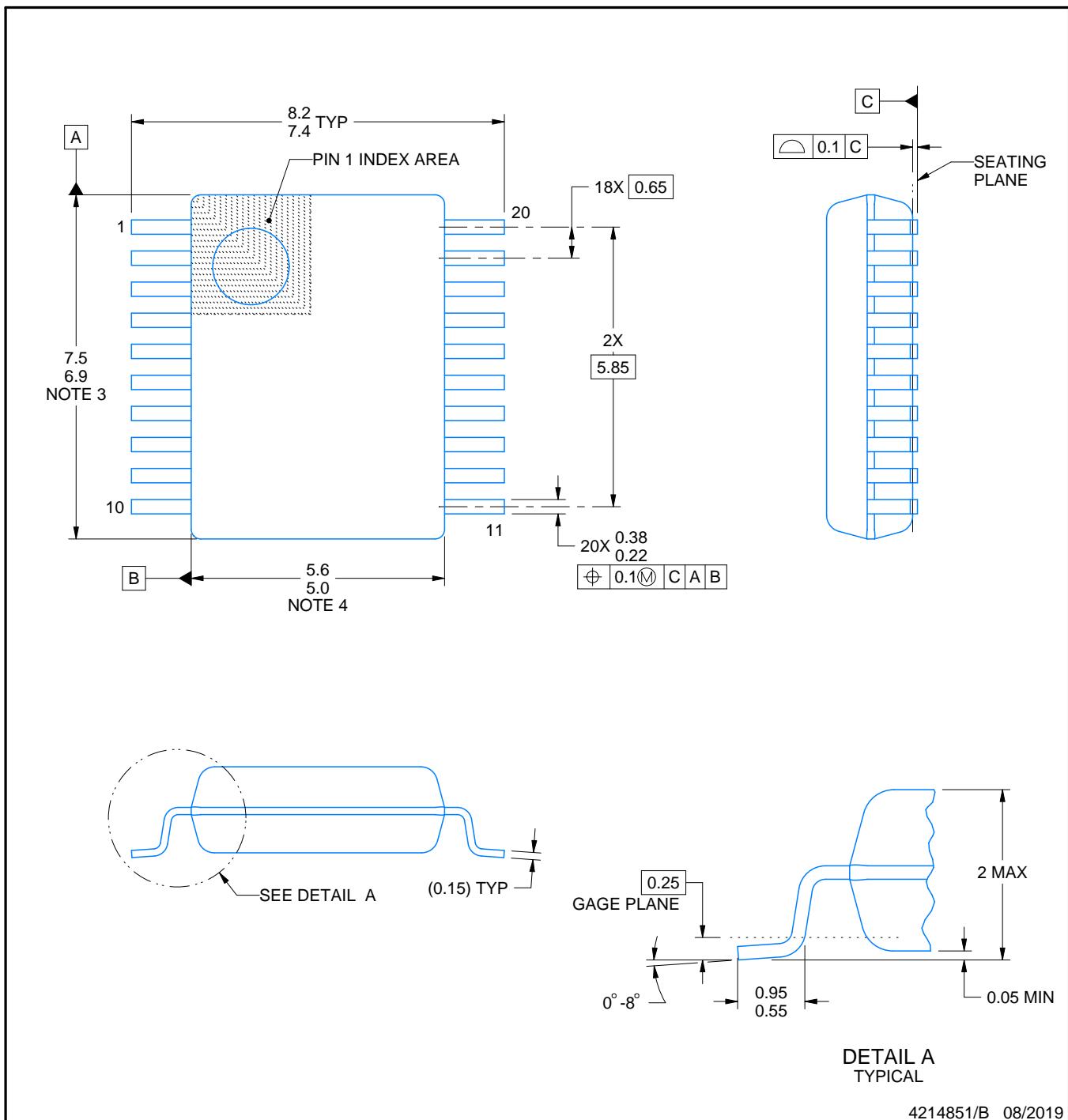
PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

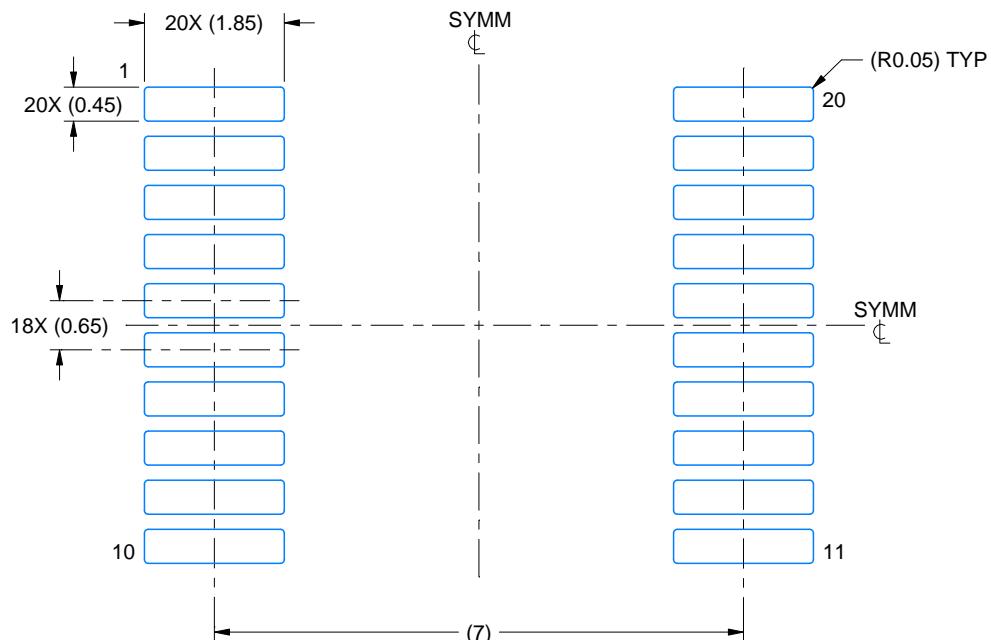
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

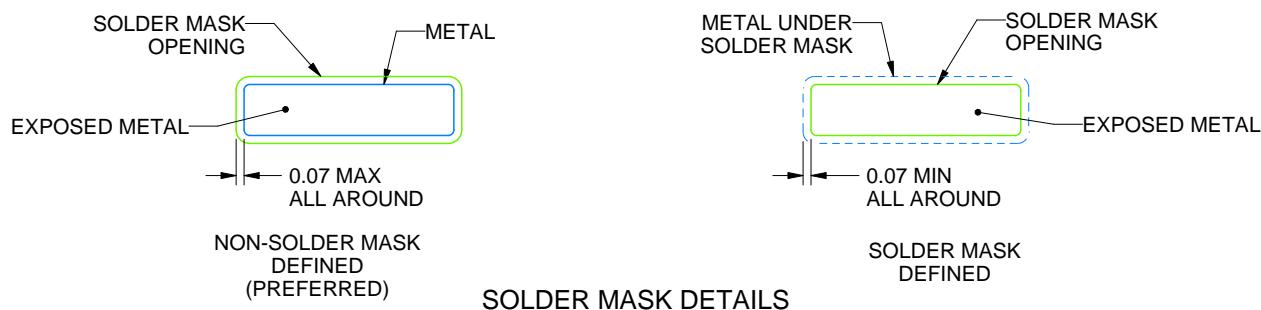
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

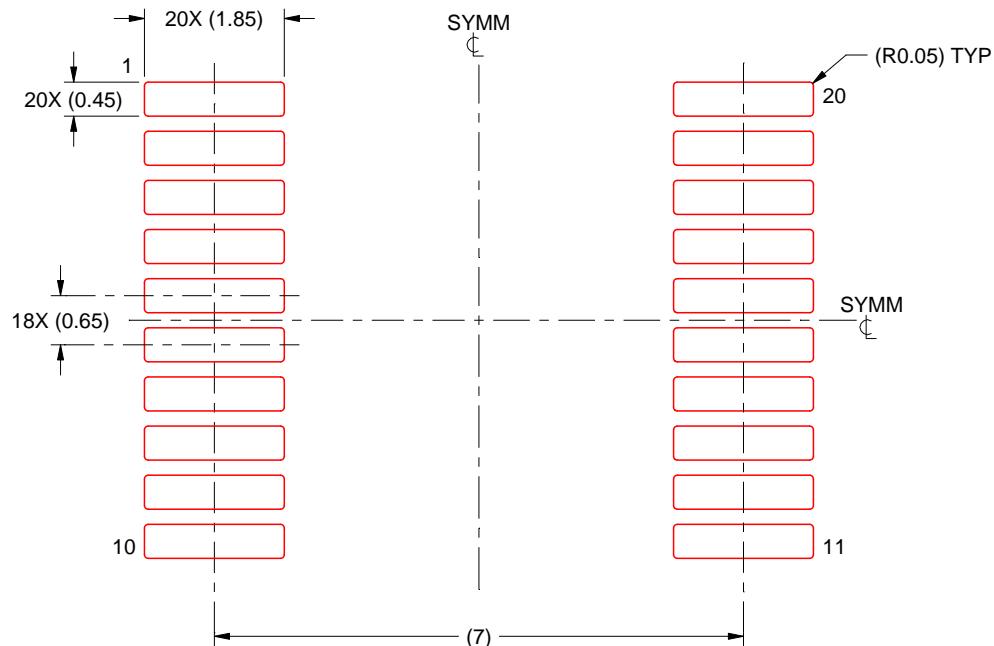
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

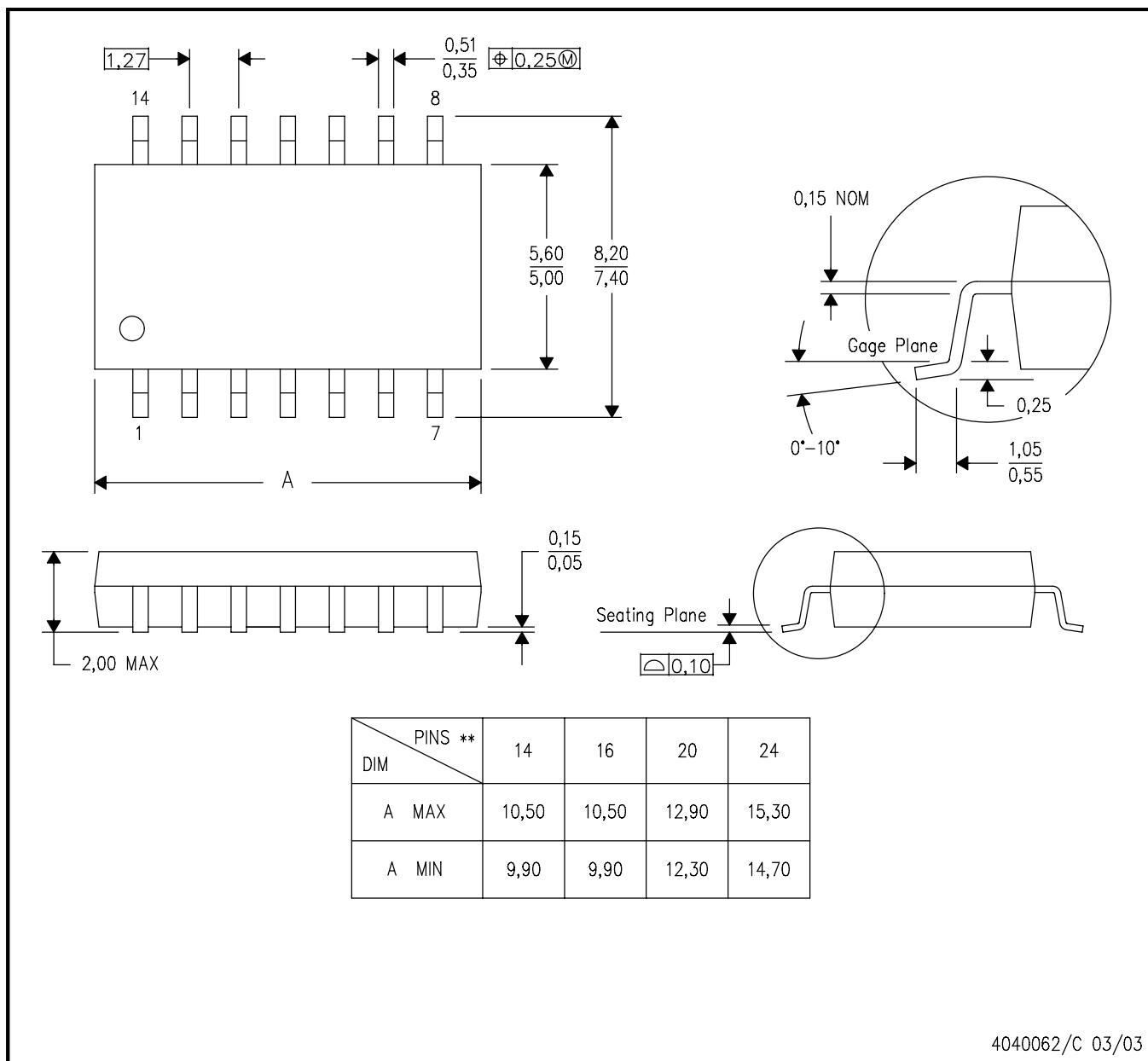
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



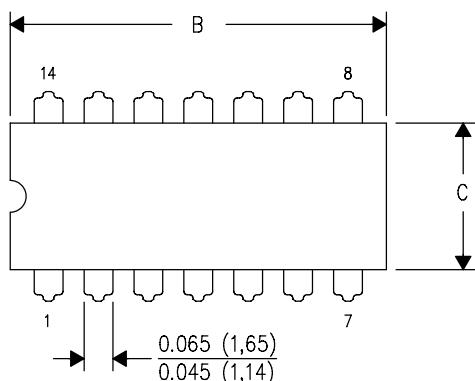
4040062/C 03/03

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

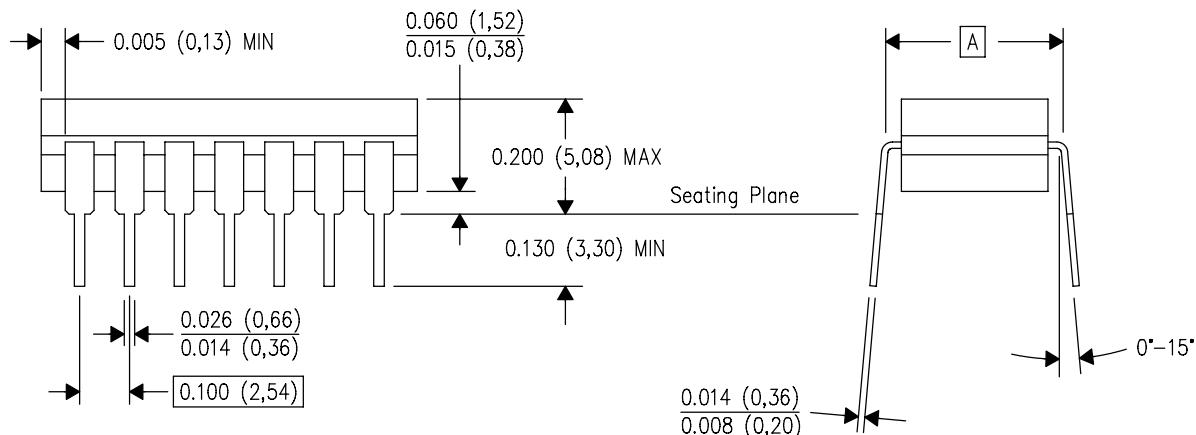
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



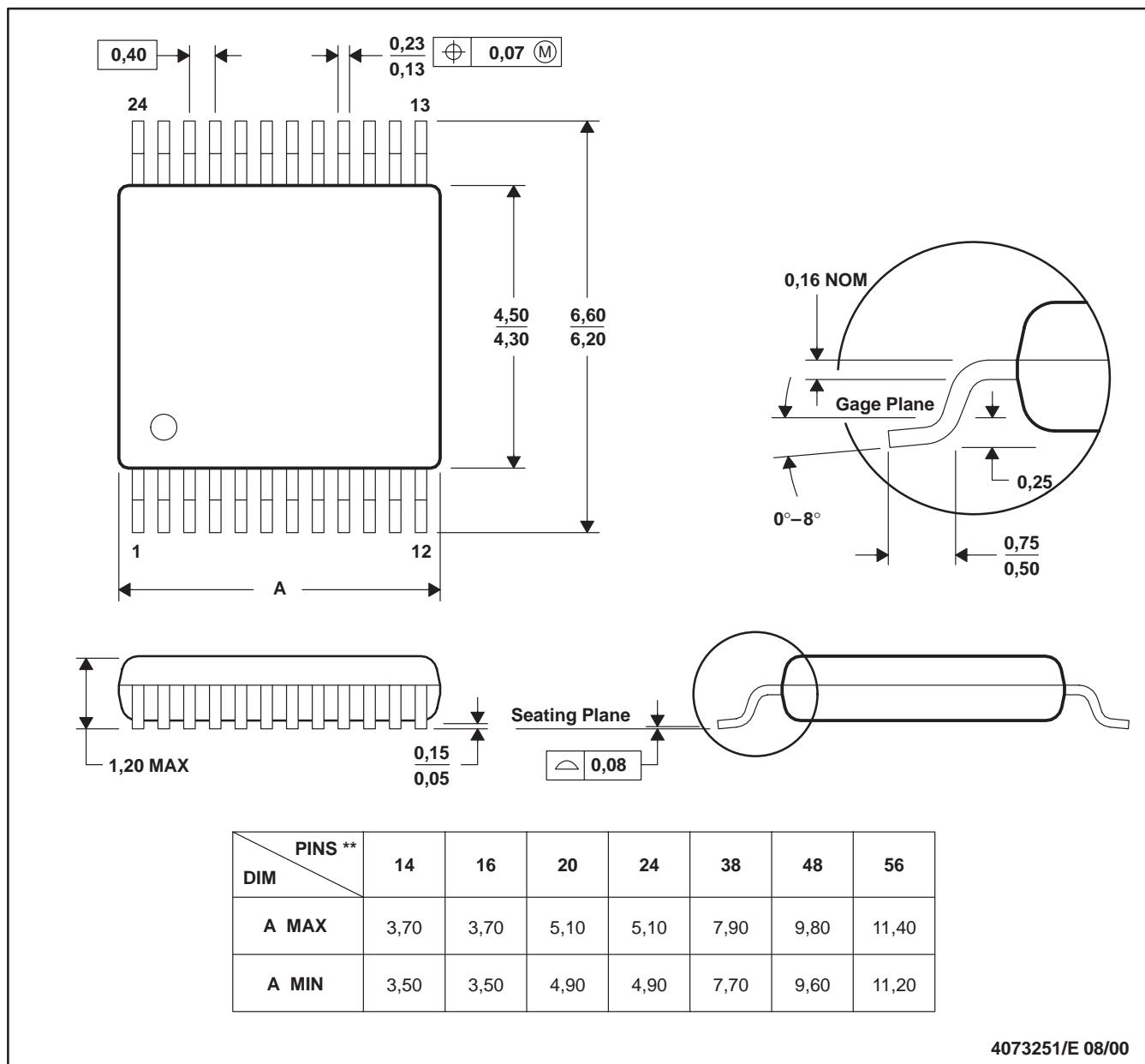
4040083/F 03/03

- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

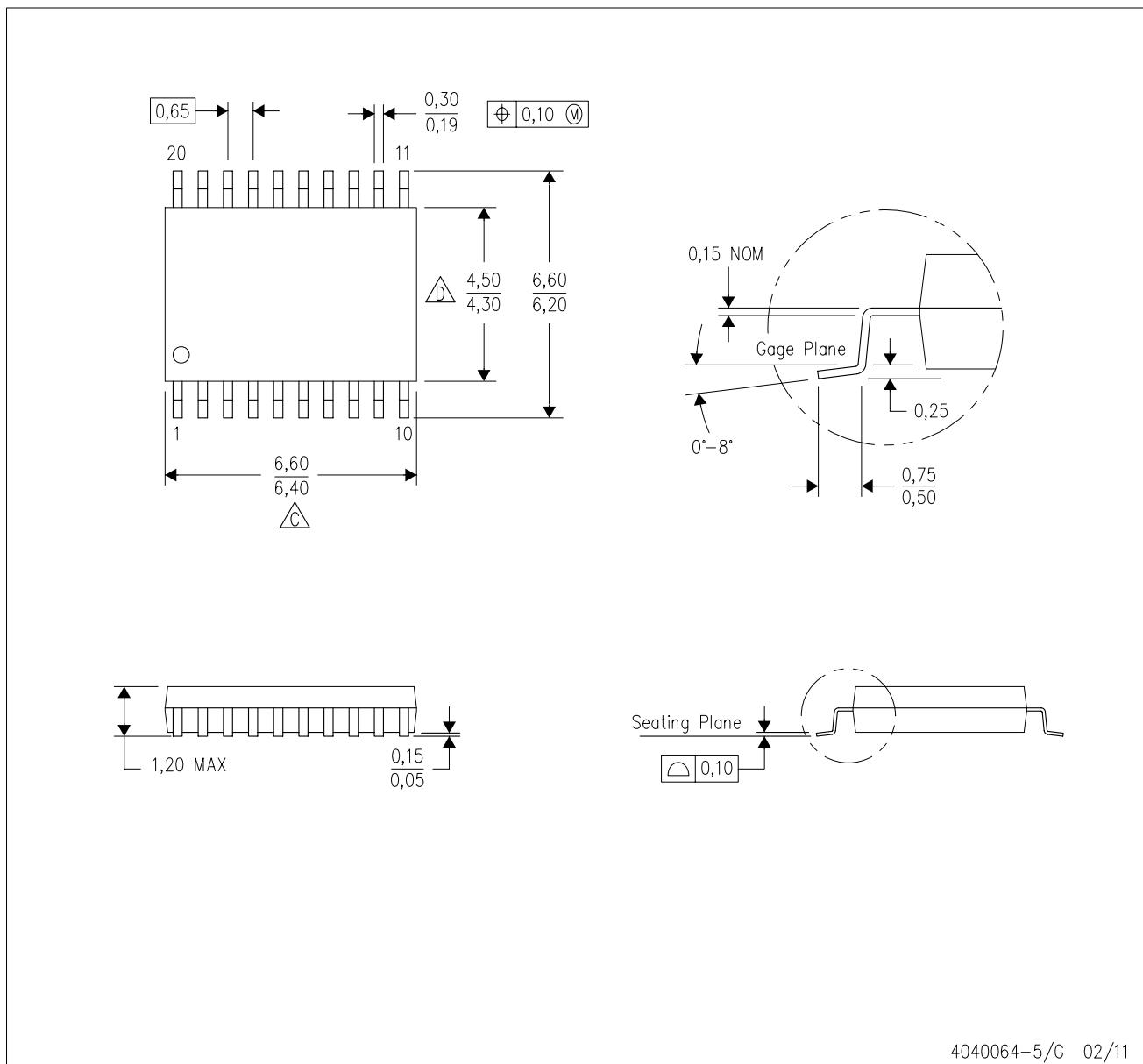
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

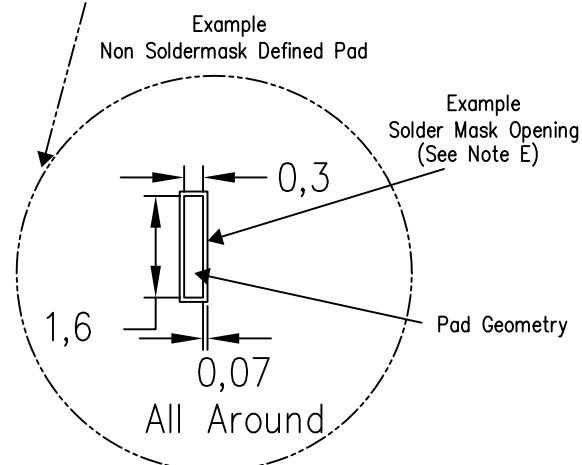
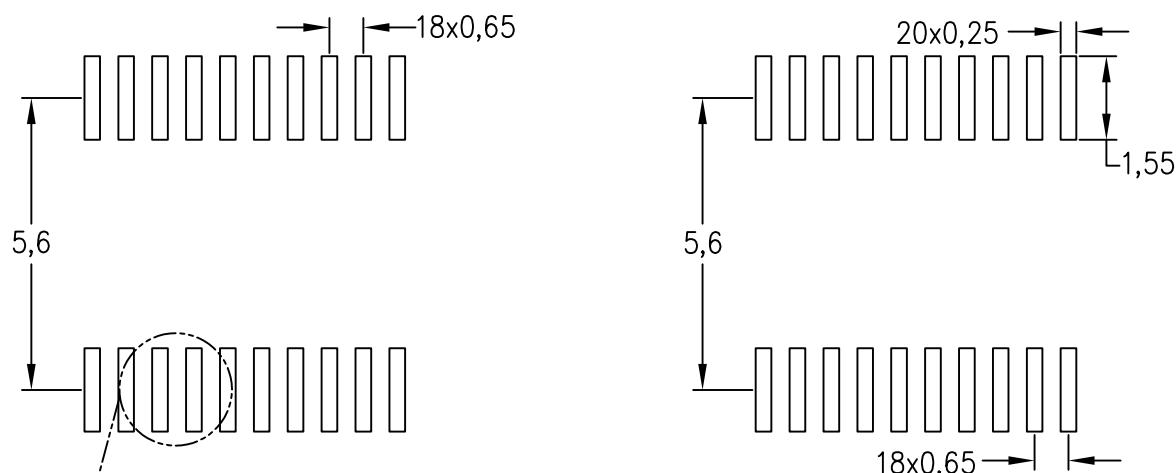
E. Falls within JEDEC MO-153

4040064-5/G 02/11

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

4211284-5/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

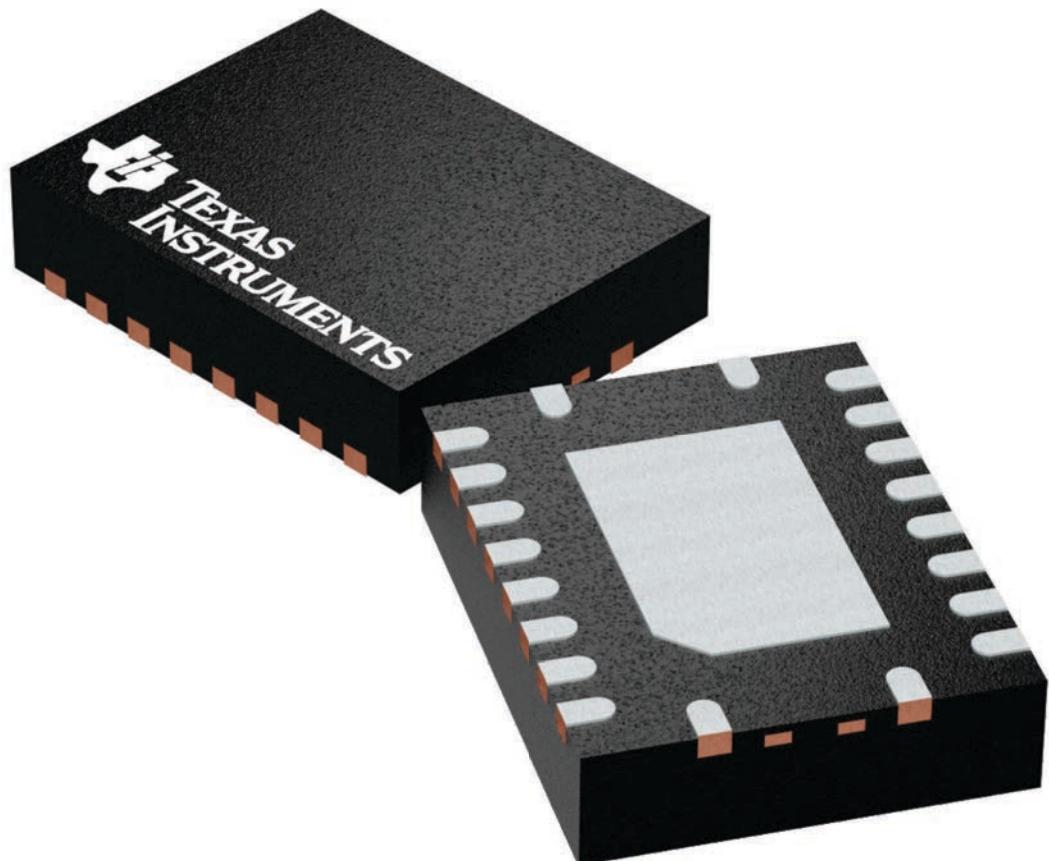
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

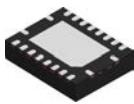
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A

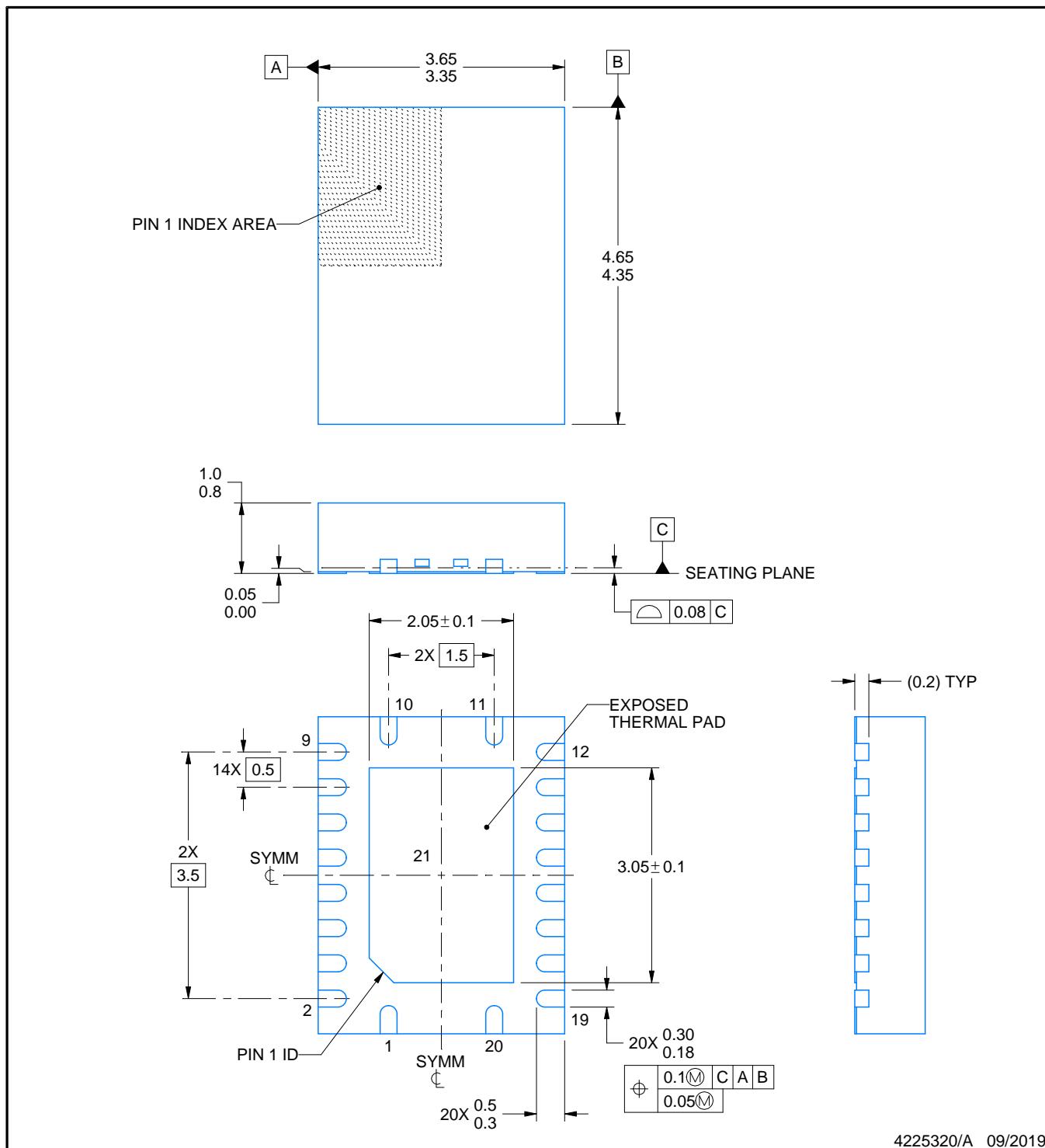
PACKAGE OUTLINE

RGY0020A



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4225320/A 09/2019

NOTES:

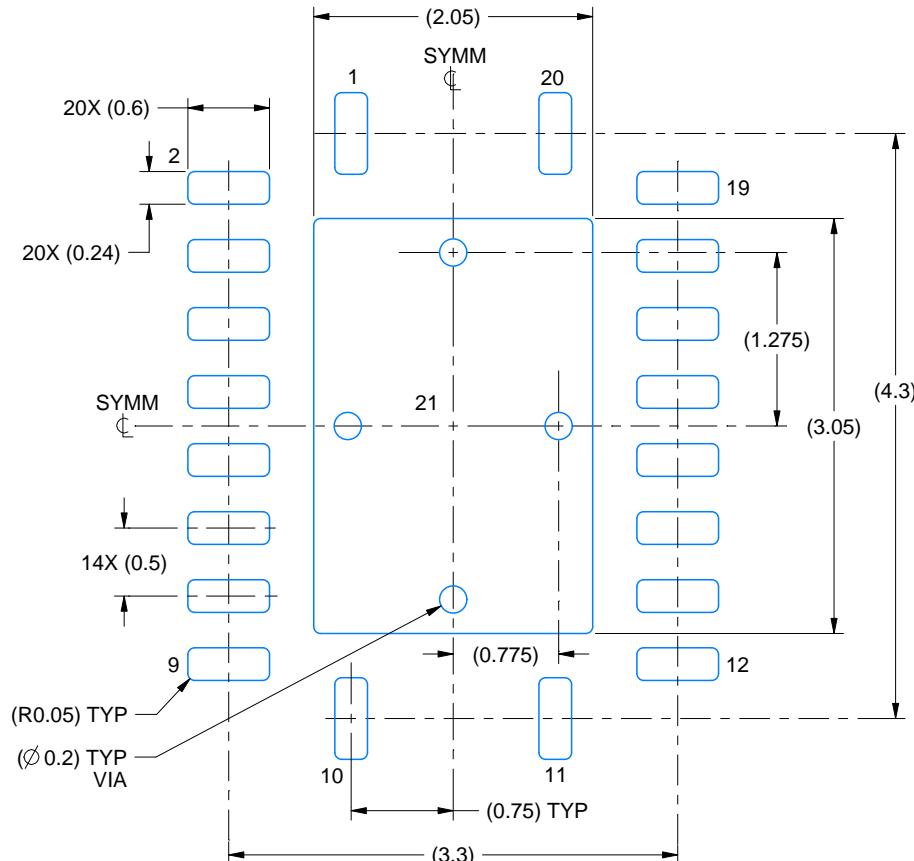
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

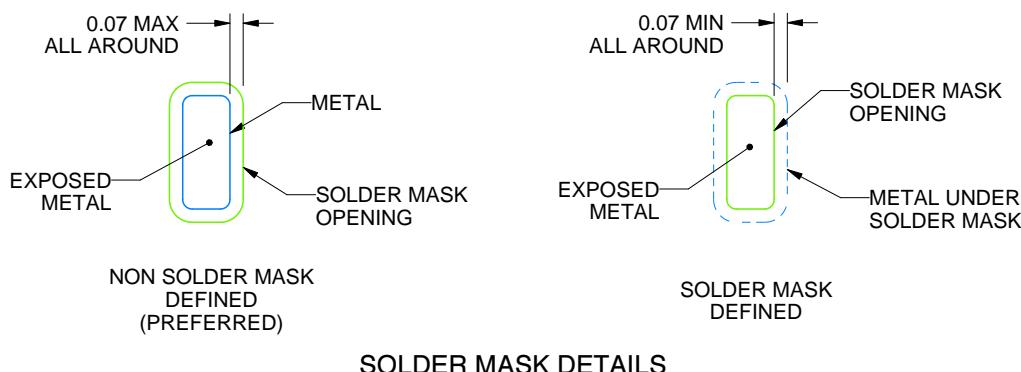
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

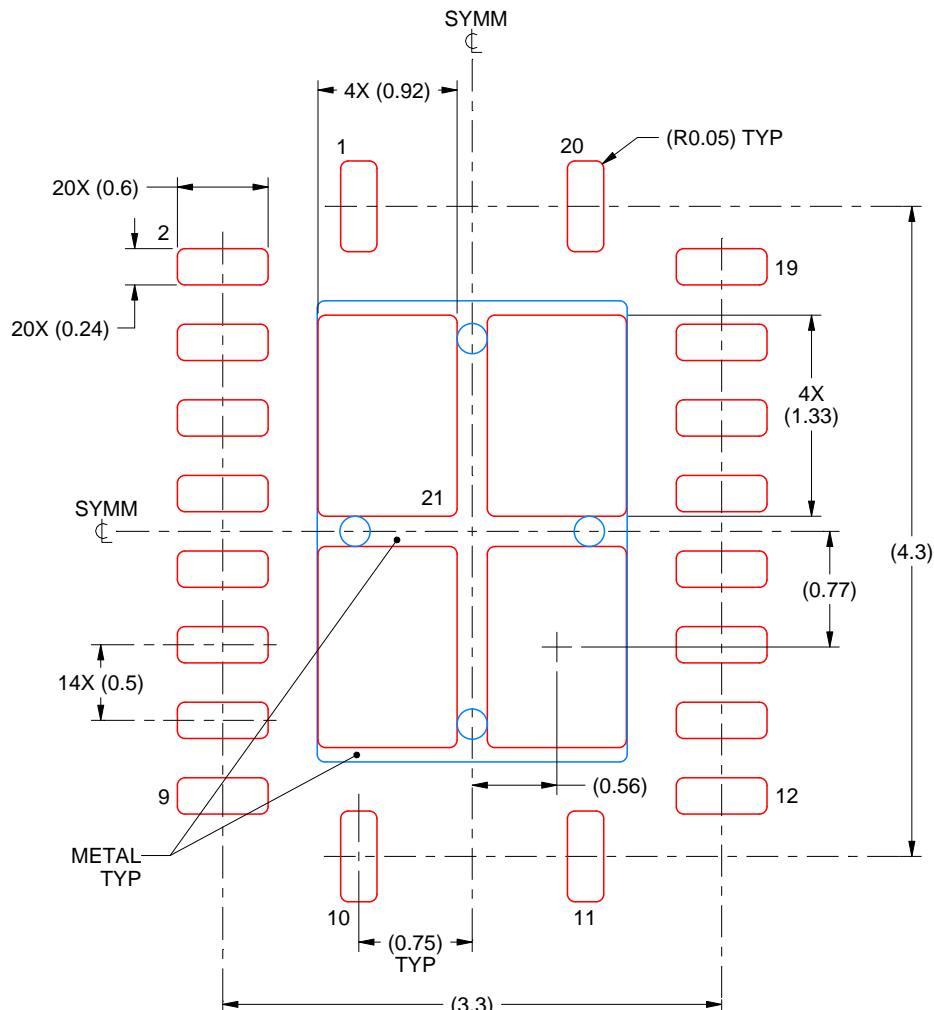
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

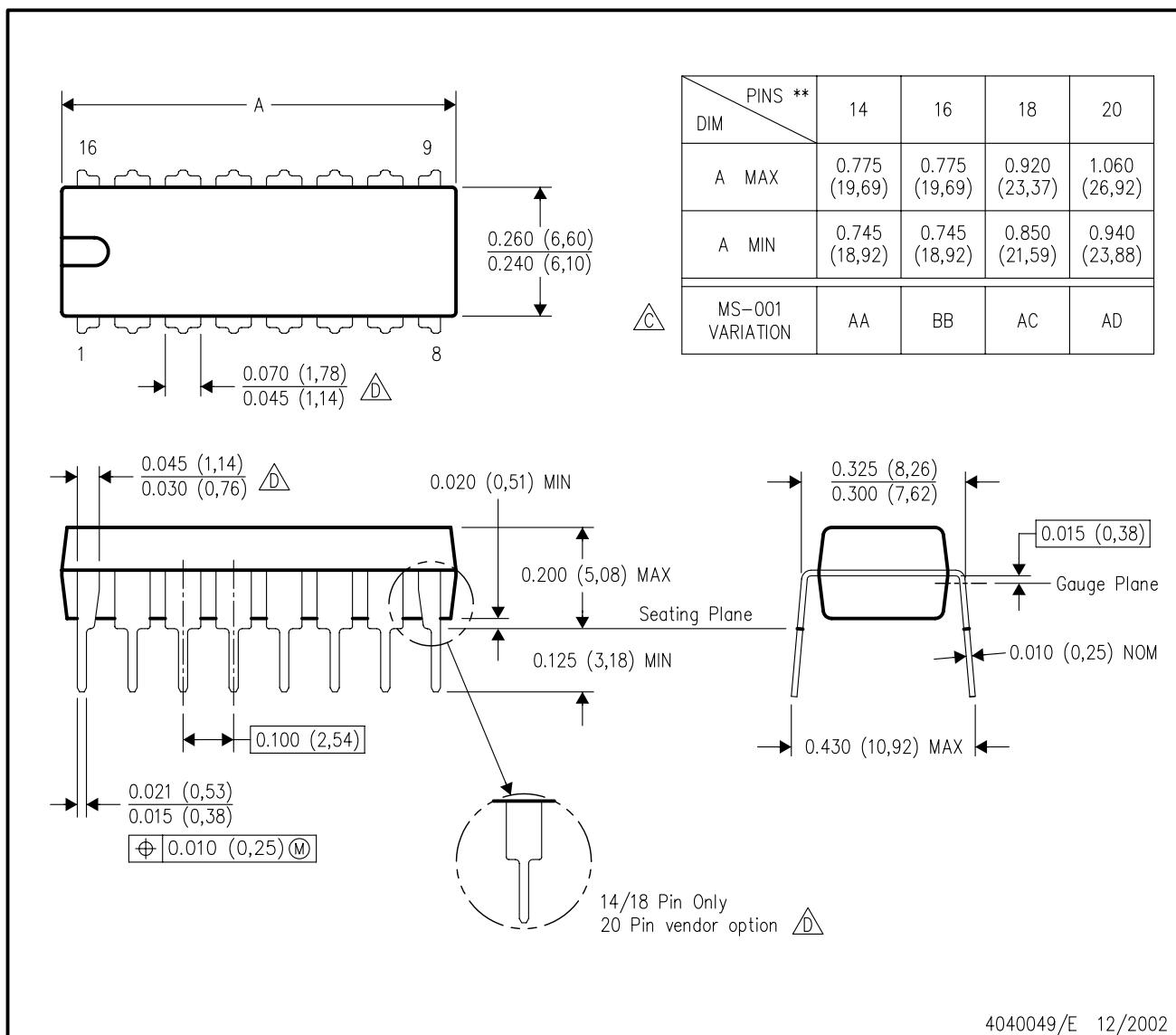
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

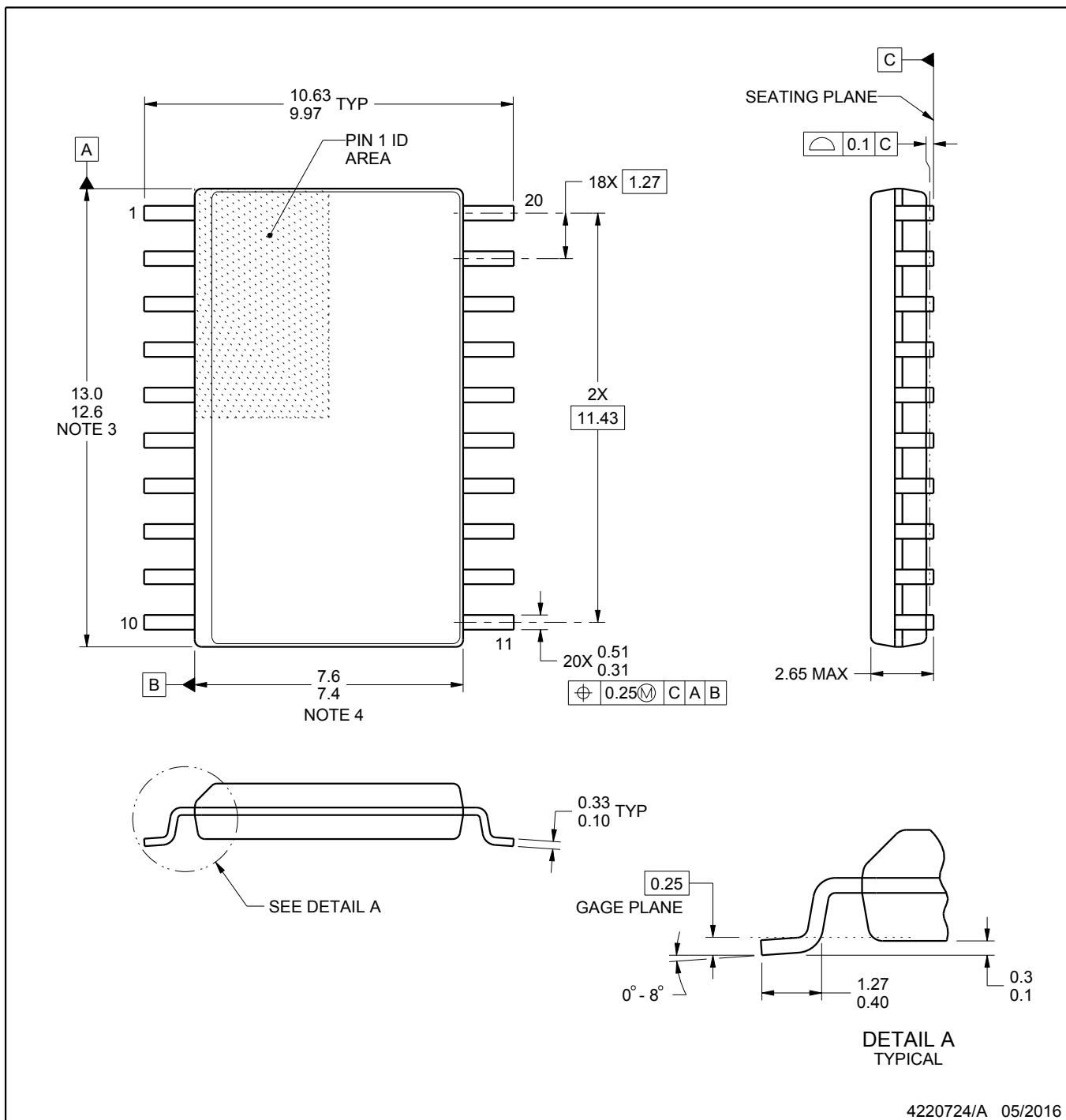


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



NOTES:

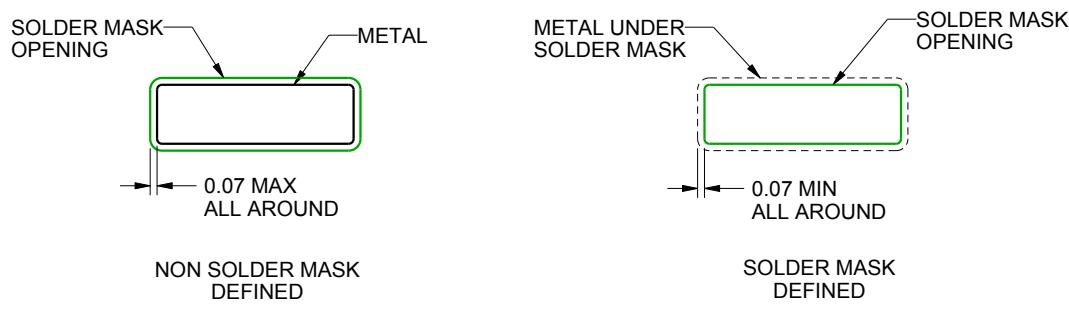
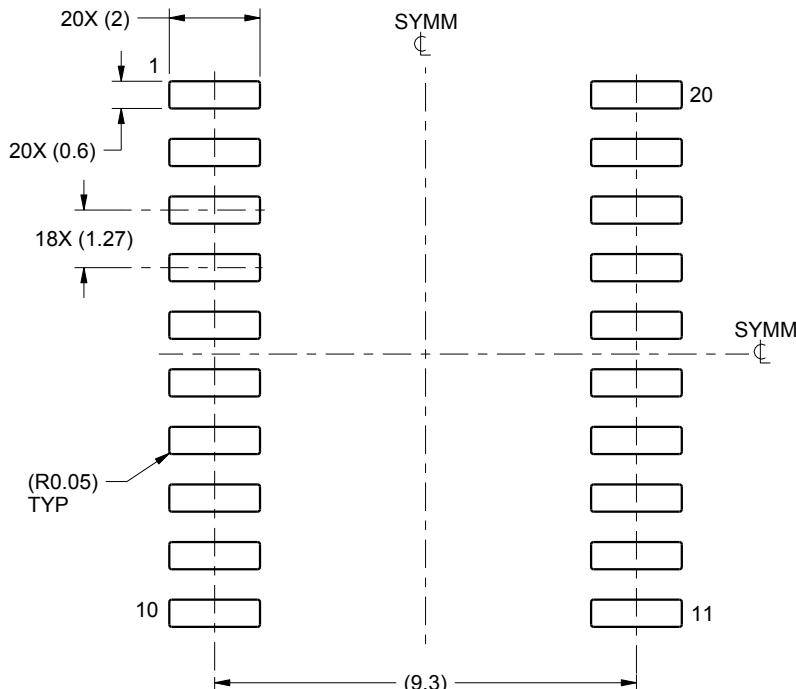
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
 5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

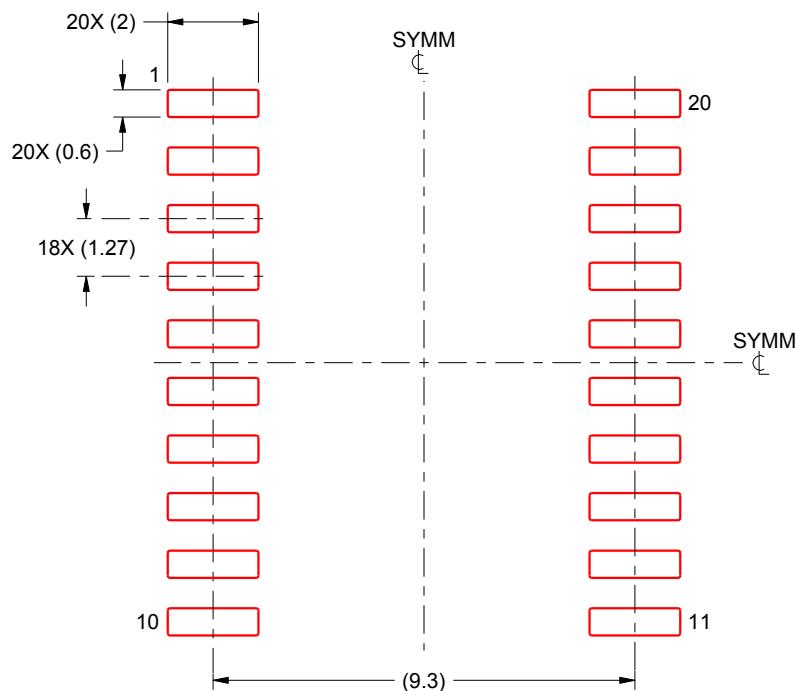
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

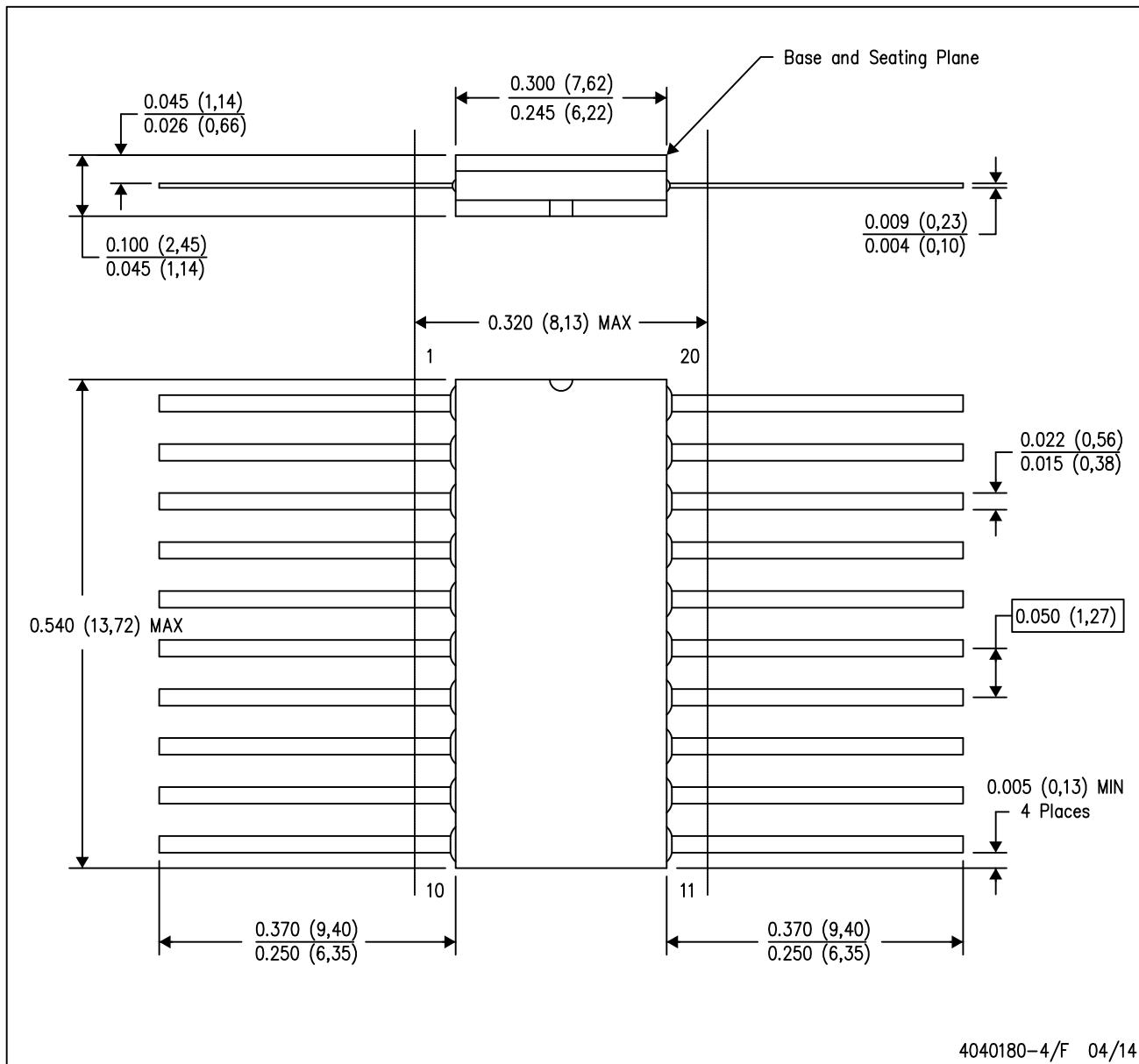
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

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