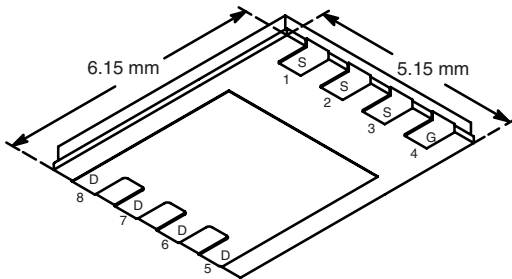


N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
40	0.0035 at $V_{GS} = 10$ V	50	45 nC
	0.0047 at $V_{GS} = 4.5$ V	50	

PowerPAK® SO-8



Bottom View

Ordering Information: Si7156DP-T1-E3 (Lead (Pb)-free)
Si7156DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

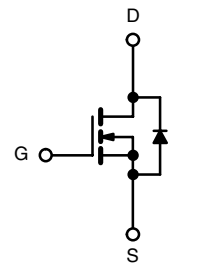
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % Avalanche Tested



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Synchronous Rectification
- Secondary Side DC/DC



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$ 50 ^a	A
		$T_C = 70^\circ\text{C}$ 50 ^a	
		$T_A = 25^\circ\text{C}$ 29 ^{b, c}	
		$T_A = 70^\circ\text{C}$ 23 ^{b, c}	
Pulsed Drain Current	I_{DM}	70	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$ 50 ^a	
		$T_A = 25^\circ\text{C}$ 4.9 ^{b, c}	
Single Pulse Avalanche Current	I_{AS}	40	mJ
Single Pulse Avalanche Energy	E_{AS}	80	
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$ 83	W
		$T_C = 70^\circ\text{C}$ 53	
		$T_A = 25^\circ\text{C}$ 5.4 ^{b, c}	
		$T_A = 70^\circ\text{C}$ 3.4 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	18	23	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	1.0	1.5	

Notes:

a. Package Limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 10$ s.

d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is $65^\circ\text{C}/\text{W}$.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		45		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 6.5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0		3.0	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V			1	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0028	0.0035	Ω
		V _{GS} = 4.5 V, I _D = 15 A		0.0038	0.0047	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A		85		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz		6900		pF
Output Capacitance	C _{oss}			605		
Reverse Transfer Capacitance	C _{rss}			310		
Total Gate Charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 20 A		103	155	nC
		V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 20 A		45	70	
Gate-Source Charge	Q _{gs}			19		
Gate-Drain Charge	Q _{gd}			12.3		
Gate Resistance	R _g	f = 1 MHz		0.6	1.2	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 2 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		22	40	ns
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			45	80	
Fall Time	t _f			9	18	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 2 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω		55	90	
Rise Time	t _r			32	60	
Turn-Off Delay Time	t _{d(off)}			56	100	
Fall Time	t _f			25	50	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			40	A
Pulse Diode Forward Current ^a	I _{SM}				70	
Body Diode Voltage	V _{SD}	I _S = 5 A		0.75	1.1	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C		40	70	ns
Body Diode Reverse Recovery Charge	Q _{rr}			52	100	nC
Reverse Recovery Fall Time	t _a			23		ns
Reverse Recovery Rise Time	t _b			17		

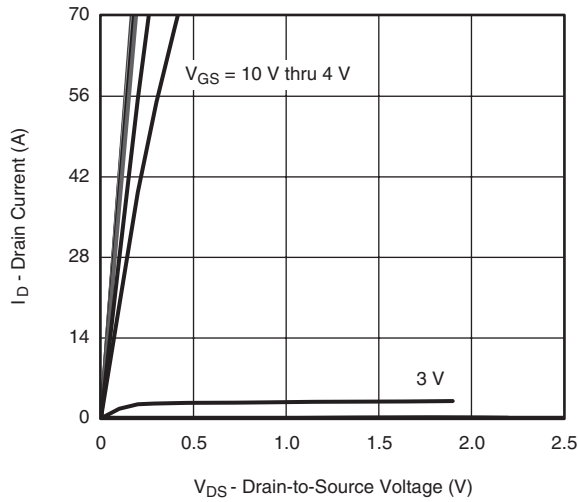
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

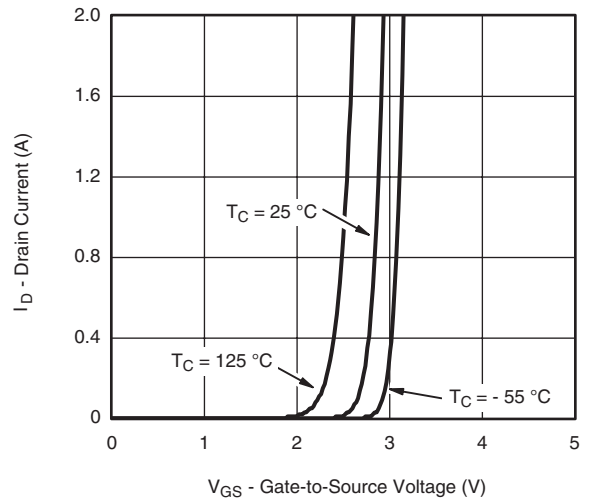
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

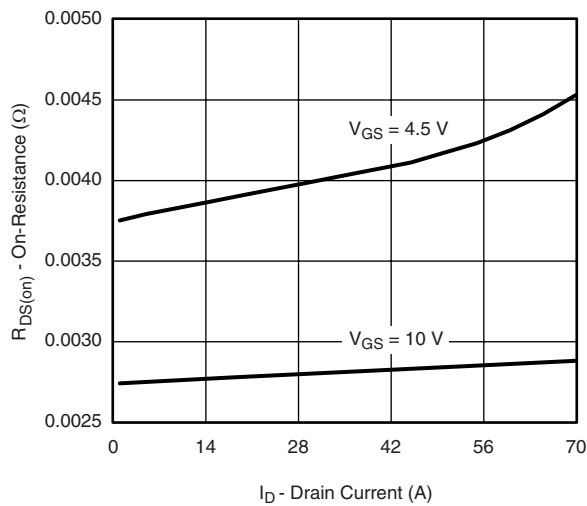
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



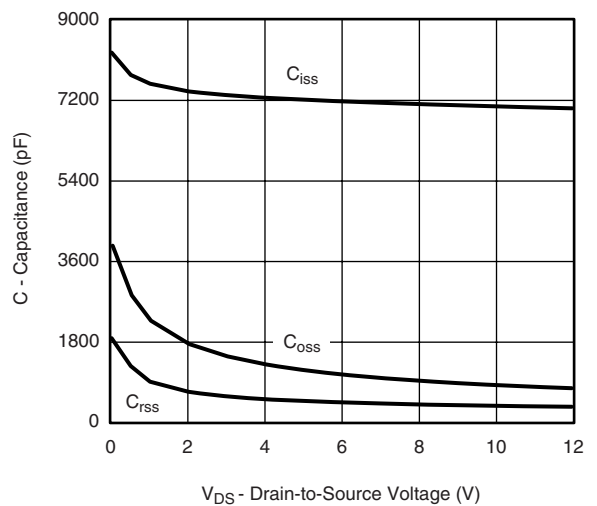
Output Characteristics



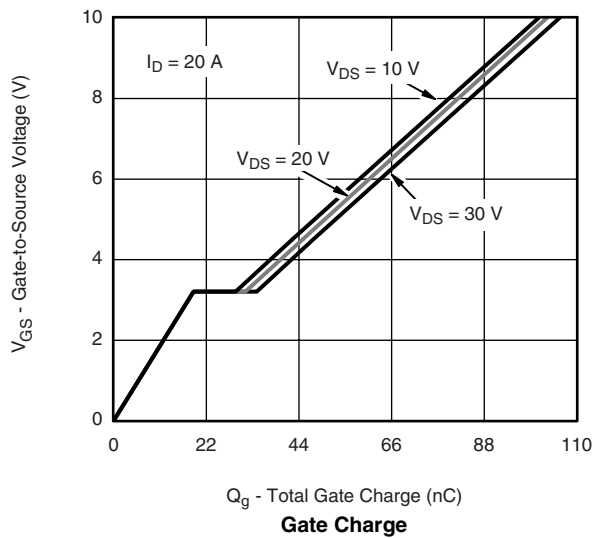
Transfer Characteristics



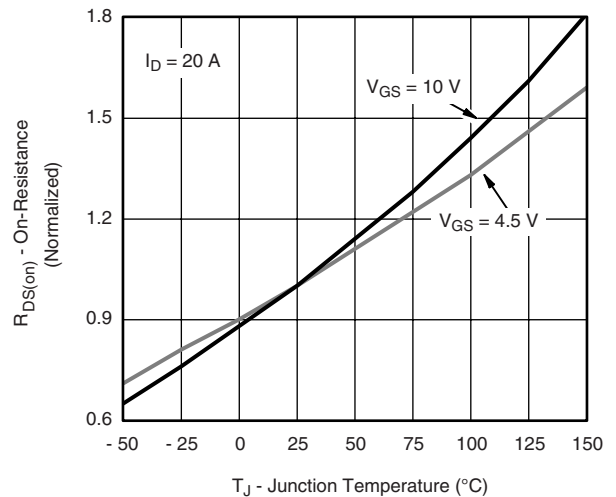
On-Resistance vs. Drain Current and Gate Voltage



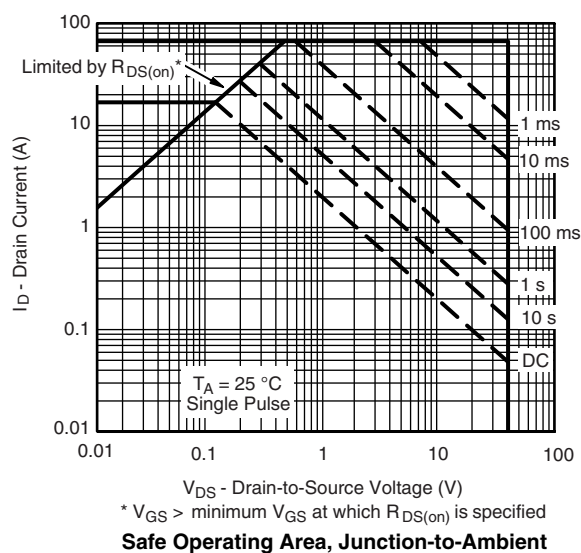
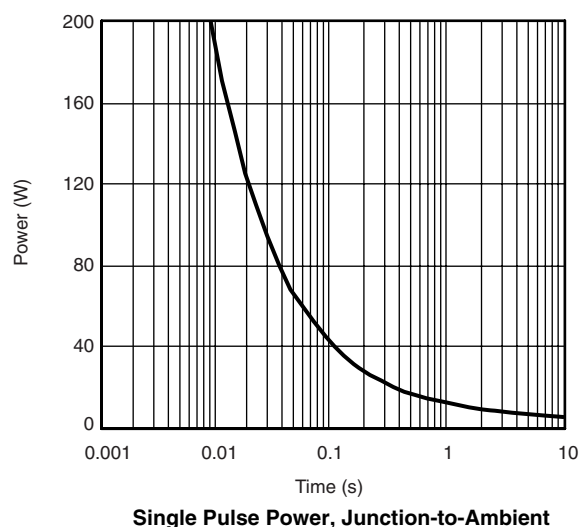
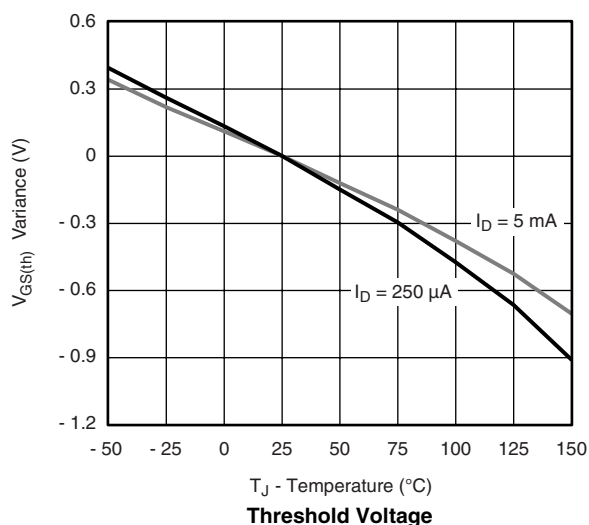
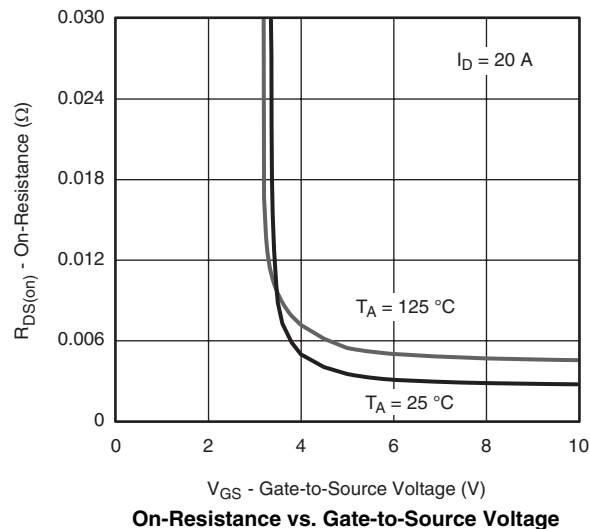
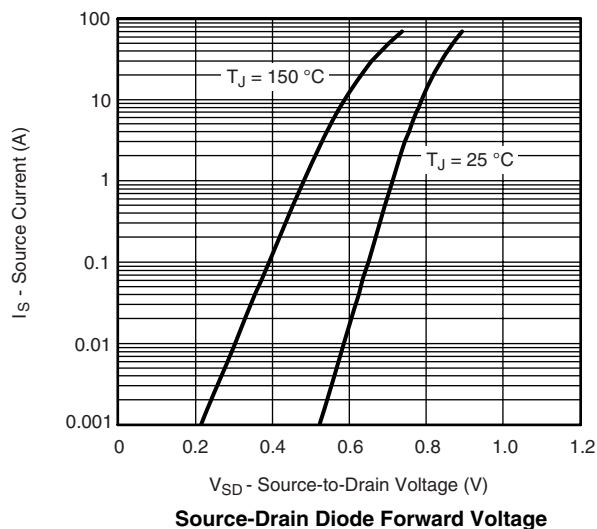
Capacitance



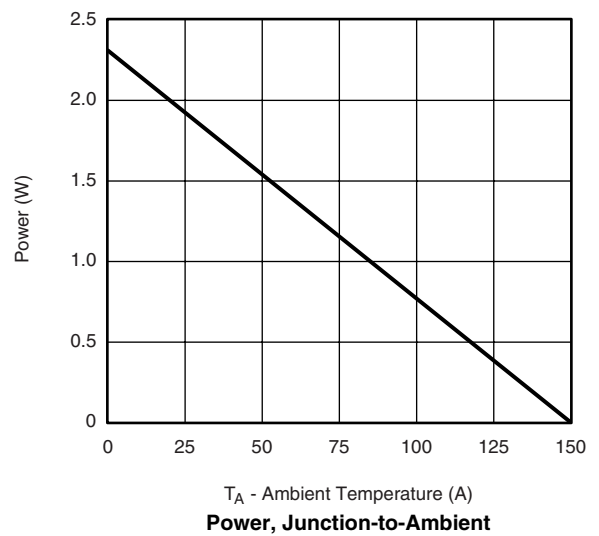
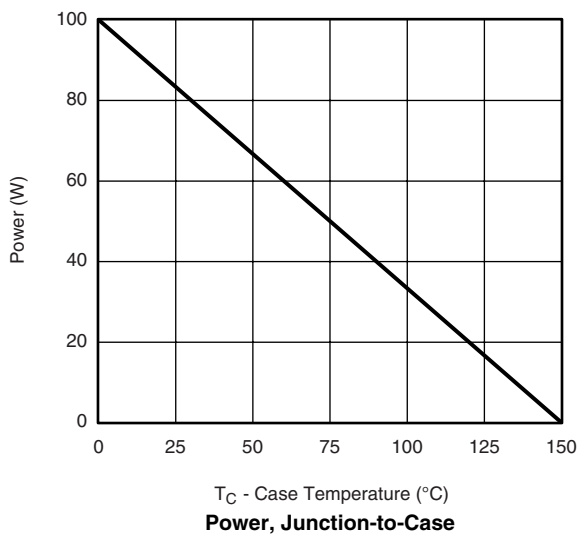
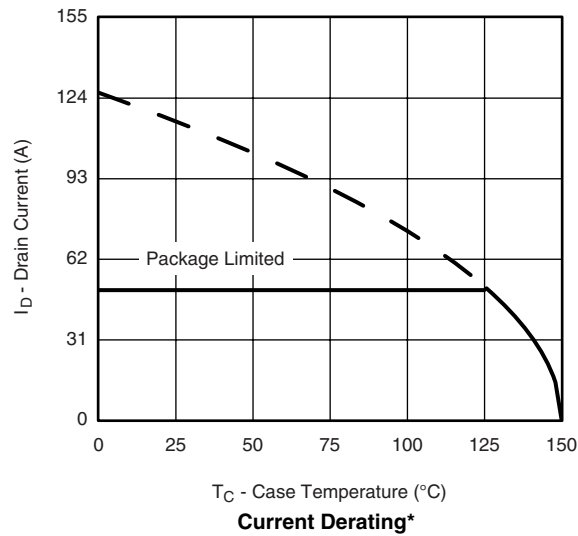
Gate Charge



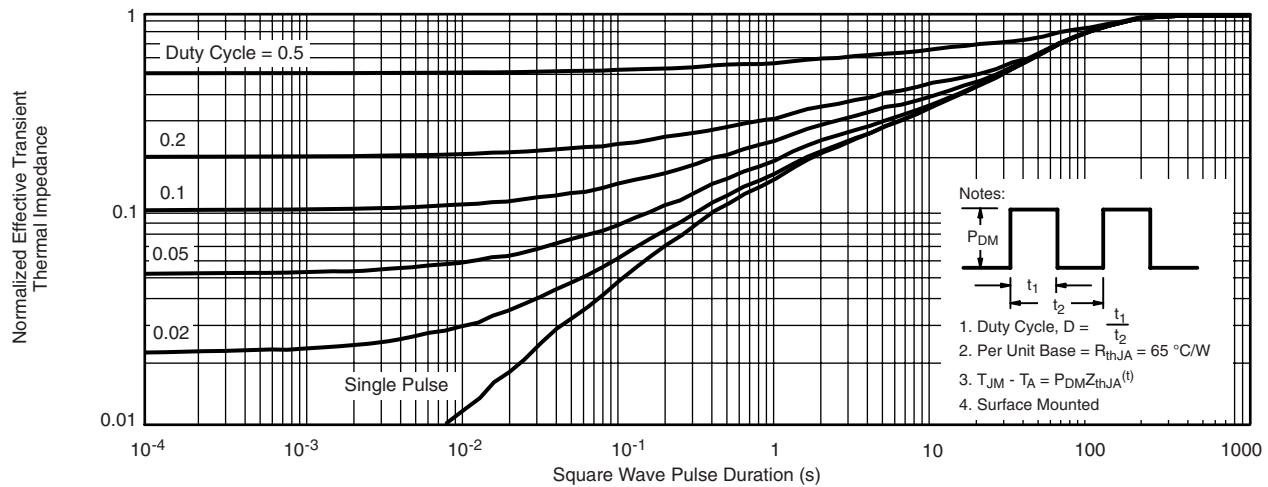
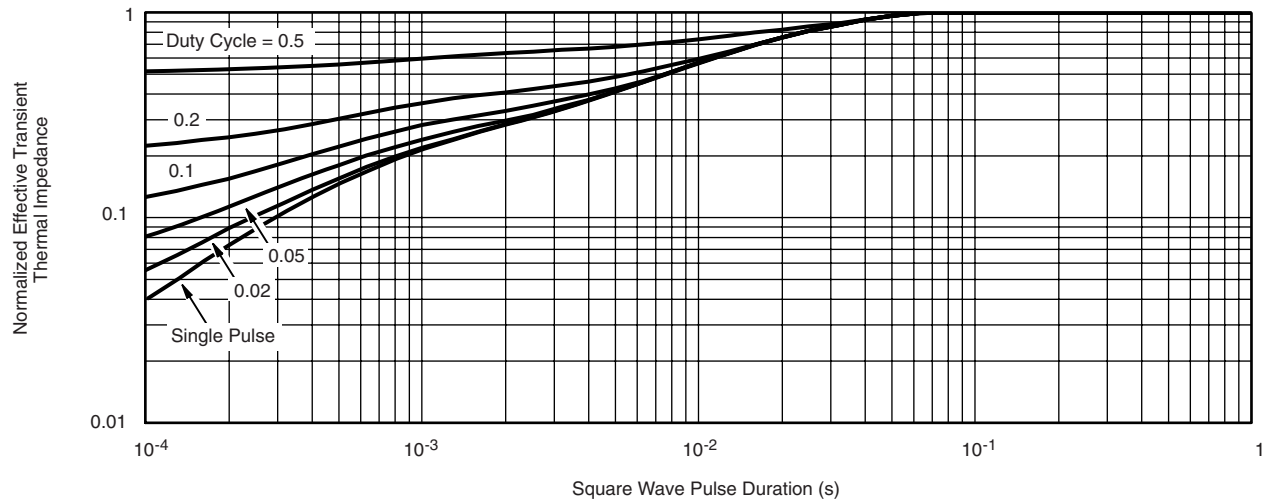
On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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