

## CY7C1020D

#### Features

- Pin- and function-compatible with CY7C1020B
- High speed
- ⊐ t<sub>AA</sub> = 10 ns
- Low active power

□ I<sub>CC</sub> = 80 mA @ 10 ns

Low complementary metal oxide semiconductor (CMOS) standby power

□ I<sub>SB2</sub> = 3 mA

- 2.0 V data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Independent control of upper and lower bits
- Available in Pb-free 44-pin 400-Mil wide Molded SOJ and 44-pin thin small outline package (TSOP) II packages

#### **Functional Description**

The CY7C1020D <sup>[1]</sup> is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected. The input and output pins ( $IO_0$  through  $IO_{15}$ ) are placed in a high-impedance state when:

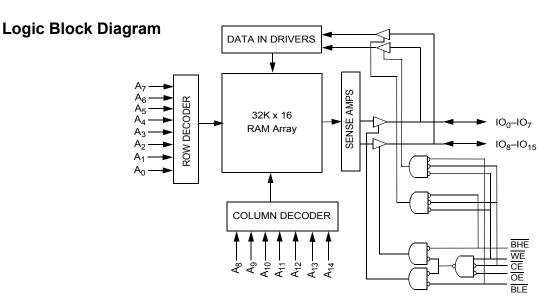
- Deselected (CE HIGH)
- Outputs are disabled (OE HIGH)
- BHE and BLE are disabled (BHE, BLE HIGH)
- When the write operation is active (CE LOW, and WE LOW)

Write to the device by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from IO pins (IO<sub>0</sub> through IO<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>14</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from IO pins (IO<sub>8</sub> through IO<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>14</sub>).

Reading from the device by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on IO<sub>0</sub> to IO<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on IO<sub>8</sub> to IO<sub>15</sub>. See the "Truth Table" on page 11 for a complete description of read and write modes.

The CY7C1020D device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click here.



#### Note

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

**Cypress Semiconductor Corporation** Document Number: 38-05463 Rev. \*J 198 Champion Court

San Jose, CA 95134-1709 • 408-943-2600 Revised November 28, 2014



## CY7C1020D

#### Contents

Pin Configurations	3
Selection Guide	3
Maximum Ratings	4
Operating Range	4
Electrical Characteristics	
Capacitance	5
Thermal Resistance	
AC Test Loads and Waveforms	5
Data Retention Characteristics	6
Data Retention Waveform	
Switching Characteristics	
Switching Waveforms	
Truth Table	

Ordering Information	12
Ordering Code Definitions	12
Package Diagrams	
Acronyms	15
Document Conventions	
Units of Measure	
Document History Page	16
Sales, Solutions, and Legal Information	17
Worldwide Sales and Design Support	
Products	
PSoC® Solutions	
Cypress Developer Community	
Technical Support	
••	



## **Pin Configurations**

Figure 1. 44-pin SOJ/TSOP II pinout (Top View) <sup>[2]</sup>

	44	A5
A <sub>3</sub> □ 2	43	$\Box A_6$
A <sub>2</sub> <u></u> 3	42	A7
A <sub>1</sub> □ 4	41	_ OE
A <sub>0</sub> <u></u> 5	40	BHE
CE C 6	39	BLE
IO <sub>0</sub> □ 7	38	□ IO <sub>15</sub>
IO <sub>1</sub> □ 8	37	
IO <sub>2</sub> □ 9	36	□ IO <sub>13</sub>
		□ IO <sub>12</sub>
V <sub>CC</sub> □1		⊐ v <sub>ss</sub>
V <sub>SS</sub> □ 12		□ V <sub>CC</sub>
	••••	
		₽ vc
$\begin{array}{c} A_4 \square 18 \\ A_{14} \square 19 \end{array}$		□ A <sub>8</sub> □ A <sub>9</sub>
$A_{13} \square 20$		$\square A_9$ $\square A_{10}$
$A_{12} \square 2^{\circ}$		$\square A_{11}$

### **Selection Guide**

Description	-10 (Industrial)	Unit
Maximum access time	10	ns
Maximum operating current	80	mA
Maximum CMOS standby current	3	mA



### **Maximum Ratings**

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature	–65 °C to +150 °C
Ambient temperature with power applied	–55 °C to +125 °C
Supply voltage on $V_{CC}$ to Relative GND <sup>[3]</sup>	–0.5 V to +6.0 V
DC voltage applied to outputs in High Z State <sup>[3]</sup>	s –0.5 V to V <sub>CC</sub> + 0.5 V

DC input voltage <sup>[3]</sup>	–0.5 V to $V_{CC}$ + 0.5 V
Current into outputs (LOW)	
Static discharge voltage (per MIL-STD-883, Method 3015)	>2001 V
Latch-up current	>200 mA

### **Operating Range**

Range	Ambient Temperature	V <sub>cc</sub>	Speed
Industrial	–40 °C to +85 °C	$5~V\pm0.5~V$	10 ns

#### **Electrical Characteristics**

Over the Operating Range

Devenueter	Description	Test Conditions		-10 (Industrial)		Unit
Parameter	Description	Test Conditions	Test Conditions		Мах	Unit
V <sub>OH</sub>	Output HIGH voltage	I <sub>OH</sub> = -4.0 mA		2.4	-	V
		I <sub>OH</sub> = -0.1 mA		_	3.4 <sup>[4]</sup>	
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 8.0 mA		_	0.4	V
V <sub>IH</sub>	Input HIGH voltage	-		2.2	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW voltage [3]	_		-0.5	0.8	V
I <sub>IX</sub>	Input load current	$GND \le V_I \le V_{CC}$		-1	+1	μA
I <sub>OZ</sub>	Output leakage current	$GND \le V_I \le V_{CC}$ , output disabled	$GND \leq V_{I} \leq V_{CC}$ , output disabled		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current		100 MHz	_	80	mA
		$f = f_{max} = 1/t_{RC}$	83 MHz	_	72	mA
			66 MHz	_	58	mA
			40 MHz	_	37	mA
I <sub>SB1</sub>	Automatic CE power-down current – TTL inputs	$\begin{array}{c} \text{Max } V_{CC}, \ \overline{CE} \geq V_{IH} \\ V_{IN} \geq V_{IH} \text{ or } V_{IN} \leq V_{IL}, \ f = f_{max} \end{array}$		-	10	mA
I <sub>SB2</sub>	Automatic CE Power-Down current – CMOS inputs	$eq:linear_line$	f = 0	-	3	mA

Note

- V<sub>IL</sub> (min) = -2.0 V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 1 V for pulse durations of less than 5 ns.
   Please note that the maximum V<sub>OH</sub> limit does not exceed minimum CMOS V<sub>IH</sub> of 3.5V. If you are interfacing this SRAM with 5V legacy processors that require a minimum V<sub>IH</sub> of 3.5V, please refer to Application Note AN6081 for technical details and options you may consider.



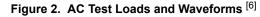
#### Capacitance

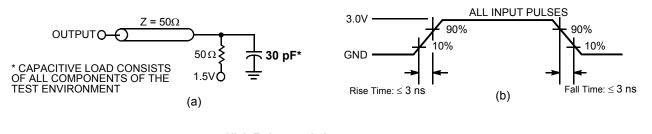
Parameter <sup>[5]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 5.0 V	8	pF
C <sub>OUT</sub>	Output capacitance		8	pF

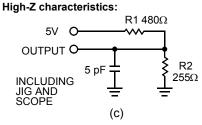
#### **Thermal Resistance**

Parameter <sup>[5]</sup>	Description	Test Conditions	SOJ	TSOP II	Unit
$\Theta_{JA}$		Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.52	53.91	°C/W
Θ <sup>JC</sup>	Thermal resistance (junction to case)		36.75	21.24	°C/W

#### AC Test Loads and Waveforms







Notes

- 5. Tested initially and after any design or process changes that may affect these parameters.
- 6. AC characteristics (except High-Z) are tested using the load conditions shown in Figure 2 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).



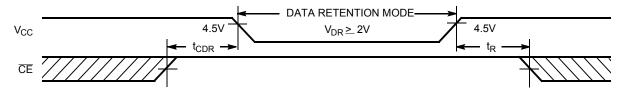
### **Data Retention Characteristics**

#### Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention	_	2.0	-	V
I <sub>CCDR</sub>	Data retention current	$\begin{array}{l} V_{\mathrm{CC}} = V_{\mathrm{DR}} = 2.0 \text{ V}, \ \overline{\mathrm{CE}} \geq V_{\mathrm{CC}} - 0.3 \text{ V}, \\ V_{\mathrm{IN}} \geq V_{\mathrm{CC}} - 0.3 \text{ V} \text{ or } V_{\mathrm{IN}} \leq 0.3 \text{ V} \end{array}$	-	3	mA
t <sub>CDR</sub> <sup>[7]</sup>	Chip deselect to data retention time	-	0	_	ns
t <sub>R</sub> <sup>[8]</sup>	Operation recovery time	-	t <sub>RC</sub>	-	ns

### **Data Retention Waveform**

Figure 3. Data Retention Waveform



- **Notes** 7. Tested initially and after any design or process changes that may affect these parameters. 8. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \ge 50 \ \mu s$  or stable at  $V_{CC(min)} \ge 50 \ \mu s$ .



#### **Switching Characteristics**

Over the Operating Range

Parameter <sup>[9]</sup>	Description	-10 (Inc	lustrial)	11:::4
Parameter <sup>101</sup>		Min	Max	Unit
Read Cycle			•	
t <sub>power</sub> <sup>[10]</sup>	V <sub>CC</sub> (typical) to the first access	100	_	μS
t <sub>RC</sub>	Read cycle time	10	-	ns
t <sub>AA</sub>	Address to data valid	-	10	ns
t <sub>OHA</sub>	Data hold from address change	3	-	ns
t <sub>ACE</sub>	CE LOW to data valid	-	10	ns
t <sub>DOE</sub>	OE LOW to data valid	-	5	ns
t <sub>LZOE</sub>	OE LOW to Low Z <sup>[12]</sup>	0		ns
t <sub>HZOE</sub>	OE HIGH to High Z [11, 12]	-	5	ns
t <sub>LZCE</sub>	CE LOW to Low Z <sup>[12]</sup>	3	_	ns
t <sub>HZCE</sub>	CE HIGH to High Z <sup>[11, 12]</sup>	-	5	ns
t <sub>PU</sub> <sup>[13]</sup>	CE LOW to power-up	0	-	ns
t <sub>PD</sub> <sup>[13]</sup>	CE HIGH to power-down	-	10	ns
t <sub>DBE</sub>	Byte enable to data valid		5	ns
t <sub>LZBE</sub>	Byte enable to Low Z	0	-	ns
t <sub>HZBE</sub>	Byte disable to High Z	-	5	ns
Write Cycle [14	, 15]		•	
t <sub>WC</sub>	Write cycle time	10	-	ns
t <sub>SCE</sub>	CE LOW to write end	7	-	ns
t <sub>AW</sub>	Address set-up to write end	7	-	ns
t <sub>HA</sub>	Address hold from write end	0	-	ns
t <sub>SA</sub>	Address set-up to write start	0	-	ns
t <sub>PWE</sub>	WE pulse width	7	-	ns
t <sub>SD</sub>	Data set-up to write end	6	-	ns
t <sub>HD</sub>	Data hold from write end	0	-	ns
t <sub>LZWE</sub>	WE HIGH to Low Z <sup>[12]</sup>	3	-	ns
t <sub>HZWE</sub>	WE LOW to High Z <sup>[11, 12]</sup>	-	5	ns
t <sub>BW</sub>	Byte enable to end of write	7	-	ns

Notes

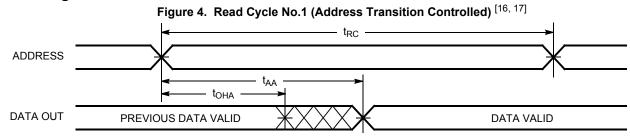
13. This parameter is guaranteed by design and is not tested.

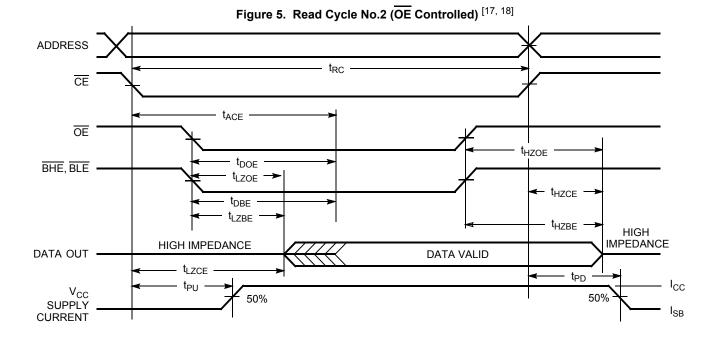
The internal write time of the memory is defined by the overlap of CE LOW, WE LOW and BHE/BLE LOW. CE, WE and BHE/BLE must be LOW to initiate a write and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
 The minimum write cycle time for Write Cycle No. 3 (WE controlled, OE LOW) should be equal to the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

<sup>9.</sup> Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
10. t<sub>POWER</sub> gives the minimum amount of time that the power supply should be at typical V<sub>CC</sub> values until the first memory access can be performed.
11. t<sub>HZOE</sub>, t<sub>HZBE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (c) of Figure 2 on page 5. Transition is measured when the outputs enter a high impedance state.
12. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZCE</sub>, and t<sub>HZWE</sub> for any given device.



**Switching Waveforms** 





#### Notes

- 16. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ . 17. WE is HIGH for read cycle.

<sup>18.</sup> Address valid prior to or coincident with  $\overline{CE}$  transition LOW.



#### Switching Waveforms(continued)

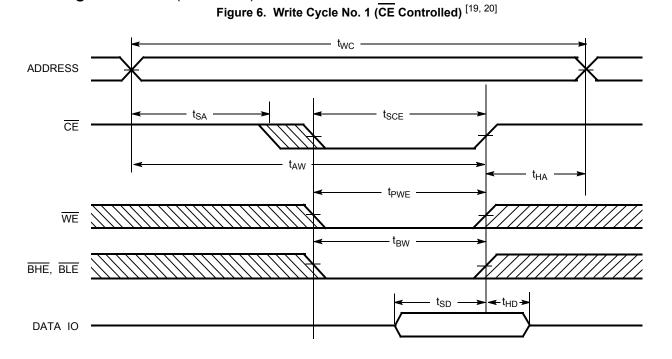
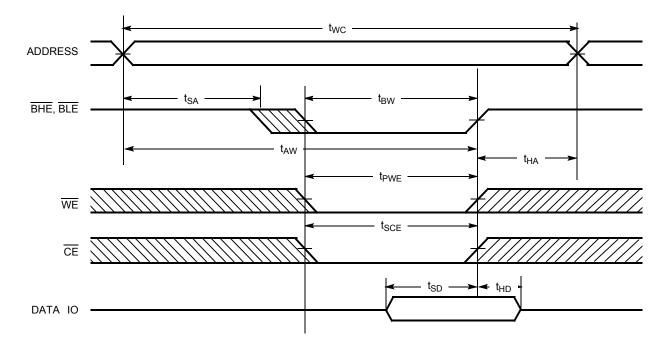


Figure 7. Write Cycle No. 2 (BLE or BHE Controlled) <sup>[19, 20]</sup>



#### Notes

19. Data IO is high impedance if OE or BHE and/or BLE= V<sub>IH</sub>. 20. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.



#### Switching Waveforms(continued)

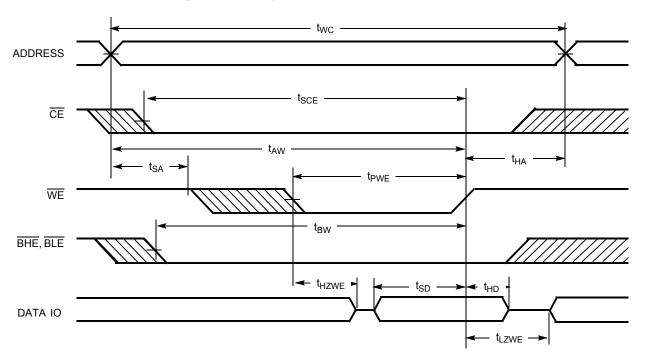


Figure 8. Write Cycle No. 3 (WE Controlled,  $\overline{\text{OE}}$  LOW) <sup>[21, 22]</sup>

Notes

21. The minimum write cycle time for Write Cycle No. 3 (WE controlled, OE LOW) should be equal to the sum of t<sub>HZWE</sub> and t<sub>SD.</sub> 22. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.



### Truth Table

CE	OE	WE	BLE	BHE	10 <sub>0</sub> –10 <sub>7</sub>	10 <sub>8</sub> –10 <sub>15</sub>	Mode	Power
Н	Х	Х	Х	Х	High Z	High Z	Power-down	Standby (I <sub>SB</sub> )
L	L	Н	L	L	Data out	Data out	Read – All bits	Active (I <sub>CC</sub> )
			L	Н	Data out	High Z	Read – Lower bits only	Active (I <sub>CC</sub> )
			Н	L	High Z	Data out	Read – Upper bits only	Active (I <sub>CC</sub> )
L	Х	L	L	L	Data in	Data in	Write – All bits	Active (I <sub>CC</sub> )
			L	Н	Data in	High Z	Write – Lower bits only	Active (I <sub>CC</sub> )
			Н	L	High Z	Data in	Write – Upper bits only	Active (I <sub>CC</sub> )
L	Н	Н	Х	Х	High Z	High Z	Selected, outputs disabled	Active (I <sub>CC</sub> )
L	Х	Х	Н	Н	High Z	High Z	selected, outputs disabled	Active (I <sub>CC</sub> )

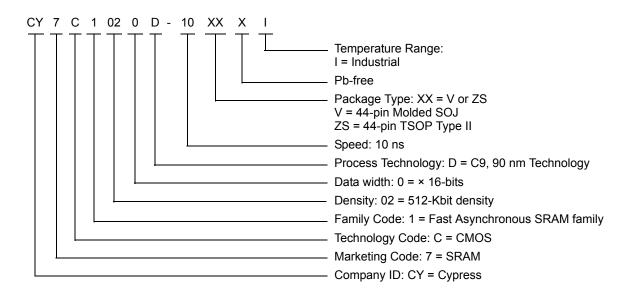


#### **Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1020D-10VXI	51-85082	44-pin SOJ (400 Mils) Pb-free	Industrial
	CY7C1020D-10ZSXI	51-85087	44-pin TSOP (Type II) Pb-free	

Please contact your local Cypress sales representative for availability of these parts.

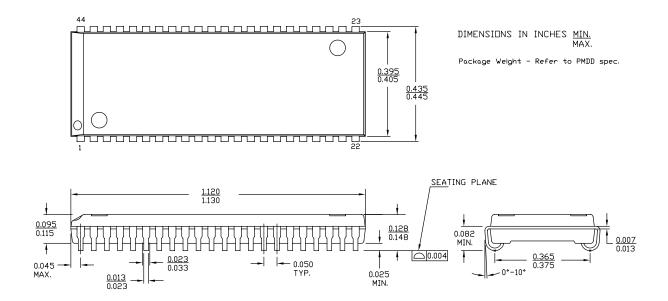
#### **Ordering Code Definitions**





#### **Package Diagrams**

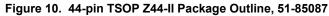
Figure 9. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082

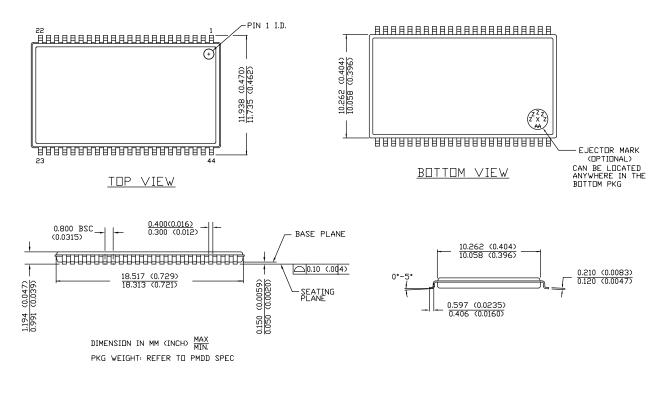


51-85082 \*E



#### Package Diagrams(continued)





51-85087 \*E



### Acronyms

Acronym	Description			
BGA	Ball Grid Array			
CMOS	Complementary Metal Oxide Semiconductor			
FBGA	Fine-Pitch Ball Gird Array			
I/O	Input/Output			
SRAM	Static Random Access Memory			
TSOP	Thin Small Outline Package			
TTL	Transistor-Transistor Logic			

#### **Document Conventions**

#### **Units of Measure**

Symbol	Unit of Measure			
°C	degree Celsius			
MHz	megahertz			
μA	microampere			
mA	milliampere			
ns	nanosecond			
Ω	ohm			
pF	picofarad			
V	volt			
W	watt			





## **Document History Page**

Document Title: CY7C1020D, 512-Kbit (32 K × 16) Static RAM Document Number: 38-05463				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Data sheet for C9 IPP
*A	233695	See ECN	RKF	<ol> <li>DC parameters modified as per EROS (Spec # 01-0216)</li> <li>Pb-free Offering in the 'Ordering Information'</li> </ol>
*B	263769	See ECN	RKF	1) Corrected pin #18 on SOJ/TSOPII Pinout (Page #1) from $A_{15}$ to $A_4$ 2) Changed IO <sub>1</sub> - IO <sub>16</sub> to IO <sub>0</sub> - IO <sub>15</sub> on the Pin-out diagram 3) Added T <sub>power</sub> Spec in Switching Characteristics Table 4) Added Data Retention Characteristics Table and Waveforms 5) Shaded 'Ordering Information'
*C	307594	See ECN	RKF	Reduced Speed bins to –10, –12 and –15 ns
*D	560995	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added $I_{CC}$ values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from $V_{CC}$ +2V to $V_{CC}$ +1V in footnote #3
*E	802877	See ECN	VKN	Changed $I_{\rm CC}$ specs from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz
*F	3109992	12/14/2010	AJU	Added Ordering Code Definitions. Updated Package Diagrams.
*G	3219056	04/07/2011	PRAS	Added TOC Added Acronyms and Units of Measure table. Updated Datasheet as per template.
*H	4033925	06/19/2013	MEMJ	Updated Functional Description. Updated Electrical Characteristics: Added one more Test Condition " $I_{OH} = -0.1$ mA" for V <sub>OH</sub> parameter and added maximum value corresponding to that Test Condition. Added Note 4 and referred the same note in maximum value for V <sub>OH</sub> paramete corresponding to Test Condition " $I_{OH} = -0.1$ mA". Updated Package Diagrams: spec 51-85082 – Changed revision from *C to *E. spec 51-85087 – Changed revision from *C to *E.
*	4385769	05/21/2014	MEMJ	No technical updates. Completing Sunset Review.
*J	4576526	11/21/2014	MEMJ	Added related documentation hyperlink in page 1.



#### Sales, Solutions, and Legal Information

#### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products	
Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
	cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

#### **PSoC<sup>®</sup> Solutions**

psoc.cypress.com/solutions PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community Community | Forums | Blogs | Video | Training

Technical Support cypress.com/go/support

© Cypress Semiconductor Corporation, 2010-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Document Number: 38-05463 Rev. \*J

Revised November 28, 2014

All products and company names mentioned in this document may be the trademarks of their respective holders.

# **Mouser Electronics**

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Cypress Semiconductor: <u>CY7C1020D-10VXI</u> <u>CY7C1020D-10VXIT</u> <u>CY7C1020D-10ZSXI</u> <u>CY7C1020D-10ZSXIT</u>