

## 32-Channel Serial-to-Parallel Converter with Open-Drain Outputs

### Features

- 100 mA Minimum Sink Current
- 16 MHz Shift Register Speed
- Polarity and Blanking Inputs
- CMOS-Compatible Inputs

### Applications

- Inkjet and Electrostatic Print Heads
- AC-Electroluminescent Displays
- Microelectromechanical Systems (MEMS) Applications

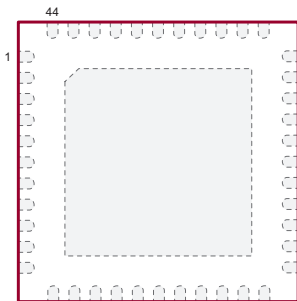
### General Description

The HV5523 is a low-voltage serial to high-voltage parallel converter with open-drain outputs. This device is designed as a driver for AC electroluminescent displays. It can also be used in any application requiring multiple-output high-voltage current sinking capabilities, such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent and large matrix LCD displays.

This device consists of a 32-bit Shift register, 32 latches and control logic to perform the polarity selection and blanking of the outputs. Data are shifted through the Shift register on the high-to-low transition of the clock. The HV5523 shifts counter clockwise when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the Shift register. Operation of the Shift register is not affected by the  $\overline{LE}$  (latch enable),  $\overline{BL}$  (blanking) and the  $\overline{POL}$  (polarity) inputs. Transfer of data from the Shift register to the latch occurs when the  $\overline{LE}$  (latch enable) input is high. The data in the latch is stored when  $\overline{LE}$  is low.

### Package Type

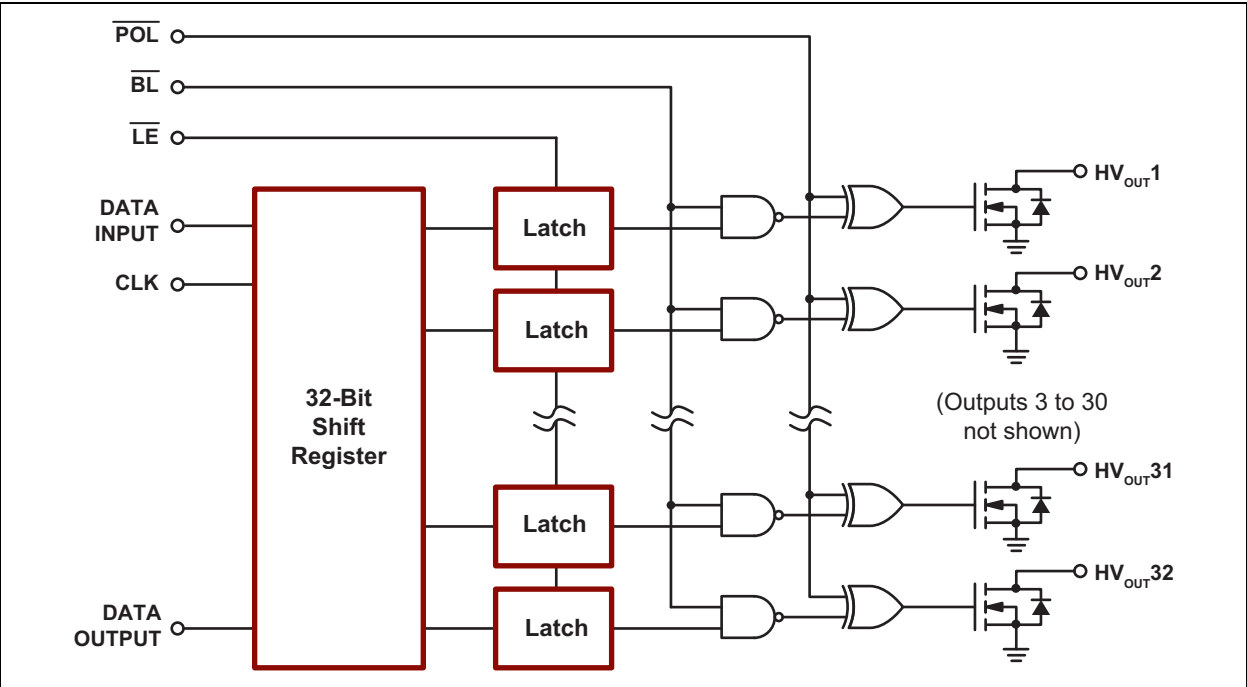
**44-lead QFN**  
(Top view)



See [Table 2-1](#) for pin information.

# HV5523

## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Supply Voltage, $V_{DD}$ (Note 1)	-0.5V to +7V
Output Voltage, $HV_{OUT}$ (Note 1)	-0.5V to +230V
Logic Input Levels (Note 1)	-0.5V to $V_{DD} + 0.5V$
Ground Current (Note 2)	1.5A
Maximum Junction Temperature, $T_{J(MAX)}$	+125°C
Storage Temperature, $T_S$	-65°C to +150°C
Continuous Total Power Dissipation:	
44-lead QFN (Note 3)	3.4W

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

- Note 1:** All voltages are referenced to  $V_{SS}$ .  
**Note 2:** Duty cycle is limited by the total power dissipated in the package.  
**Note 3:** 1 oz. 4-layer 3" x 4" PCB

### RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	$V_{DD}$	4.5	—	5.5	V	
High-Voltage Output	$HV_{OUT}$	-0.3	—	+220	V	
High-Level Input Voltage	$V_{IH}$	0.8 $V_{DD}$	—	$V_{DD}$	V	
Low-Level Input Voltage	$V_{IL}$	0	—	0.2 $V_{DD}$	V	
Clock Frequency	$f_{CLK}$	—	—	16	MHz	
Operating Ambient Temperature	$T_A$	-40	—	+85	°C	

### DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise noted.							
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions	
$V_{DD}$ Supply Current	$I_{DD}$	—	—	25	mA	$f_{CLK} = 16$ MHz, $f_{DATA} = 8$ MHz	
Quiescent $V_{DD}$ Supply Current	$I_{DDQ}$	—	—	100	μA	$D_{IN} = 0V$ , all input logic pins = 0V, all outputs off	
Off-State Output Current	$I_{O(OFF)}$	—	—	10	μA	All outputs high, all switches parallel	
High-Level Logic Input Current	$I_{IH}$	—	—	1	μA	$V_{IH} = V_{DD}$	
Low-Level Logic Input Current	$I_{IL}$	—	—	-1	μA	$V_{IL} = 0V$	
High-Level Output Data Out	$V_{OH}$	$V_{DD} - 1V$	—	—	V	$I_{DOUT} = -10$ mA	
Low-Level Output Voltage	$HV_{OUT}$	$V_{OL}$	—	—	15	V	$I_{HV_{OUT}} = +100$ mA
	Data Out		—	—	1	V	$I_{DOUT} = +10$ mA
$HV_{OUT}$ Clamp Voltage	$V_{OC}$	—	—	-1.5	V	$I_{OL} = -100$ mA	

# HV5523

## AC ELECTRICAL CHARACTERISTICS

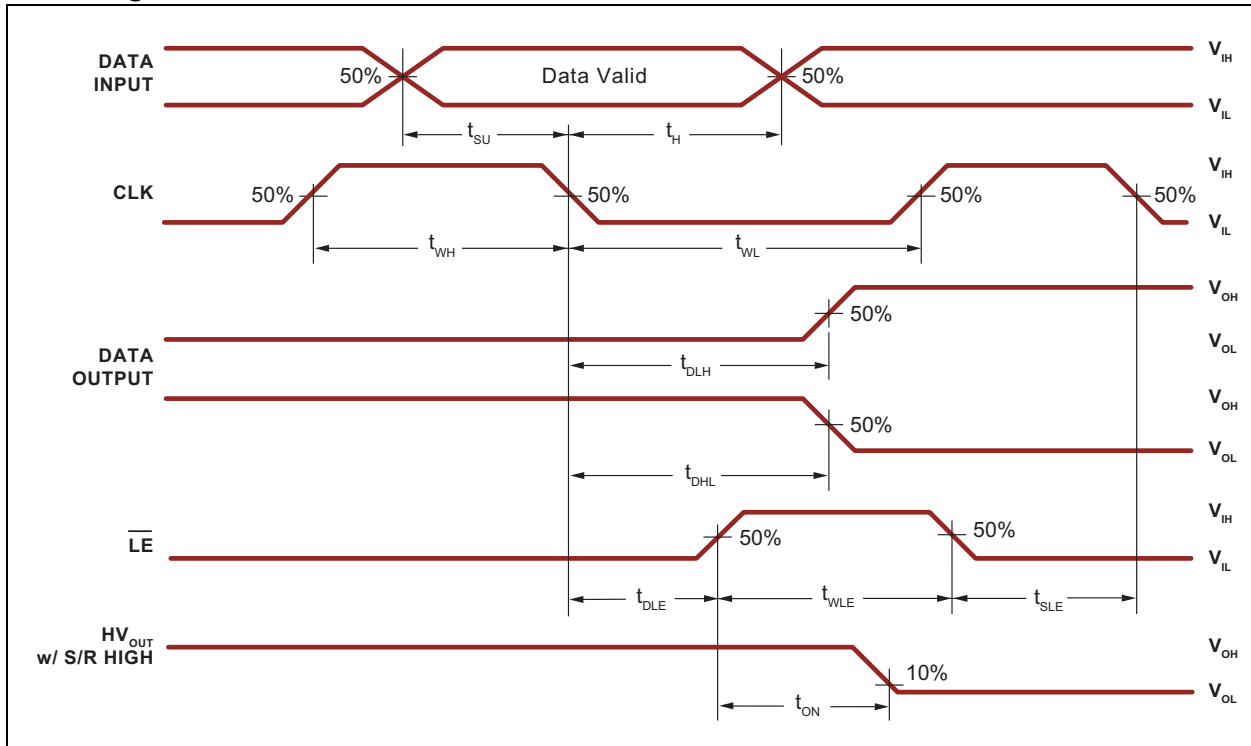
Electrical Specifications: $V_{DD} = 5V$ , $T_J = 25^\circ C$						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	$f_{CLK}$	—	—	16	MHz	
Clock Pulse Width, High or Low	$t_{WL}, t_{WH}$	31	—	—	ns	
Data Setup Time Before CLK Falls	$t_{SU}$	25	—	—	ns	
Data Hold Time after CLK Falls	$t_H$	10	—	—	ns	
Turn-On Time, $HV_{OUT}$ from Enable	$t_{ON}$	—	—	400	ns	$R_L = 2\text{ k}\Omega$ to $V_{PP}$ maximum
Delay Time Clock to Data High to Low	$t_{DHL}$	—	—	35	ns	$C_L = 15\text{ pF}$
Delay Time Clock to Data Low to High	$t_{DLH}$	—	—	35	ns	$C_L = 15\text{ pF}$
Delay Time Clock to $\overline{LE}$ Low to High	$t_{DLE}$	20	—	—	ns	
Width of $\overline{LE}$ Pulse	$t_{WLE}$	20	—	—	ns	
$\overline{LE}$ Setup Time Before Clock Falls	$t_{SLE}$	20	—	—	ns	
Digital Logic Input Capacitance	$C_{IN}$	—	—	15	pF	

## TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>TEMPERATURE RANGE</b>						
Operating Ambient Temperature	$T_A$	-40	—	+85	$^\circ C$	
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+125	$^\circ C$	
Storage Temperature	$T_S$	-65	—	+150	$^\circ C$	
<b>PACKAGE THERMAL RESISTANCE</b>						
44-lead QFN	$\theta_{JA}$	—	19	—	$^\circ C/W$	<a href="#">Note 1</a>

**Note 1:** 1 oz. 4-layer 3" x 4" PCB

## Switching Waveforms



# HV5523

## 2.0 PIN DESCRIPTION

The details on the pins of HV5523 are listed in [Table 2-1](#). Refer to [Package Type](#) for the location of pins.

**TABLE 2-1: 44-LEAD QFN PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	HV <sub>OUT</sub> 11	High-voltage output
2	HV <sub>OUT</sub> 12	High-voltage output
3	HV <sub>OUT</sub> 13	High-voltage output
4	HV <sub>OUT</sub> 14	High-voltage output
5	HV <sub>OUT</sub> 15	High-voltage output
6	HV <sub>OUT</sub> 16	High-voltage output
7	HV <sub>OUT</sub> 17	High-voltage output
8	HV <sub>OUT</sub> 18	High-voltage output
9	HV <sub>OUT</sub> 19	High-voltage output
10	HV <sub>OUT</sub> 20	High-voltage output
11	HV <sub>OUT</sub> 21	High-voltage output
12	HV <sub>OUT</sub> 22	High-voltage output
13	HV <sub>OUT</sub> 23	High-voltage output
14	HV <sub>OUT</sub> 24	High-voltage output
15	HV <sub>OUT</sub> 25	High-voltage output
16	HV <sub>OUT</sub> 26	High-voltage output
17	HV <sub>OUT</sub> 27	High-voltage output
18	HV <sub>OUT</sub> 28	High-voltage output
19	HV <sub>OUT</sub> 29	High-voltage output
20	HV <sub>OUT</sub> 30	High-voltage output
21	HV <sub>OUT</sub> 31	High-voltage output
22	HV <sub>OUT</sub> 32	High-voltage output
23	DATA OUT	Data output pin
24	NC	No internal connection
25	NC	No internal connection
26	NC	No internal connection
27	POL	Inverts the polarity of the HV <sub>OUT</sub> pins
28	CLK	Clock pin. The Shift registers shift data on the falling edge of input clock.
29	VSS	Reference voltage, usually ground
30	VDD	Logic supply voltage
31	LE	Latch enable pin. Data is shifted from the Shift register to the latches on logic input high.
32	DATA IN	Data input pin
33	$\overline{\text{BL}}$	Blanking pin sets all HV <sub>OUT</sub> pins ON or OFF, depending upon the state of polarity. See <a href="#">Table 3-2</a> .
34	N/C	No internal connection

**TABLE 2-1: 44-LEAD QFN PIN FUNCTION TABLE (CONTINUED)**

Pin Number	Pin Name	Description
35	HV <sub>OUT1</sub>	High-voltage output
36	HV <sub>OUT2</sub>	High-voltage output
37	HV <sub>OUT3</sub>	High-voltage output
38	HV <sub>OUT4</sub>	High-voltage output
39	HV <sub>OUT5</sub>	High-voltage output
40	HV <sub>OUT6</sub>	High-voltage output
41	HV <sub>OUT7</sub>	High-voltage output
42	HV <sub>OUT8</sub>	High-voltage output
43	HV <sub>OUT9</sub>	High-voltage output
44	HV <sub>OUT10</sub>	High-voltage output
Center Tab		Connect to VSS.

# HV5523

## 3.0 FUNCTIONAL DESCRIPTION

Follow the steps in [Table 3-1](#) to power up and power down the HV5523.

**TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE**

Power-Up		Power-Down	
Step	Description	Step	Description
1	Connect ground.	1	Remove all inputs.
2	Apply $V_{DD}$ .	2	Remove $V_{DD}$ .
3	Set all inputs to a known state.	3	Disconnect ground.

**TABLE 3-2: FUNCTION TABLE**

Function	Inputs <sup>1</sup>					Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Register		High-Voltage Output		Data Out
						1	2...32	1	2...32	
All On	X	X	X	L	L	Note 2	Note 2	On	On	Note 2
All Off	X	X	X	L	H	Note 2	Note 2	Off	Off	Note 2
Invert Mode	X	X	L	H	L	Note 2	Note 2	$\overline{\text{Note 2}}$	$\overline{\text{Note 2}}$	Note 2
Load S/R	H or L	↓	L	H	H	H or L	Note 2	Note 2	Note 2	Note 2
Load Latches	X	H or L	↑	H	H	Note 2	Note 2	Note 2	Note 2	Note 2
	X	H or L	↑	H	L	Note 2	Note 2	$\overline{\text{Note 2}}$	$\overline{\text{Note 2}}$	Note 2
Transparent Latch Mode	L	↓	H	H	H	L	Note 2	Off	Note 2	Note 2
	H	↓	H	H	H	H	Note 2	On	Note 2	Note 2

**Note 1:** H = High logic level

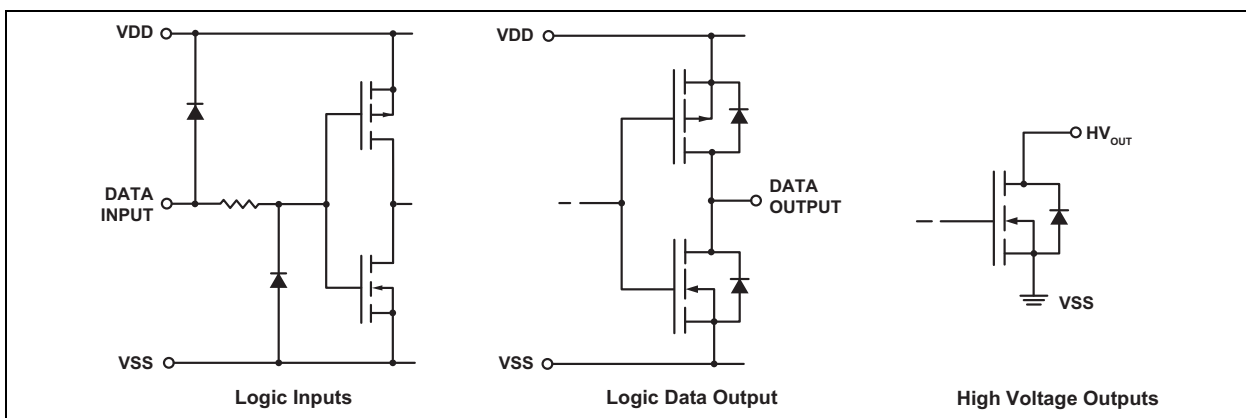
L = Low logic level

X = Don't care

↓ = High-to-low transition

↑ = Low-to-high transition

**2:** Dependent on previous stage's state before the last CLK ↓ or last  $\overline{LE}$  high



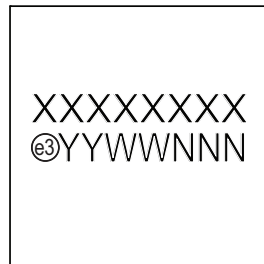
**FIGURE 3-1:** Input and Output Equivalent Circuits.



## 4.0 PACKAGE MARKING INFORMATION

### 4.1 Packaging Information

44-lead QFN

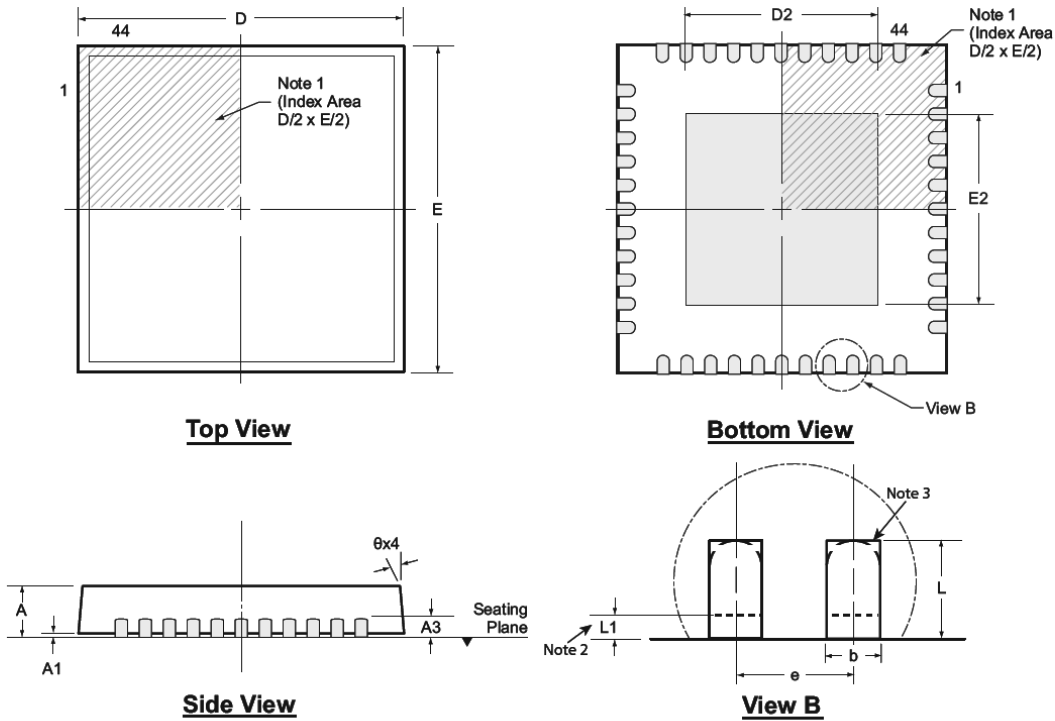


Example



<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

## 44-Lead QFN Package Outline (K7) 7.00x7.00mm body, 0.80mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

**Notes:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol	A	A1	A3	b	D	D2	E	E2	e	L	L1	θ	
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.18	6.85*	5.00†	6.85*	5.00†	0.50 BSC	0.45†	0.00	0°
	NOM	0.75	0.02		0.25	7.00	5.15†	7.00	5.15†		0.55†	-	-
	MAX	0.80	0.05		0.30	7.15*	5.25†	7.15*	5.25†		0.65†	0.15	14°

JEDEC Registration MO-220, Variation WKKD-3, Issue K, June 2006

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

## APPENDIX A: REVISION HISTORY

### Revision A (July 2019)

- Converted Supertex Doc# DSFP-HV5523 to Microchip DS20005700A
- Changed the quantity of the 44-lead QFN K7 package from 280/Tray to 260/Tray
- Changed the quantity of the 44-lead QFN K7 M933 media type from 2000/Reel to 3000/Reel
- Made minor text changes throughout the document

# HV5523

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	HV5523	=	32-Channel Serial-to-Parallel Converter with Open-Drain Outputs		
Package:	K7	=	44-lead (7x7) WQFN		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	260/Tray for a K7 Package		
	M933	=	3000/Reel for a K7 Package		

**Examples:**

a) HV5523K7-G: 32-Channel Serial-to-Parallel Converter with Open-Drain Outputs, 44-lead (7x7) WQFN, 260/Tray

b) HV5523K7-G-M933: 32-Channel Serial-to-Parallel Converter with Open-Drain Outputs, 44-lead (7x7) WQFN, 3000/Reel

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