19-3063; Rev 0; 1/04

Ultra-Low-Power, 12-Bit, Voltage-Output DACs

General Description

The MAX5530/MAX5531 are single, 12-bit, ultra-low-power, voltage-output, digital-to-analog converters (DACs) offering Rail-to-Rail® buffered voltage outputs. The DACs operate from a 1.8V to 5.5V supply and consume less than 6µA, making them desirable for low-power and low-voltage applications. A shutdown mode reduces overall current, including the reference input current, to just 0.18µA. The MAX5530/MAX5531 use a 3-wire serial interface that is compatible with SPI™, QSPI™, and MICROWIRE™.

At power-up, the MAX5530/MAX5531 outputs are driven to zero scale, providing additional safety for applications that drive valves or for other transducers that must be off during power-up. The zero-scale outputs enable glitch-free power-up.

The MAX5530 accepts an external reference input. The MAX5531 contains an internal reference and provides an external reference output. Both devices have force-sense-configured output buffers.

The MAX5530/MAX5531 are available in a 4mm x 4mm x 0.8mm, 12-pin, thin QFN package and are guaranteed over the extended -40°C to +85°C temperature range.

For 10-bit compatible devices, refer to the MAX5520/MAX5521 data sheet. For 8-bit compatible devices, refer to the MAX5510/MAX5511 data sheet.

Applications

- Portable Battery-Powered Devices
- Instrumentation
- Automatic Trimming and Calibration in Factory or Field
- Programmable Voltage and Current Sources
- Industrial Process Control and Remote Industrial Devices
- Remote Data Conversion and Monitoring
- Chemical Sensor Cell Bias for Gas Monitors
- Programmable Liquid Crystal Display (LCD) Bias

Selector Guide

PART	REFERENCE	TOP MARK
MAX5530ETC	External	AACS
MAX5531ETC	Internal	AACT

Rail-to-Rail is a registered trademark of Nippon Motorola, Inc.
SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp

Features

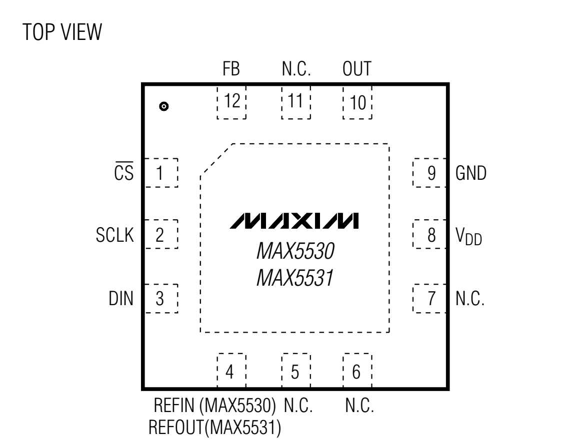
- ♦ **Ultra-Low 6µA Supply Current**
- ♦ **Shutdown Mode Reduces Supply Current to 0.18µA (max)**
- ♦ **Single +1.8V to +5.5V Supply**
- ♦ **Small 4mm x 4mm x 0.8mm Thin QFN Package**
- ♦ **Flexible Force-Sense-Configured Rail-to-Rail Output Buffers**
- ♦ **Internal Reference Sources 8mA of Current (MAX5531)**
- ♦ **Fast 16MHz 3-Wire SPI-/QSPI-/MICROWIRE-Compatible Serial Interface**
- ♦ **TTL- and CMOS-Compatible Digital Inputs with Hysteresis**
- ♦ **Glitch-Free Outputs During Power-Up**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5530ETC	-40°C to +85°C	12 Thin QFN-EP*
MAX5531ETC	-40°C to +85°C	12 Thin QFN-EP*

**EP = Exposed paddle (internally connected to GND).*

Pin Configuration



THIN QFN

Ultra-Low-Power, 12-Bit, Voltage-Output DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ....-0.3V to +6V
OUT to GND ....-0.3V to (V_{DD} + 0.3V)
FB to GND ....-0.3V to (V_{DD} + 0.3V)
SCLK, DIN, $\overline{CS}$ to GND ....-0.3V to (V_{DD} + 0.3V)
REFIN, REFOUT to GND ....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Thin QFN (derate 16.9mW/°C above +70°C 1349mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Junction Temperature .... +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +1.8V to +5.5V, OUT unloaded, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY (MAX5530 EXTERNAL REFERENCE)						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	V_{DD} = 5V, V_{REF} = 4.096V		±4	±8	LSB
		V_{DD} = 1.8V, V_{REF} = 1.024V		±4	±8	
Differential Nonlinearity (Note 1)	DNL	Guaranteed monotonic, V_{DD} = 5V, V_{REF} = 4.096V		±0.2	±1	LSB
		Guaranteed monotonic, V_{DD} = 1.8V, V_{REF} = 1.024V		±0.2	±1	
Offset Error (Note 2)	V_{OS}	V_{DD} = 5V, V_{REF} = 4.096V		±1	±20	mV
		V_{DD} = 1.8V, V_{REF} = 1.024V		±1	±20	
Offset-Error Temperature Drift				±2		µV/°C
Gain Error (Note 3)	GE	V_{DD} = 5V, V_{REF} = 4.096V		±2	±4	LSB
		V_{DD} = 1.8V, V_{REF} = 1.024V		±2	±4	
Gain-Error Temperature Coefficient				±4		ppm/°C
Power-Supply Rejection Ratio	PSRR	1.8V ≤ V_{DD} ≤ 5.5V		85		dB
STATIC ACCURACY (MAX5531 INTERNAL REFERENCE)						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	V_{DD} = 5V, V_{REF} = 3.9V		±4	±8	LSB
		V_{DD} = 1.8V, V_{REF} = 1.2V		±4	±8	
Differential Nonlinearity (Note 1)	DNL	Guaranteed monotonic, V_{DD} = 5V, V_{REF} = 3.9V		±0.2	±1	LSB
		Guaranteed monotonic, V_{DD} = 1.8V, V_{REF} = 1.2V		±0.2	±1	
Offset Error (Note 2)	V_{OS}	V_{DD} = 5V, V_{REF} = 3.9V		±1	±20	mV
		V_{DD} = 1.8V, V_{REF} = 1.2V		±1	±20	
Offset-Error Temperature Drift				±2		µV/°C
Gain Error (Note 3)	GE	V_{DD} = 5V, V_{REF} = 3.9V		±2	±4	LSB
		V_{DD} = 1.8V, V_{REF} = 1.2V		±2	±4	
Gain-Error Temperature Coefficient				±4		ppm/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.8V to +5.5V, OUT unloaded, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	1.8V ≤ V_{DD} ≤ 5.5V		85		dB
REFERENCE INPUT (MAX5530)						
Reference-Input Voltage Range	V_{REFIN}		0		V_{DD}	V
Reference-Input Impedance	R_{REFIN}	Normal operation	4.1			MΩ
		In shutdown		2.5		GΩ
REFERENCE OUTPUT (MAX5531)						
Initial Accuracy	V_{REFOUT}	No external load, V_{DD} = 1.8V	1.197	1.214	1.231	V
		No external load, V_{DD} = 2.5V	1.913	1.940	1.967	
		No external load, V_{DD} = 3V	2.391	2.425	2.459	
		No external load, V_{DD} = 5V	3.828	3.885	3.941	
Output-Voltage Temperature Coefficient	V_{TEMPCO}	T_A = -40°C to +85°C (Note 4)		12	30	ppm/°C
Line Regulation		V_{REFOUT} < V_{DD} - 200mV (Note 5)		2	200	µV/V
Load Regulation		0 ≤ I_{REFOUT} ≤ 1mA, sourcing, V_{DD} = 1.8V, V_{REF} = 1.2V		0.3	2	µV/µA
		0 ≤ I_{REFOUT} ≤ 8mA, sourcing, V_{DD} = 5V, V_{REF} = 3.9V		0.3	2	
		-150µA ≤ I_{REFOUT} ≤ 0, sinking		0.2		
Output Noise Voltage		0.1Hz to 10Hz, V_{REFOUT} = 3.9V		150		$µV_{P-P}$
		10Hz to 10kHz, V_{REFOUT} = 3.9V		600		
		0.1Hz to 10Hz, V_{REFOUT} = 1.2V		50		
		10Hz to 10kHz, V_{REFOUT} = 1.2V		450		
Short-Circuit Current (Note 6)		V_{DD} = 5V		30		mA
		V_{DD} = 1.8V		14		
Capacitive Load Stability Range		(Note 7)		0 to 10		nF
Thermal Hysteresis		(Note 8)		200		ppm
Reference Power-Up Time (from Shutdown)		REFOUT unloaded, V_{DD} = 5V		5.4		ms
		REFOUT unloaded, V_{DD} = 1.8V		4.4		
Long-Term Stability				200		ppm/ 1khrs
DAC OUTPUT (OUT)						
Capacitive Driving Capability	C_L			1000		pF
Short-Circuit Current (Note 6)		V_{DD} = 5V, V_{OUT} set to full scale, OUT shorted to GND, source current			65	mA
		V_{DD} = 5V, V_{OUT} set to 0V, OUT shorted to V_{DD}, sink current			65	
		V_{DD} = 1.8V, V_{OUT} set to full scale, OUT shorted to GND, source current			14	
		V_{DD} = 1.8V, V_{OUT} set to 0V, OUT shorted to V_{DD}, sink current			14	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.8V to +5.5V, OUT unloaded, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC Power-Up Time		Coming out of shutdown (MAX5530)	V_{DD} = 5V		3		ms
			V_{DD} = 1.8V		3.8		
		Coming out of standby (MAX5531)	V_{DD} = 1.8V to 5.5V		0.4		
Output Power-Up Glitch		C_L = 100pF			10		mV
FB_ Input Current					10		pA
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$)							
Input High Voltage	V_{IH}	4.5V ≤ V_{DD} ≤ 5.5V		2.4			V
		2.7V < V_{DD} ≤ 3.6V		2.0			
		1.8V ≤ V_{DD} ≤ 2.7V		0.7 x V_{DD}			
Input Low Voltage	V_{IL}	4.5V ≤ V_{DD} ≤ 5.5V				0.8	V
		2.7V < V_{DD} ≤ 3.6V				0.6	
		1.8V ≤ V_{DD} ≤ 2.7V				0.3 x V_{DD}	
Input Leakage Current	I_{IN}	(Note 9)			±0.05	±0.5	µA
Input Capacitance	C_{IN}				10		pF
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	Positive and negative (Note 10)			10		V/ms
Voltage-Output Settling Time		0.1 to 0.9 of full scale to within 0.5 LSB (Note 10)			660		µs
Output Noise Voltage		0.1Hz to 10Hz	V_{DD} = 5V		80		μV_{P-P}
			V_{DD} = 1.8V		55		
		10Hz to 10kHz	V_{DD} = 5V		620		
			V_{DD} = 1.8V		476		
POWER REQUIREMENTS							
Supply Voltage Range	V_{DD}			1.8		5.5	V
Supply Current (Note 9)	I_{DD}	MAX5530	V_{DD} = 5V		2.6	4	µA
			V_{DD} = 3V		2.6	4	
			V_{DD} = 1.8V		3.6	5	
		MAX5531	V_{DD} = 5V		5.3	7.0	
			V_{DD} = 3V		4.8	7.0	
			V_{DD} = 1.8V		5.4	7.0	
Standby Supply Current	I_{DDSD}	(Note 9)	V_{DD} = 5V		3.3	4.5	µA
			V_{DD} = 3V		2.8	4.0	
			V_{DD} = 1.8V		2.4	3.5	
Shutdown Supply Current	I_{DDPD}	(Note 9)			0.05	0.25	µA

TIMING CHARACTERISTICS

(V_{DD} = +4.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (V_{DD} = 4.5V TO 5.5V)						
Serial Clock Frequency	f_{SCLK}		0		16.7	MHz
DIN to SCLK Rise Setup Time	t_{DS}		15			ns
DIN to SCLK Rise Hold Time	t_{DH}		0			ns
SCLK Pulse-Width High	t_{CH}		24			ns
SCLK Pulse-Width Low	t_{CL}		24			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		100			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		20			ns
SCLK Fall to $\overline{CS}$ Fall Setup	t_{CSO}		0			ns
$\overline{CS}$ Rise to SCK Rise Hold Time	t_{CS1}		20			ns

TIMING CHARACTERISTICS

(V_{DD} = +1.8V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (V_{DD} = 1.8V TO 5.5V)						
Serial Clock Frequency	f_{SCLK}		0		10	MHz
DIN to SCLK Rise Setup Time	t_{DS}		24			ns
DIN to SCLK Rise Hold Time	t_{DH}		0			ns
SCLK Pulse-Width High	t_{CH}		40			ns
SCLK Pulse-Width Low	t_{CL}		40			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		150			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		30			ns
SCLK Fall to $\overline{CS}$ Fall Setup	t_{CSO}		0			ns
$\overline{CS}$ Rise to SCK Rise Hold Time	t_{CS1}		30			ns

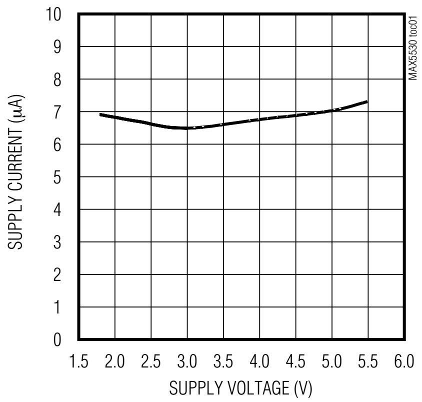
Note 1: Linearity is tested within codes 96 to 4080.
Note 2: Offset is tested at code 96.
Note 3: Gain is tested at code 4095. FB is connected to OUT.
Note 4: Guaranteed by design. Not production tested.
Note 5: V_{DD} must be a minimum of 1.8V.
Note 6: Outputs can be shorted to V_{DD} or GND indefinitely, provided that the package power dissipation is not exceeded.
Note 7: Optimal noise performance is at 2nF load capacitance.
Note 8: Thermal hysteresis is defined as the change in the initial +25°C output voltage after cycling the device from T_{MAX} to T_{MIN}.
Note 9: All digital inputs at V_{DD} or GND.
Note 10: Load = 10kΩ in parallel with 100pF, V_{DD} = 5V, V_{REF} = 4.096V (MAX5530) or V_{REF} = 3.9V (MAX5531).

Ultra-Low-Power, 12-Bit, Voltage-Output DACs

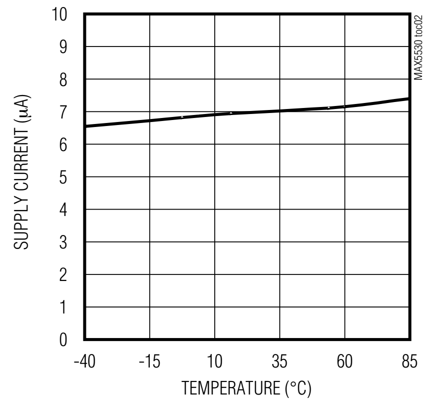
Typical Operating Characteristics

(V_{DD} = 5.0V, V_{REF} = 4.096V (MAX5530), V_{REF} = 3.9V (MAX5531), T_A = +25°C, unless otherwise noted.)

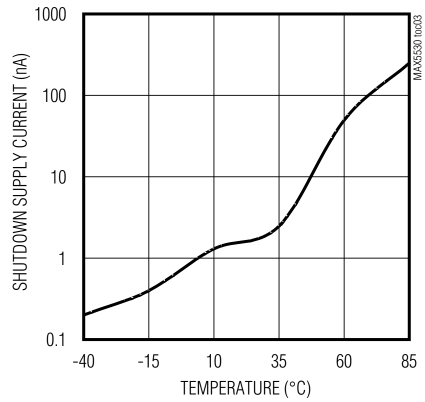
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX5531)



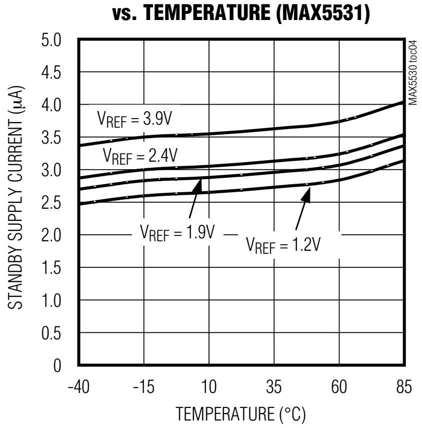
SUPPLY CURRENT vs. TEMPERATURE (MAX5531)



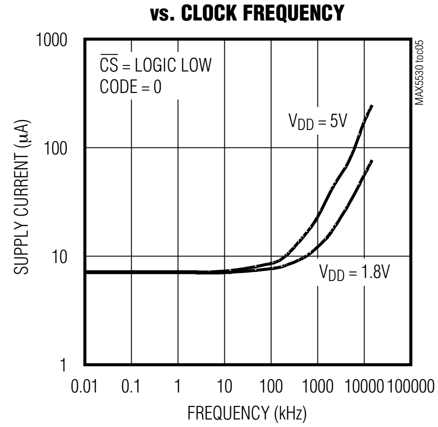
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE (MAX5531)



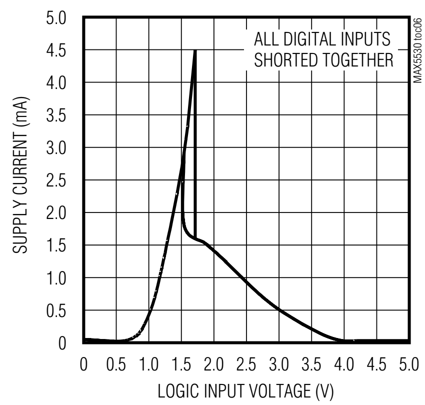
STANDBY SUPPLY CURRENT vs. TEMPERATURE (MAX5531)



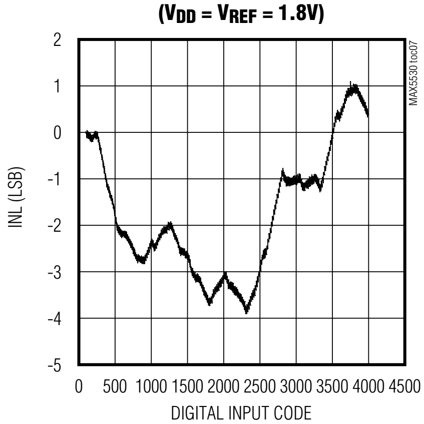
SUPPLY CURRENT vs. CLOCK FREQUENCY



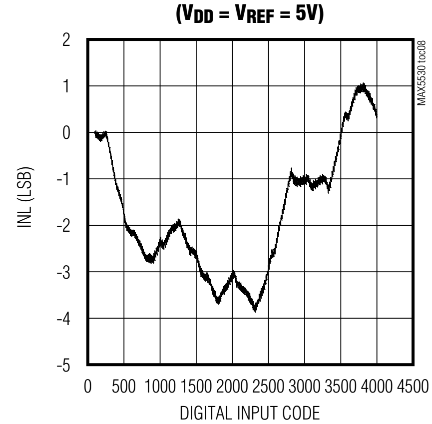
SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



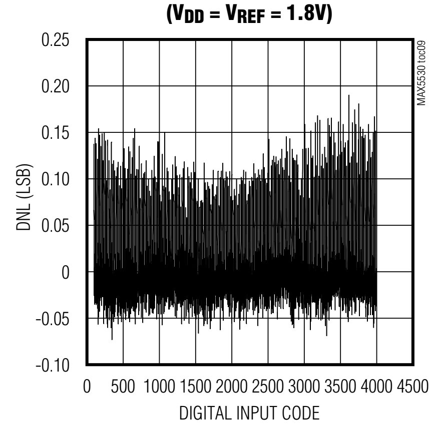
INL vs. INPUT CODE (V_{DD} = V_{REF} = 1.8V)



INL vs. INPUT CODE (V_{DD} = V_{REF} = 5V)



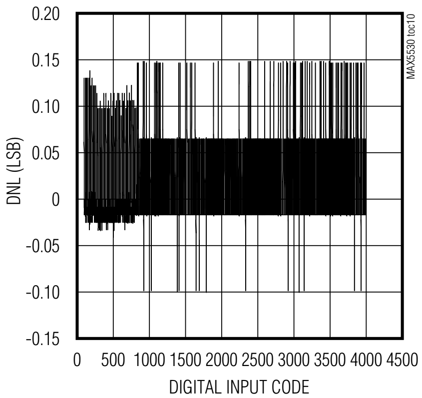
DNL vs. INPUT CODE (V_{DD} = V_{REF} = 1.8V)



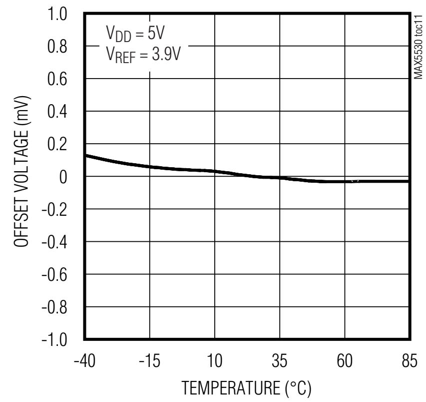
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{REF} = 4.096V (MAX5530), V_{REF} = 3.9V (MAX5531), T_A = +25°C, unless otherwise noted.)

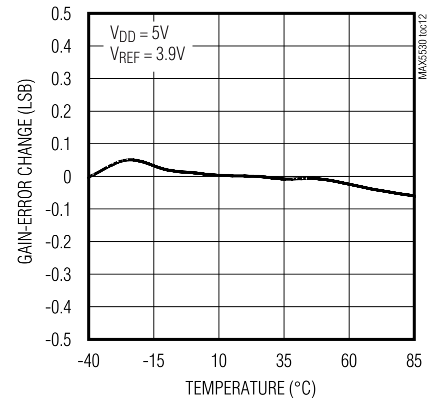
DNL vs. INPUT CODE (V_{DD} = V_{REF} = 5V)



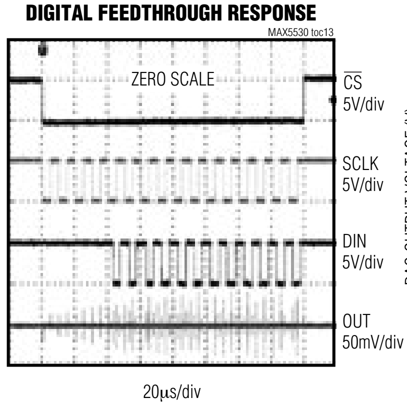
OFFSET VOLTAGE vs. TEMPERATURE



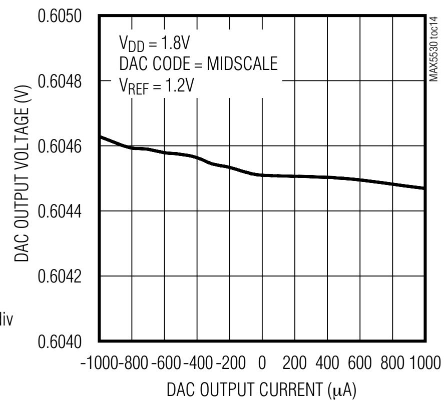
GAIN-ERROR CHANGE vs. TEMPERATURE



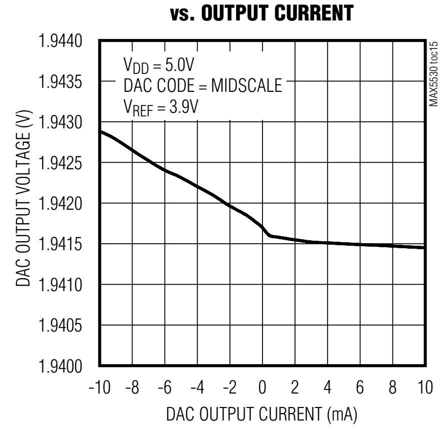
DIGITAL FEEDTHROUGH RESPONSE



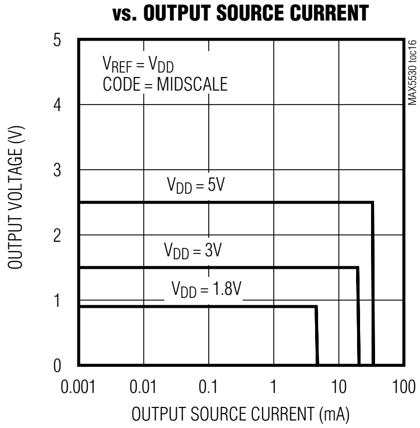
DAC OUTPUT LOAD REGULATION vs. OUTPUT CURRENT



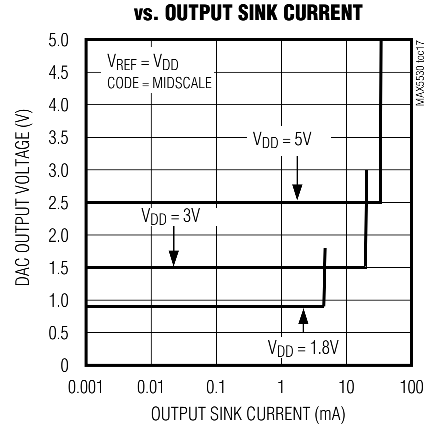
DAC OUTPUT LOAD REGULATION vs. OUTPUT CURRENT



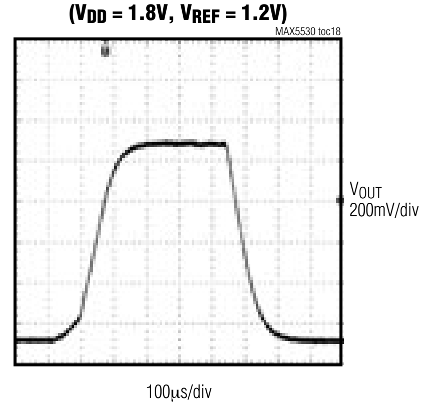
DAC OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



DAC OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



OUTPUT LARGE-SIGNAL STEP RESPONSE (V_{DD} = 1.8V, V_{REF} = 1.2V)

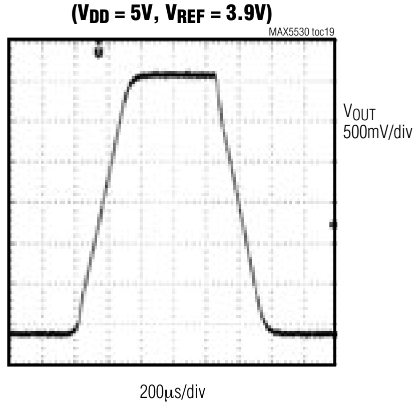


Ultra-Low-Power, 12-Bit, Voltage-Output DACs

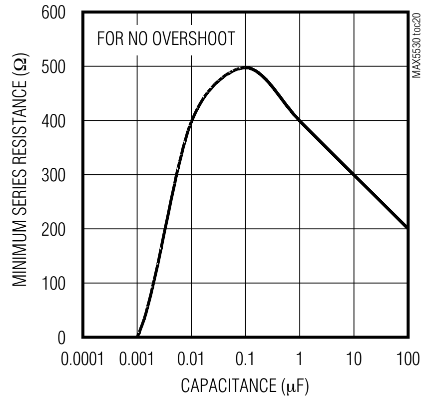
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{REF} = 4.096V (MAX5530), V_{REF} = 3.9V (MAX5531), T_A = +25°C, unless otherwise noted.)

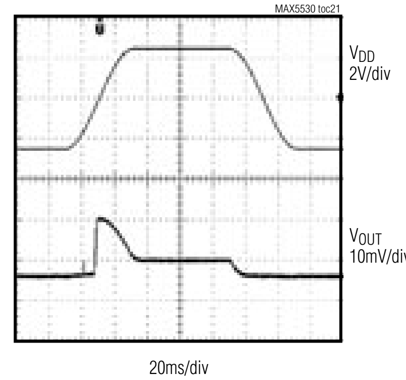
OUTPUT LARGE-SIGNAL STEP RESPONSE (V_{DD} = 5V, V_{REF} = 3.9V)



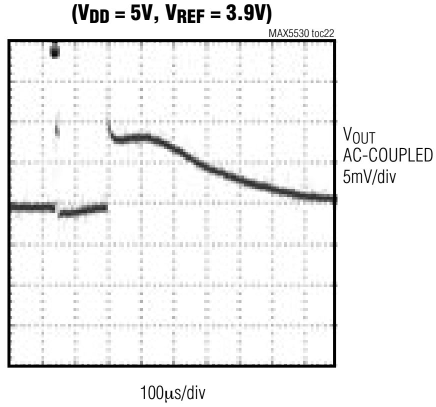
OUTPUT MINIMUM SERIES RESISTANCE vs. LOAD CAPACITANCE



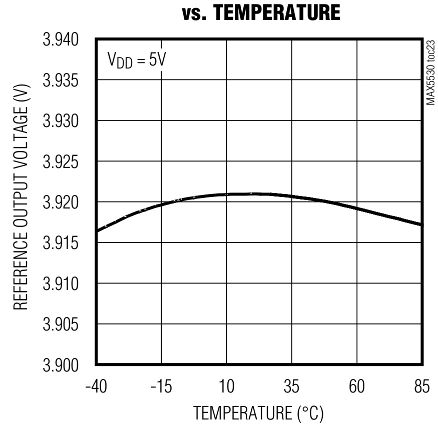
POWER-UP OUTPUT VOLTAGE GLITCH



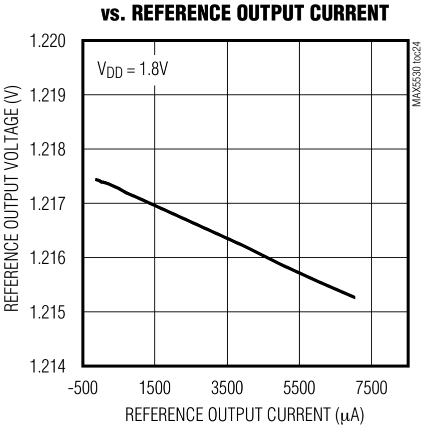
MAJOR CARRY OUTPUT VOLTAGE GLITCH (CODE 7FFh TO 800h) (V_{DD} = 5V, V_{REF} = 3.9V)



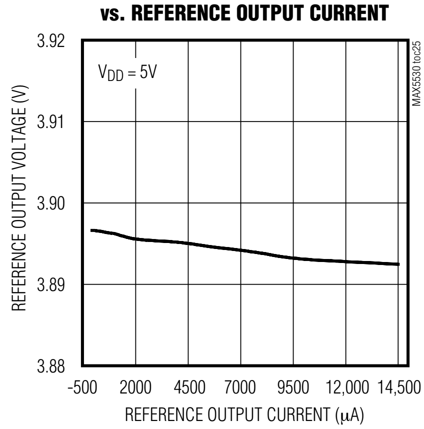
REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



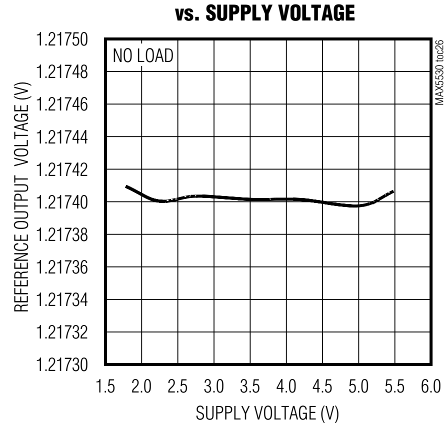
REFERENCE OUTPUT VOLTAGE vs. REFERENCE OUTPUT CURRENT



REFERENCE OUTPUT VOLTAGE vs. REFERENCE OUTPUT CURRENT

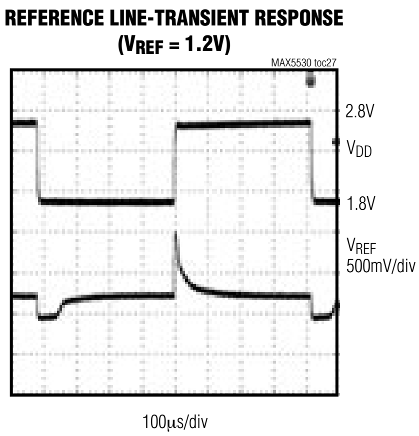


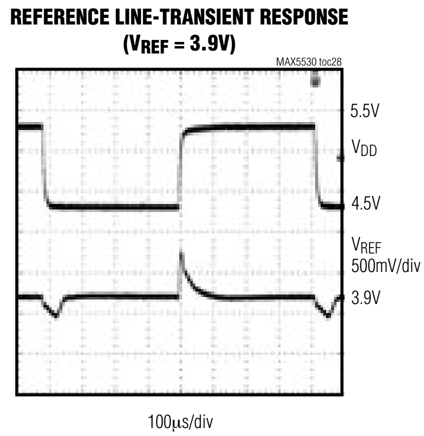
REFERENCE OUTPUT VOLTAGE vs. SUPPLY VOLTAGE

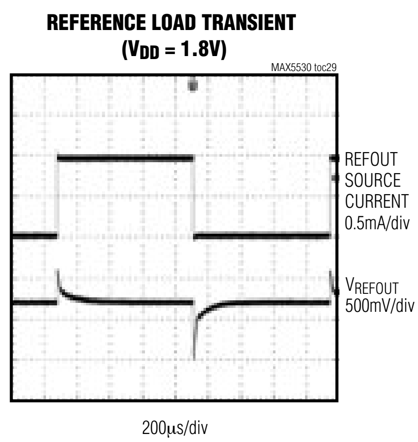


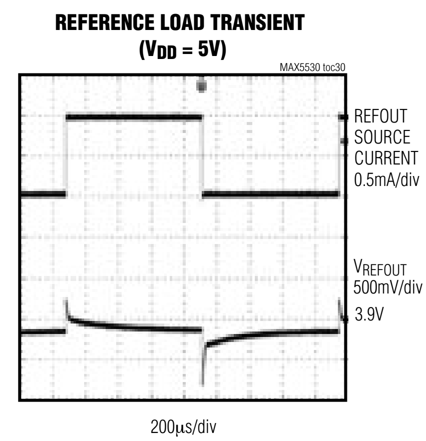
Typical Operating Characteristics (continued)

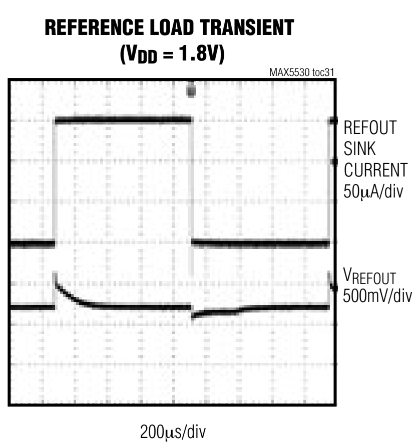
(V_{DD} = 5.0V, V_{REF} = 4.096V (MAX5530), V_{REF} = 3.9V (MAX5531), T_A = +25°C, unless otherwise noted.)

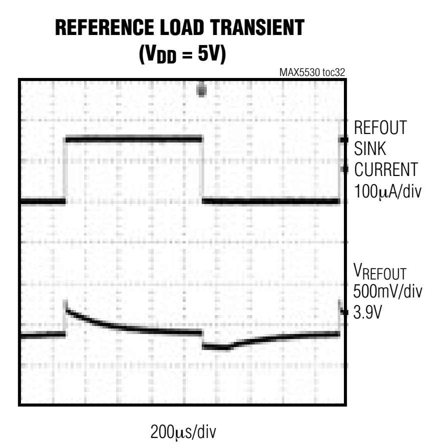








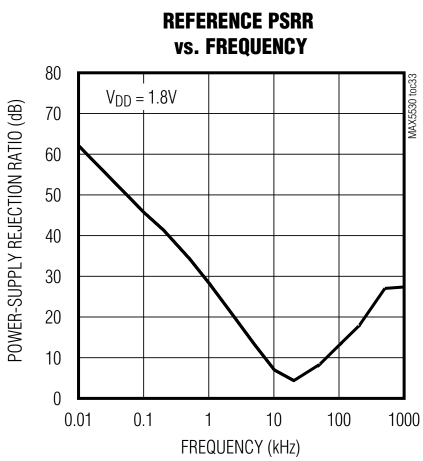


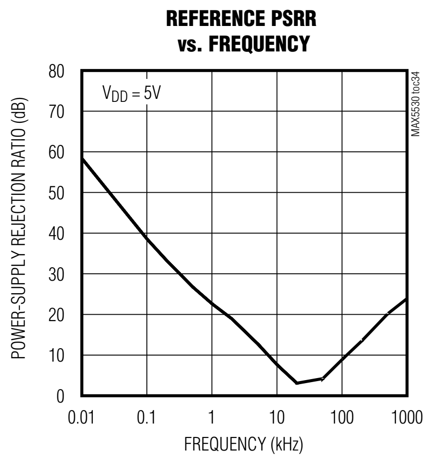


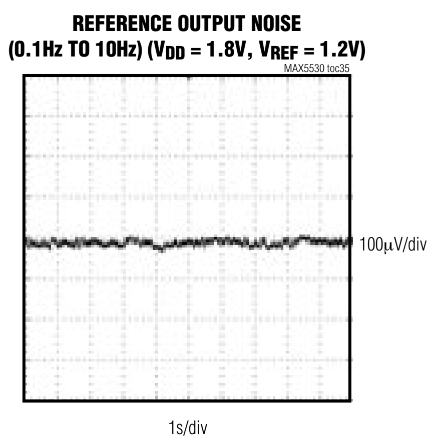
Ultra-Low-Power, 12-Bit, Voltage-Output DACs

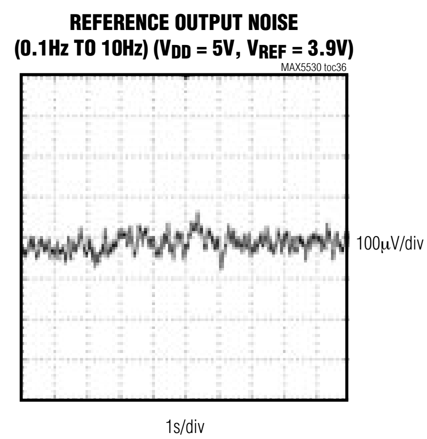
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{REF} = 4.096V (MAX5530), V_{REF} = 3.9V (MAX5531), T_A = +25°C, unless otherwise noted.)





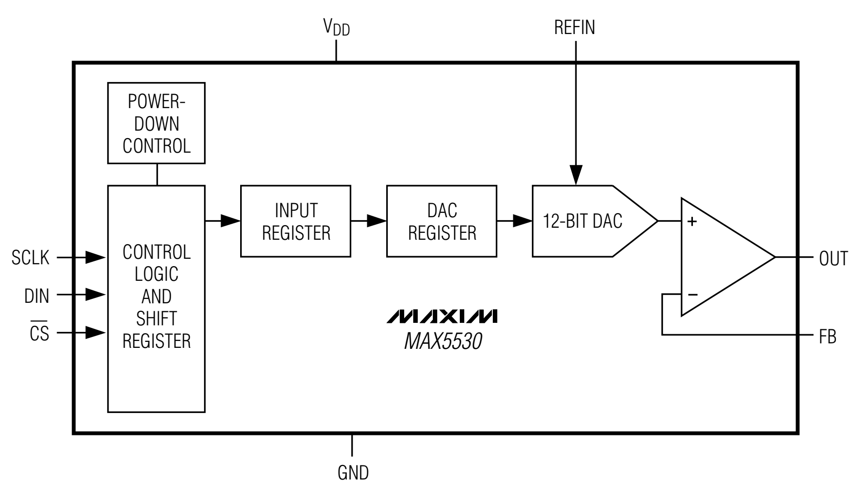




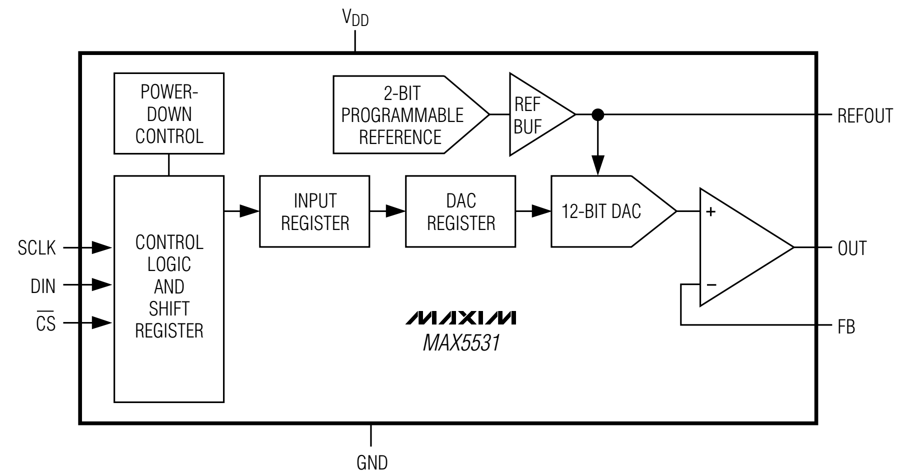
Pin Description

PIN		NAME	FUNCTION
MAX5530	MAX5531		
1	1	$\overline{CS}$	Active-Low Digital-Input Chip Select
2	2	SCLK	Serial-Interface Clock
3	3	DIN	Serial-Interface Data Input
4	—	REFIN	Reference Input
—	4	REFOUT	Reference Output
5, 6, 7, 11	5, 6, 7, 11	N.C.	No Connection. Leave N.C. inputs unconnected (floating) or connected to GND.
8	8	V_{DD}	Power Input. Connect V_{DD} to a 1.8V to 5.5V power supply. Bypass V_{DD} to GND with a 0.1µF capacitor.
9	9	GND	Ground
10	10	OUT	Analog Voltage Output
12	12	FB	Feedback Input
EP	EP	Exposed Paddle	Exposed Paddle. Connect EP to GND.

MAX5530 Functional Diagram



MAX5531 Functional Diagram



Detailed Description

The MAX5530/MAX5531 single, 12-bit, ultra-low-power, voltage-output DACs offer Rail-to-Rail buffered voltage outputs. The DACs operate from a 1.8V to 5.5V supply and require only 6µA (max) supply current. These devices feature a shutdown mode that reduces overall current, including the reference input current, to just 0.18µA. The MAX5531 includes an internal reference that saves additional board space and can source up to 8mA, making it functional as a system reference. The 16MHz, 3-wire serial interface is compatible with SPI, QSPI, and MICROWIRE protocols. When V_{DD} is applied, all DAC outputs are driven to zero scale with virtually no output glitch. The MAX5530/MAX5531 output buffers are configured in force sense allowing users to externally set voltage gains on the output (an output amplifier inverting input is available). These devices come in a 4mm x 4mm thin QFN package.

Digital Interface

The MAX5530/MAX5531 use a 3-wire serial interface compatible with SPI, QSPI, and MICROWIRE protocols (Figures 1 and 2).

The MAX5530/MAX5531 include a single, 16-bit, input shift register. Data loads into the shift register through the serial interface. $\overline{CS}$ must remain low until all 16 bits are clocked in. Data loads MSB first, D11–D0. The 16 bits consist of 4 control bits (C3–C0) and 12 data bits (D11–D0) (see Table 1). The control bits C3–C0 control the MAX5530/MAX5531, as outlined in Table 2.

Each DAC channel includes two registers: an input register and a DAC register. The input register holds input data. The DAC register contains the data updated to the DAC output.

The double-buffered register configuration allows any of the following:

- Loading the input registers without updating the DAC registers
- Updating the DAC registers from the input registers
- Updating all the input and DAC registers simultaneously

Table 1. Serial Write Data Format

CONTROL				DATA BITS											
MSB															**LSB**
C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

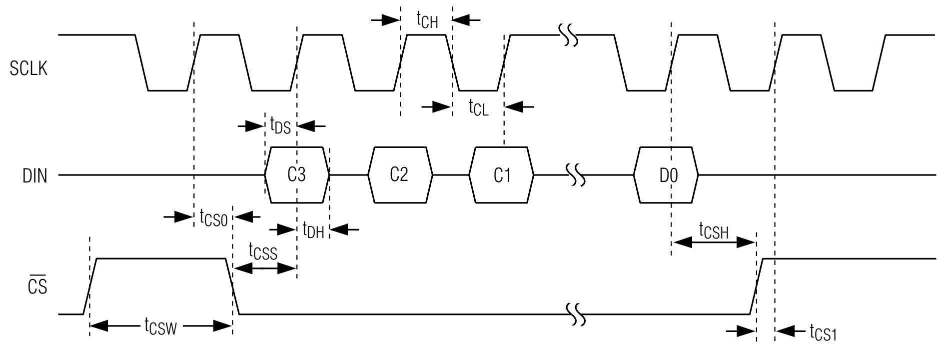


Figure 1. Timing Diagram

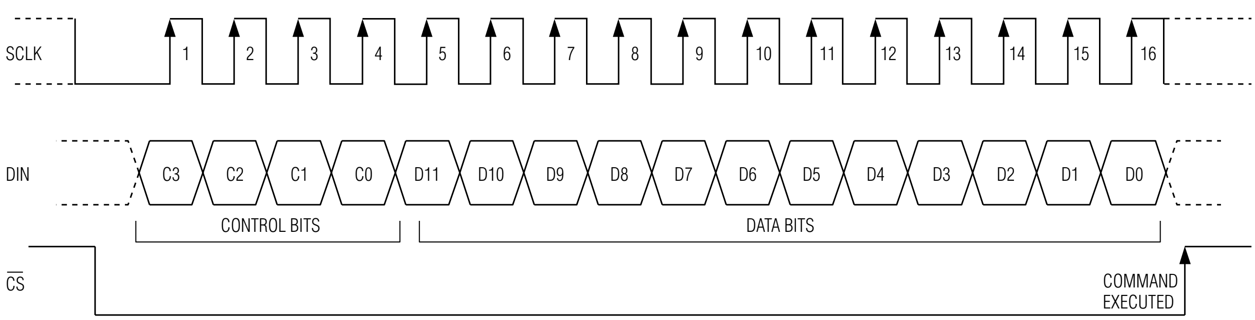


Figure 2. Register Loading Diagram

Ultra-Low-Power, 12-Bit, Voltage-Output DACs

Table 2. Serial-Interface Programming Commands

CONTROL BITS				INPUT DATA	FUNCTION
C3	C2	C1	C0	D11–D0	
0	0	0	0	XXXXXXXXXXXX	No operation; command is ignored.
0	0	0	1	12-bit data	Load input register from shift register; DAC register unchanged; DAC output unchanged.
0	0	1	0	—	Command reserved; do not use.
0	0	1	1	—	Command reserved; do not use.
0	1	0	0	—	Command reserved; do not use.
0	1	0	1	—	Command reserved; do not use.
0	1	1	0	—	Command reserved; do not use.
0	1	1	1	—	Command reserved; do not use.
1	0	0	0	12-bit data	Load DAC register from input register; DAC output updated; MAX5530 enters normal operation if in shutdown; MAX5531 enters normal operation if in standby or shutdown.
1	0	0	1	12-bit data	Load input register and DAC register from shift register; DAC output updated; MAX5530 enters normal operation if in shutdown; MAX5531 enters normal operation if in standby or shutdown.
1	0	1	0	—	Command reserved; do not use.
1	0	1	1	—	Command reserved; do not use.
1	1	0	0	D11, D10, XXXXXXXXXX	MAX5530 enters shutdown; MAX5531 enters standby*. For the MAX5531, D11 and D10 configure the internal reference voltage (Table 3).
1	1	0	1	D11, D10, XXXXXXXXXX	MAX5530/MAX5531 enter normal operation; DAC output reflects existing contents of DAC register. For the MAX5531, D11 and D10 configure the internal reference voltage (Table 3).
1	1	1	0	D11, D10, XXXXXXXXXX	MAX5530/MAX5531 enter shutdown; DAC output set to high impedance. For the MAX5531, D11 and D10 configure the internal reference voltage (Table 3).
1	1	1	1	12-bit data	Load input register and DAC register from shift register; DAC output updated; MAX5530 enters normal operation if in shutdown; MAX5531 enters normal operation if in standby or shutdown.

X = Don't care.
**Standby mode can be entered from normal operation only. It is not possible to enter standby mode from shutdown.*

Power Modes

The MAX5530/MAX5531 feature two power modes to conserve power during idle periods. In normal operation, the device is fully operational. In shutdown mode, the device is completely powered down, including the internal voltage reference in the MAX5531. The MAX5531 also offers a standby mode where all circuitry is powered down except the internal voltage reference. Standby mode keeps the reference powered up while the remaining circuitry is shut down, allowing it to be used as a system reference. Standby mode also helps reduce the wake-up delay by not requiring the reference to power up when returning to normal operation.

Shutdown Mode

The MAX5530/MAX5531 feature a software-programmable shutdown mode that reduces the typical supply current and the reference input current to 0.18µA (max). Writing an input control word with control bits C[3:0] = 1110 places the device in shutdown mode (Table 2). In shutdown, the MAX5530 reference input and DAC output buffers go high impedance. Placing the MAX5531 into shutdown turns off the internal reference, and the DAC output buffers go high impedance. The serial interface remains active for all devices.

Table 2 shows several commands that bring the MAX5530/MAX5531 back to normal operation. The power-up time from shutdown is required before the DAC outputs are valid.

Note: For the MAX5531, standby mode cannot be entered directly from shutdown mode. The device must be brought into normal operation before entering standby mode.

Table 3. Reference Output Voltage Programming

D11	D10	REFERENCE VOLTAGE (V)
0	0	1.214
0	1	1.940
1	0	2.425
1	1	3.885

Standby Mode (MAX5531 Only)

The MAX5531 features a software-programmable standby mode that reduces the typical supply current to 6µA. Standby mode powers down all circuitry except the internal voltage reference. Place the device in standby mode by writing an input control word with control bits C[3:0] = 1100 (Table 2). The internal reference and serial interface remain active while the DAC output buffers go high impedance. If the MAX5531 is coming out of standby, the power-up time from standby is required before the DAC outputs are valid.

For the MAX5531, standby mode cannot be entered directly from shutdown mode. The device must be brought into normal operation before entering standby mode. To enter standby from shutdown, issue the command to return to normal operation, followed immediately by the command to go into standby.

Table 2 shows several commands that bring the MAX5531 back to normal operation. When transitioning from standby mode to normal operation, only the DAC power-up time is required before the DAC outputs are valid.

Reference Input

The MAX5530 accepts a reference with a voltage range extending from 0 to V_{DD}. The output voltage (V_{OUT}) is represented by a digitally programmable voltage source as:

$$V_{OUT} = (V_{REF} \times N / 4096) \times gain$$

where N is the numeric value of the DAC's binary input code (0 to 4095), V_{REF} is the reference voltage and gain is the externally set voltage gain for the MAX5530/ MAX5531.

In shutdown mode, the reference input enters a high-impedance state with an input impedance of 2.5GΩ (typ).

Reference Output

The MAX5531 internal voltage reference is software configurable to one of four voltages. Upon power-up, the default reference voltage is 1.214V. Configure the reference voltage using the D11 and D10 data bits (Table 3) when the control bits are as follows C[3:0] = 1100, 1101, or 1110 (Table 2). V_{DD} must be kept at a minimum of 200mV above V_{REF} for proper operation.

Applications Information

1-Cell and 2-Cell Circuit

See Figure 3 for an illustration of how to power the MAX5530/MAX5531 with either one lithium-ion battery or two alkaline batteries. The low current consumption of the devices makes the MAX5530/MAX5531 ideal for battery-powered applications.

Programmable Current Source

See the circuit in Figure 4 for an illustration of how to configure the MAX5530 as a programmable current source for driving an LED. The MAX5530 drives a standard NPN transistor to program the current source. The current source (I_{LED}) is defined in the equation in Figure 4.

Voltage Biasing a Current-Output Transducer

See the circuit in Figure 5 for an illustration of how to configure the MAX5530 to bias a current output transducer. In Figure 5, the output voltage of the MAX5530 is a function of the voltage drop across the transducer added to the voltage drop across the feedback resistor R.

Self-Biased Two-Electrode Potentiostat Application

See the circuit in Figure 6 for an illustration of how to use the MAX5531 to bias a two-electrode potentiostat on the input of an ADC.

Unipolar Output

Figure 7 shows the MAX5530 in a unipolar output configuration with unity gain. Table 4 lists the unipolar output codes.

Bipolar Output

The MAX5530 output can be configured for bipolar operation, as shown in Figure 8. The output voltage is given by the following equation:

$$V_{OUT} = V_{REF} \times [(N_A - 2048) / 2048]$$

where N_A represents the numeric value of the DAC's binary input code. Table 5 shows digital codes (offset binary) and the corresponding output voltage for the circuit in Figure 4.

Configurable Output Gain

The MAX5530/MAX5531 have a force-sense output, which provides a connection directly to the inverting terminal of the output op amp, yielding the most flexibility. The advantage of the force-sense output is that specific gains can be set externally for a given application. The gain error for the MAX5530/MAX5531 is specified in a unity-gain configuration (op-amp output and inverting terminals connected), and additional gain error results from external resistor tolerances. Another advantage of the force-sense DAC is that it allows many useful circuits to be created with only a few simple external components.

An example of a custom fixed gain using the force-sense output of the MAX5530/MAX5531 is shown in Figure 9. In this example, R1 and R2 set the gain for V_{OUT}.

$$V_{OUT} = [(V_{REFIN} \times N_A) / 4096] \times [1 + (R2 / R1)]$$

where N_A represents the numeric value of the DAC input code.

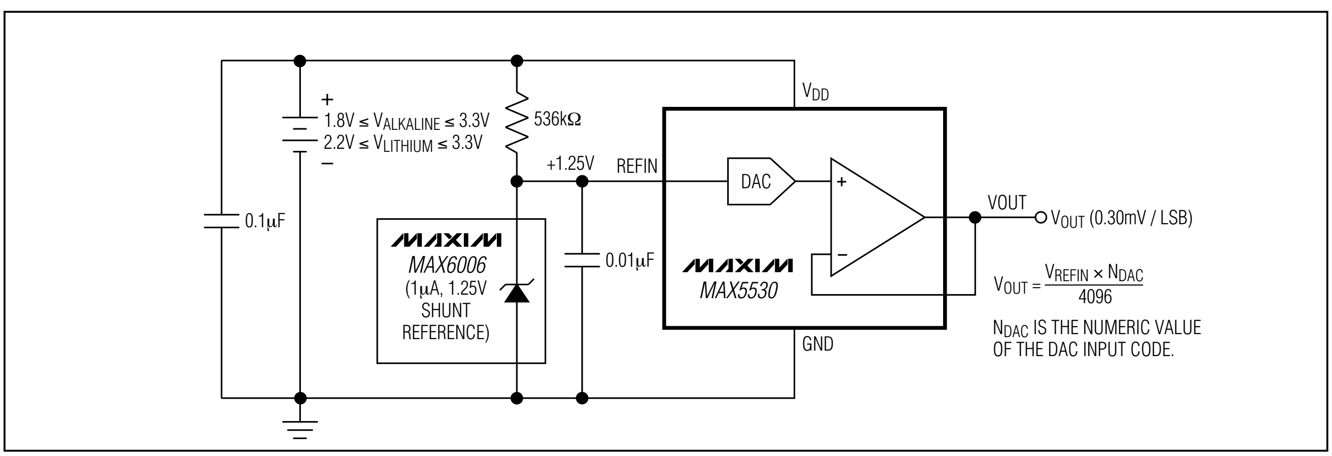


Figure 3. Portable Application Using Two Alkaline Cells or One Lithium Coin Cell

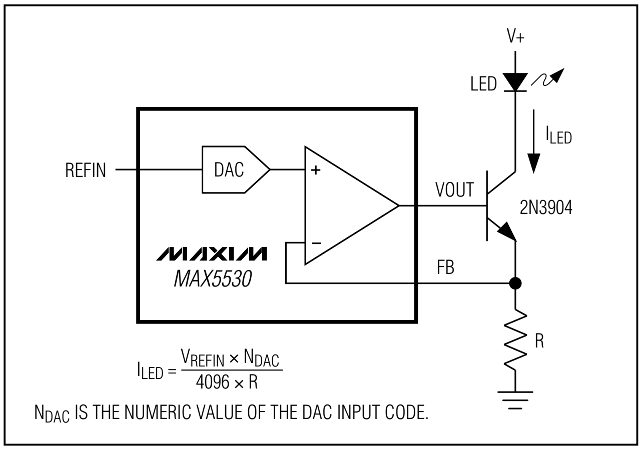


Figure 4. Programmable Current Source Driving an LED

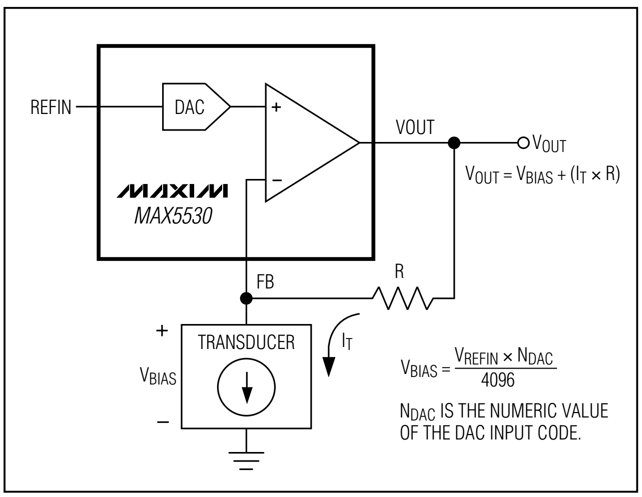


Figure 5. Transimpedance Configuration for a Voltage-Biased Current-Output Transducer

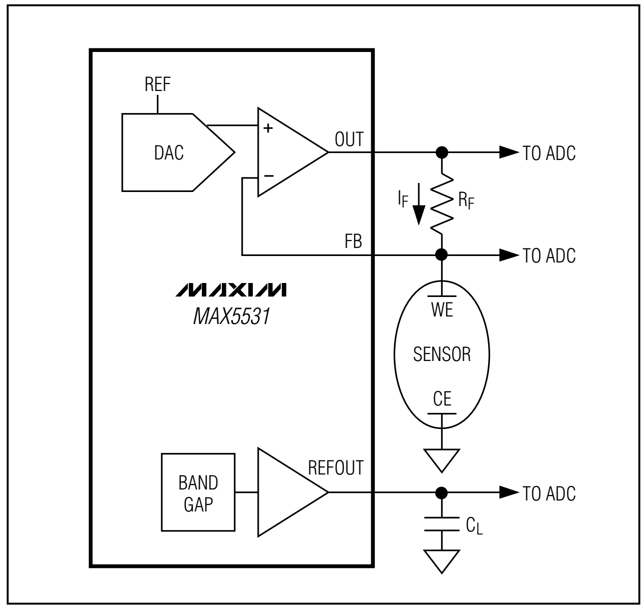


Figure 6. Self-Biased Two-Electrode Potentiostat Application

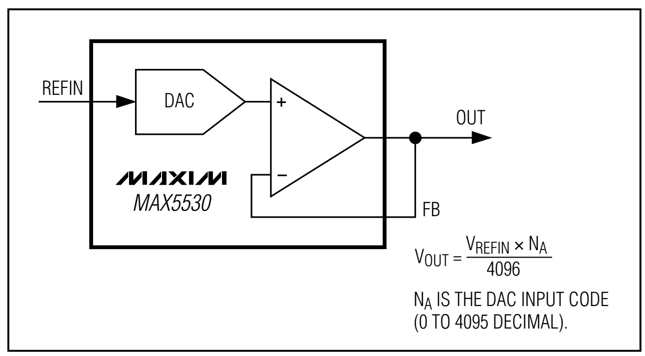


Figure 7. Unipolar Output Circuit

Table 4. Unipolar Code Table (Gain = +1)

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1100	$+V_{REF}$ (4095/4096)
1000	0000	0001	$+V_{REF}$ (2049/4096)
1000	0000	0000	$+V_{REF}$ (2048/4096) = $+V_{REF}$ / 2
0111	1111	1111	$+V_{REF}$ (2047/4096)
0000	0001	0001	$+V_{REF}$ (1/4096)
0000	0000	0000	0V

Table 5. Bipolar Code Table (Gain = +1)

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF}$ (2047/2048)
1000	0000	0001	$+V_{REF}$ (1/2048)
1000	0000	0000	0V
0111	1111	1111	$-V_{REF}$ (1/2048)
0000	0000	0001	$-V_{REF}$ (2047/2048)
0000	0000	0000	$-V_{REF}$ (2048/2048) = $-V_{REF}$

Ultra-Low-Power, 12-Bit, Voltage-Output DACs

Power Supply and Bypassing Considerations

Bypass the power supply with a 0.1µF capacitor to GND. Minimize lengths to reduce lead inductance. If noise becomes an issue, use shielding and/or ferrite beads to increase isolation. For the thin QFN package, connect the exposed paddle to ground.

Layout Considerations

Digital and AC transient signals coupling to GND can create noise at the output. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane. Wire-wrapped boards and sockets are not recommended. For optimum system performance, use printed circuit (PC) boards. Good PC board ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines.

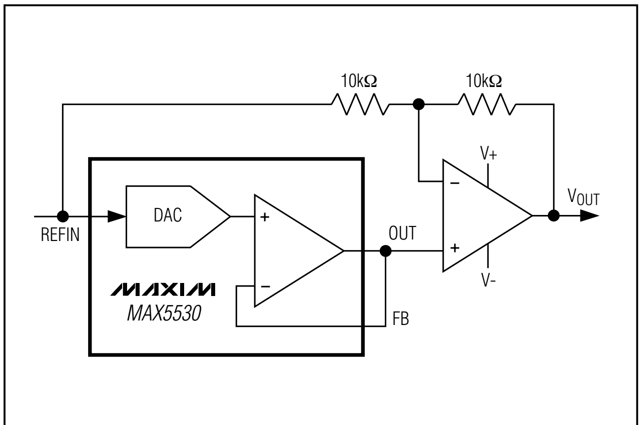


Figure 8. Bipolar Output Circuit

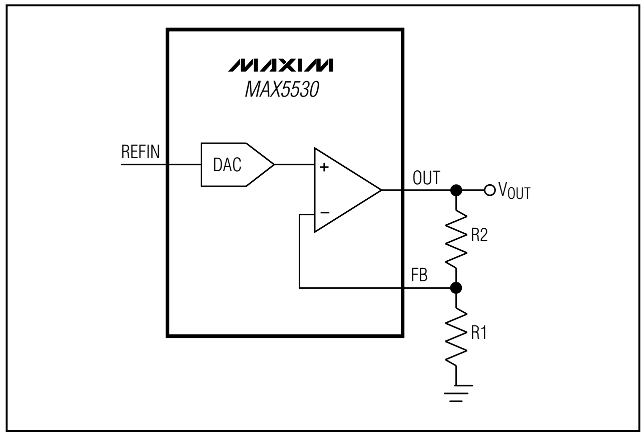
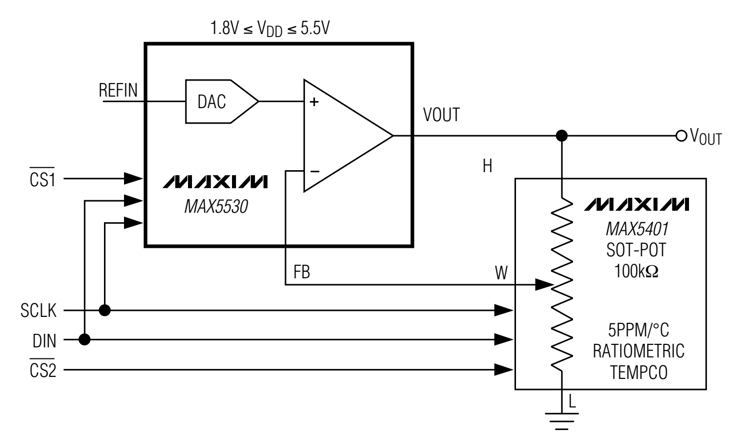


Figure 9. Separate Force-Sense Outputs Create Unity and Greater-than-Unity DAC Gains Using the Same Reference



$$V_{OUT} = \frac{V_{REFIN} \times N_{DAC}}{4096}\left(1 + \frac{255 - N_{POT}}{255}\right)$$

Figure 10. Software-Configurable Output Gain

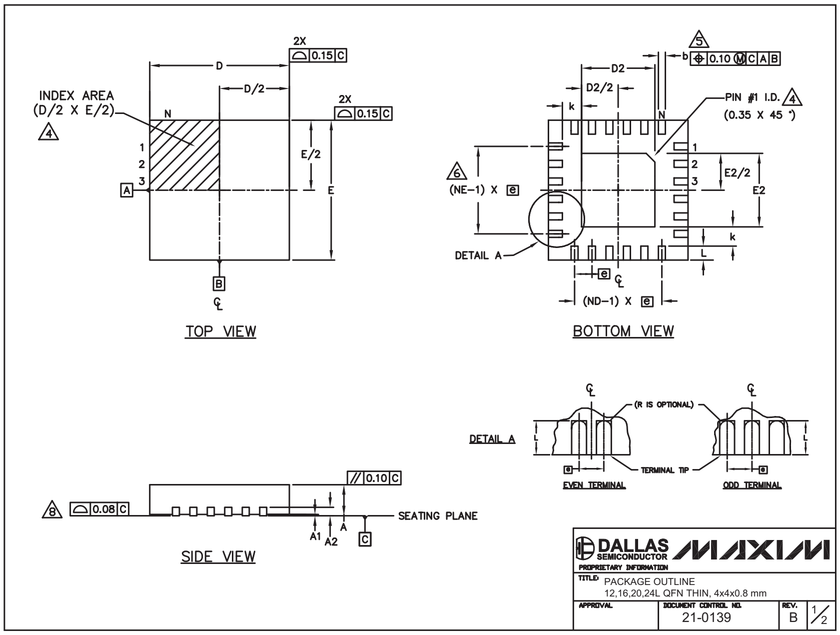
Chip Information

TRANSISTOR COUNT: 10,688

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. (△) THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. (△) DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. (△) ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. (△) COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV. B | 2/2

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.