SN75LVCP600S 1.5-, 3.0-, and 6.0-Gbps SATA/SAS Redriver

1 Features

- Single 3.3-V Supply
- Suitable to Receive 6-Gbps Data Over up to >40 Inches (1 m) of FR4 PCB
- Two-Level RX and TX Equalization
  - RX→ 7, 15 dB
  - TX→ 0, –1.3 dB
- Pin-Selectable SATA/SAS Signaling
- Programmable Squelch Threshold for Long Channels
- Low Power in Active, Partial, and Slumber States
  - 106 mW Typical (Active Mode at 6 Gbps)
  - <11 mW (When Link in Partial and Slumber State)
- Ultra-small Package for Optimal Placement
  - 10-Pad 2.5-mm × 2.5-mm QFN
- High ESD-Transient Protection
  - HBM: 9,000 V
  - CDM: 1,500 V
  - MM: 200 V

2 Applications

- Notebook and Desktop PCs
- Docking Stations
- Active Cable
- Servers
- Workstations

3 Description

The SN75LVCP600S is a single-channel SATA/SAS signal conditioner supporting data rates up to 6 Gbps. The device complies with SATA physical spec rev 3.0 and SAS electrical spec 2.0. The SN75LVCP600S operates from a single 3.3-V supply and has 100-Ω line termination with a self-biasing feature, making the device suitable for AC coupling. The inputs incorporate an out-of-band (OOB) detector, which automatically squelches the output while maintaining a stable common-mode voltage compliant to the SATA/SAS link.

The SN75LVCP600S handles interconnect losses at its input with selectable equalization settings that can be programmed to the match loss in the channel. For data rates of 3 Gbps and lower, the LVCP600S equalizes signals for a span of up to 50 inches of FR4 board material. For data rates of 6 Gbps, the device compensates >40 inches (1 m) of FR4 material. Rx/Tx equalization level is controlled by the setting of signal control pins EQ and DE.

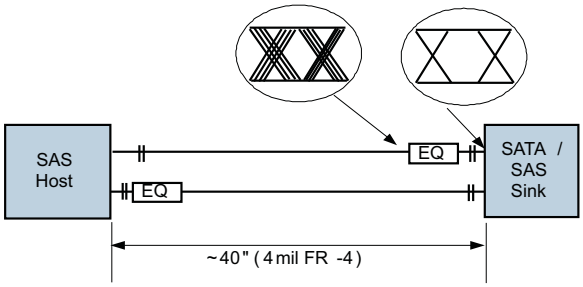
The device is hot-plug capable (requires use of AC-coupling capacitors at differential inputs and outputs), preventing device damage during device *hot*-insertion such as async signal plug/removal, unpowered plug/removal, powered plug/removal, or surprise plug/removal.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN75LVCP600S	SON (10)	2.50 mm x 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



EQ = LVCP600S

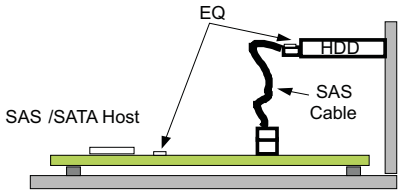


Table of Contents

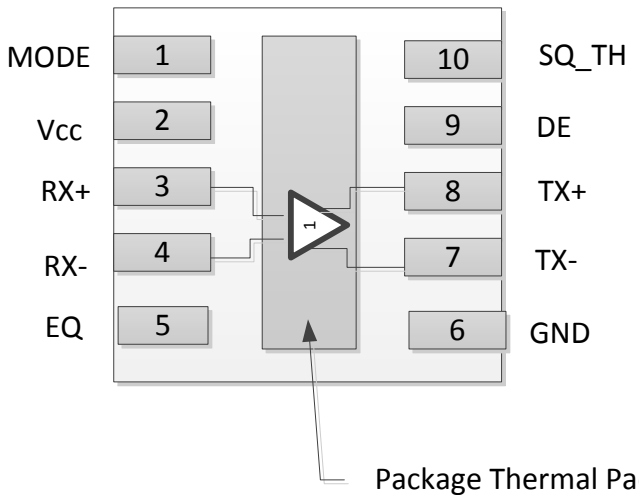
4 Revision History

Changes from Original (March 2011) to Revision A **Page**

- Added *Device Information* table, *ESD Ratings* table, *Timing Requirements* table, *Parameter Measurement Information* section, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support*, *Mechanical, Packaging, and Orderable Information* ... 1
- Changed pins TX+ and TX- I/O Type From: I, CML To: O, VML ... 3
- Changed pins TX+ and TX- Description From: "Non-inverting and inverting CML differential outputs." To: "Noninverting and inverting VML differential outputs." ... 3
- Deleted last bullet list item "The control pin pullup and pulldown resistors..." from the *Layout Guidelines* section ... 20

5 Pin Configuration and Functions

DSK Package
10-Pin (SON)
Top View



TI recommends soldering the package thermal pad to the ground plane for maximum thermal performance.

Pin Functions

PIN		I/O TYPE	DESCRIPTION
NO.	NAME		
HIGH SPEED DIFFERENTIAL I/O			
3	RX+	I, CML	Noninverting and inverting CML differential inputs. These pins are tied to an internal voltage bias by dual termination-resistor circuit.
4	RX–	I, CML	
8	TX+	O, VML	Noninverting and inverting VML differential outputs. These pins are tied to an internal voltage bias by dual termination-resistor circuit.
7	TX–	O, VML	
CONTROL PINS			
5	EQ	I, LVCMOS	Selects equalization settings per Table 1. Internally tied to GND
9	DE	I, LVCMOS	Selects de-emphasis settings per Table 1. Internally tied to GND
1	MODE	I, LVCMOS	Selects SATA or SAS output levels per Table 1. Internally tied to GND
10	SQ_TH	I, LVCMOS	Selects squelch threshold settings per Table 1. Internally tied to GND
POWER			
2	V_{CC}	Power	Positive supply must be 3.3 V ±10%
6	GND	Power	Supply ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage (2)	V_{CC}	–0.5	4	V
Voltage	Differential I/O	–0.5	4	V
	Control I/O	–0.5	V_{CC} + 0.5	V
Continuous power dissipation		See *Thermal Information* Table		
Storage temperature, T_A		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground terminal.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±9000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
	Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

typical values for all parameters are at V_{CC} = 3.3 V and T_A = 25°C; all temperature limits are specified by design

PARAMETER		MIN	NOM	MAX	UNITS
V_{CC}	Supply voltage	3	3.3	3.6	V
$C_{COUPLING}$	Coupling capacitor		12		nF
T_A	Operating free-air temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN75LVCP600S DSK (SON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
ICC_{Max}	Active mode supply current	MODE/EQ/DE/SQ_TH = NC, K28.5 pattern at 6 Gbps, V_{ID} = 700 mV_{pp}, (SATA mode)		29	41	mA
		MODE/EQ/DE/SQ_TH = V_{CC}, K28.5 pattern at 6 Gbps, V_{ID} = 700 mV_{pp}, (SAS mode)		32	45	
I_{CCPS}	Auto power-save mode I_{CC}	When auto low-power conditions are met		3.3	5	mA
	Maximum data rate				6	Gbps
OOB						
V_{OOB_SAS}	Input OOB threshold (output squelched below this level)	f = 750MHz; SQ_TH=0, MODE = 1, measured at receiver pin	88	112	131	mV_{pp}
		f = 750MHz; SQ_TH=1, MODE = 1, measured at receiver pin	67	85	100	
V_{OOB_SATA}	Input OOB threshold (output squelched below this level)	f = 750MHz; SQ_TH=0, MODE = 0, measured at receiver pin	40	66	86	
		f = 750MHz; SQ_TH=1, MODE = 0, measured at receiver pin	35	56	72	
$D_{VdiffOOB}$	OOB differential delta				25	mV
D_{VCMOOB}	OOB common-mode delta				50	mV
CONTROL LOGIC						
V_{IH}	High-level input voltage	For all control pins	1.4			V
V_{IL}	Low-level input voltage				0.5	V
VIN_{HYS}	Input hysteresis			115		mV
I_{IH}	High-level input current	MODE, SQ_TH = V_{CC}			30	µA
		EQ, DE = V_{CC}			20	
I_{IL}	Low-level input current	MODE, SQ_TH = GND	–30			
		EQ, DE = GND	–10			
RECEIVER AC/DC						
Z_{DIFFRX}	Differential input impedance		85	100	115	Ω
Z_{SERX}	Single-ended input impedance		40			Ω
VCM_{RX}	Common-mode voltage			1.7		V
RL_{DiffRX}	Differential mode return loss (RL)	f = 150 MHz–300 MHz	18	26		dB
		f = 300 MHz–600 MHz	14	23		
		f = 600 MHz–1.2 GHz	10	17		
		f = 1.2 GHz–2.4 GHz	8	14		
		f = 2.4 GHz–3 GHz	3	13		
$RX_{DiffRLSlope}$	Differential mode RL slope	f = 300 MHz–6 GHz		–13		dB/dec
RL_{CMRX}	Common-mode return loss	f = 150 MHz–300 MHz	5	10		dB
		f = 300 MHz–600 MHz	5	18		
		f = 600 MHz–1.2 GHz	2	16		
		f = 1.2 GHz–2.4 GHz	1	12		
		f = 2.4 GHz–3 GHz	1	12		
V_{diffRX}	Differential input voltage PP	MODE = 1, f = 1.5 GHz and 3 GHz	275		1600	mVpp
		MODE = 0, f = 1.5 GHz and 3 GHz	225		1600	

Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IB_{RX}	Impedance balance	f = 150 MHz–300 MHz	30	47		dB
		f = 300 MHz–600 MHz	30	40		
		f = 600 MHz–1.2 GHz	20	34		
		f = 1.2 GHz–2.4 GHz	10	28		
		f = 2.4 GHz–3. GHz	10	24		
		f = 3 GHz–5 GHz	4	22		
		f = 5 GHz–6.5 GHz	4	22		
TRANSMITTER AC/DC						
Z_{diffTX}	Pair differential impedance		85	100	122	Ω
Z_{SETX}	Single-ended input impedance		40			Ω
$V_{TXtrans}$	Sequencing transient voltage	Transient voltages on the serial data bus during power sequencing (lab load)	–1.2	0	1.2	V
RL_{DiffTX}	Differential mode return loss	f = 150 MHz–300 MHz	13	22		dB
		f = 300 MHz–600 MHz	8	21		
		f = 600 MHz–1.2 GHz	6	20		
		f = 1.2 GHz–2.4 GHz	6	17		
		f = 2.4 GHz–3 GHz	3	17		
$TX_{DiffRLSlope}$	Differential-mode RL slope	f = 300 MHz–3 GHz		–13		dB/dec
RL_{CMTX}	Common-mode return loss	f = 150 MHz–300 MHz	5	19		dB
		f = 300 MHz–600 MHz	5	16		
		f = 600 MHz–1.2 GHz	2	11		
		f = 1.2 GHz–2.4 GHz	1	9		
		f = 2.4 GHz–3 GHz	1	10		
IB_{TX}	Impedance balance	f = 150 MHz–300 MHz	30	43		dB
		f = 300 MHz–600 MHz	30	40		
		f = 600 MHz–1.2 GHz	20	32		
		f = 1.2 GHz–2.4 GHz	10	25		
		f = 2.4 GHz–3 GHz	10	27		
		f = 3 GHz–5 GHz	4	25		
		f = 5. GHz–6.5 GHz	4	26		
$Diff_{VppTX}$	Differential output-voltage swing	DE = 1, MODE = 1→(SAS), f = 3 GHz (under no interconnect loss)	385	850	1300	mVpp
		DE = 0, MODE = 0→(SATA), f = 3 GHz (under no interconnect loss)	400	600	800	
DE	De-emphasis level	DE = 1		–1.3		dB
		DE = 0		0		
VCM_{AC_TX}	TX AC CM voltage	At 1.5 GHz		20	50	mVpp
		At 3 GHz		11	26	dBmv (rms)
		At 6 GHz		13	30	
VCM_{TX}	Common-mode voltage			1.7		V
TxR/F_{lmb}	TX rise/fall imbalance	At 3 Gbps		3%	18%	
$TxAm_{plmb}$	TX amplitude imbalance			1.5%	10%	

Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSMITTER JITTER AT CP(1)						
3-Gbps SATA Mode						
TJ_{TX}	Total jitter(1)			0.26	0.38	UI_{pp}
DJ_{TX}	Deterministic jitter	V_{ID} = 500 mV_{pp}, UI = 333 ps, K28.5 control character, EQ/DE = 1		0.13	0.24	UI_{pp}
RJ_{TX}	Residual random jitter	V_{ID} = 500 mV_{pp}, UI = 333 ps, K28.7 control character, EQ/DE = 1		1.16	1.95	ps-rms
6-Gbps SATA Mode						
TJ_{TX}	Total jitter(1)			0.37	0.61	UI_{pp}
DJ_{TX}	Deterministic jitter	V_{ID} = 500 mV_{pp}, UI = 167 ps, K28.5 control character, EQ/DE = 1		0.12	0.32	UI_{pp}
RJ_{TX}	Residual random jitter	V_{ID} = 500 mV_{pp}, UI = 167 ps, K28.7 control character, EQ/DE = 1		1.15	2.2	ps-rms
3-Gbps SAS Mode						
TJ_{TX}	Total jitter(1)			0.25	0.37	UI_{pp}
DJ_{TX}	Deterministic jitter	V_{ID} = 500 mV_{pp}, UI = 333 ps, K28.5 control character, EQ/DE = 1		0.12	0.23	UI_{pp}
RJ_{TX}	Residual random jitter	V_{ID} = 500 mV_{pp}, UI = 333 ps, K28.7 control character, EQ/DE = 1		1.11	2	ps-rms
6-Gbps SAS Mode						
TJ_{TX}	Total jitter(1)			0.35	0.57	UI_{pp}
DJ_{TX}	Deterministic jitter	V_{ID} = 500 mV_{pp}, UI = 167 ps, K28.5 control character, EQ/DE = 1		0.10	0.29	UI_{pp}
RJ_{TX}	Residual random jitter	V_{ID} = 500 mV_{pp}, UI = 167 ps, K28.7 control character, EQ/DE = 1		1.1	2.14	ps-rms

(1) T_J = (14.1 × RJ_{SD} + DJ), where RJ_{SD} is one standard deviation value of RJ Gaussian distribution. Jitter measurement is at the CP connector and includes jitter generated at the package connection on the printed circuit board, and at the board interconnect as shown in Figure 1.

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
DEVICE PARAMETERS						
t_{PDelay}	Propagation delay	Measured using K28.5 pattern, See Figure 3		280	330	ps
$AutoLP_{ENTRY}$	Auto low power entry time	Electrical idle at input, See Figure 5		11	20	µs
$AutoLP_{EXIT}$	Auto low power exit time	After first signal activity, See Figure 5		30	40	ns
OOB						
t_{OOB1}	OOB mode enter	See Figure 4		3	8	ns
t_{OOB2}	OOB mode exit	See Figure 4		3	8	ns
RECEIVER AC/DC						
$t_{20\text{-}80RX}$	Rise and fall time	Rise times and fall times measured between 20% and 80% of the signal. SATA/SAS 6 Gbps speed measured 1 inch (2.54 cm) from device pin	62		75	ps
t_{skewRX}	Differential skew	Difference between the single-ended mid-point of the RX+ signal rising/falling edge, and the single-ended mid-point of the RX– signal falling/rising edge			30	ps
TRANSMITTER AC/DC						
$t_{20\text{-}80TX}$	Rise and fall time	Rise times and fall times measured between 20% and 80% of the signal. At 6 Gbps SATA or SAS, under no load, measured at the pin	33	50	76	ps
t_{skewTX}	Differential skew	Difference between the single-ended mid-point of the TX+ signal rising/falling edge, and the single-ended mid-point of the TX– signal falling/rising edge, SATA or SAS mode		4	14	ps

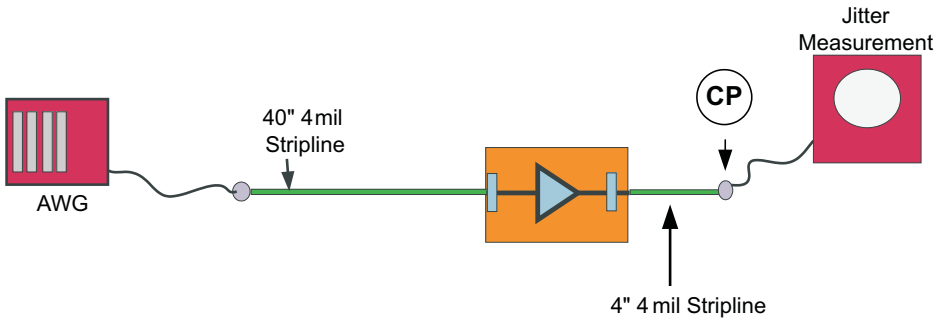


Figure 1. Jitter Measurement Test Condition

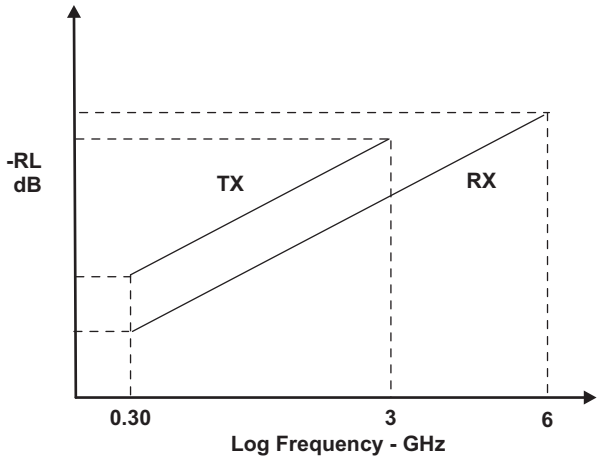


Figure 2. TX, RX Differential Return Loss Limits

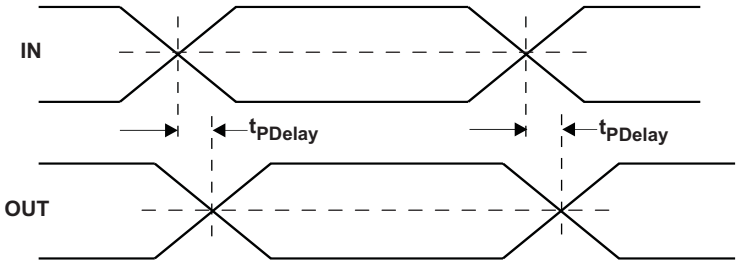


Figure 3. Propagation Delay Timing Diagram

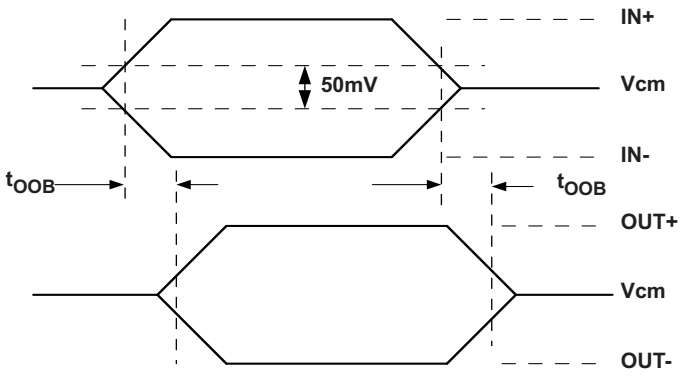


Figure 4. OOB Enter and Exit Timing

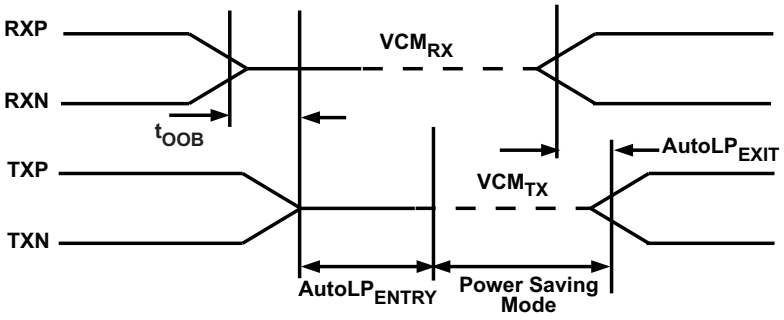


Figure 5. Auto Low-Power Mode Entry and Exit Timing

6.7 Typical Characteristics

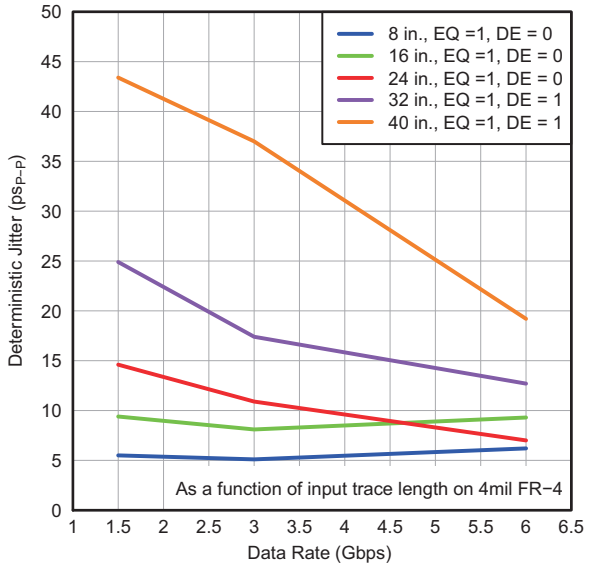


Figure 6. SATA-Mode Deterministic Jitter vs Data Rate

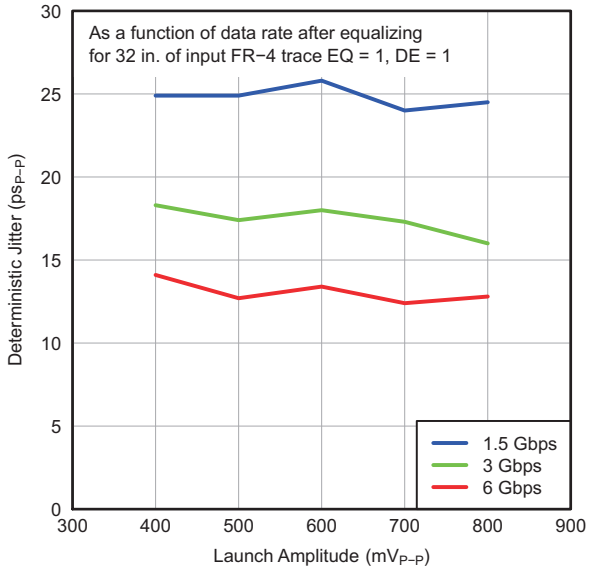


Figure 7. SATA-Mode Deterministic Jitter vs Launch Amplitude

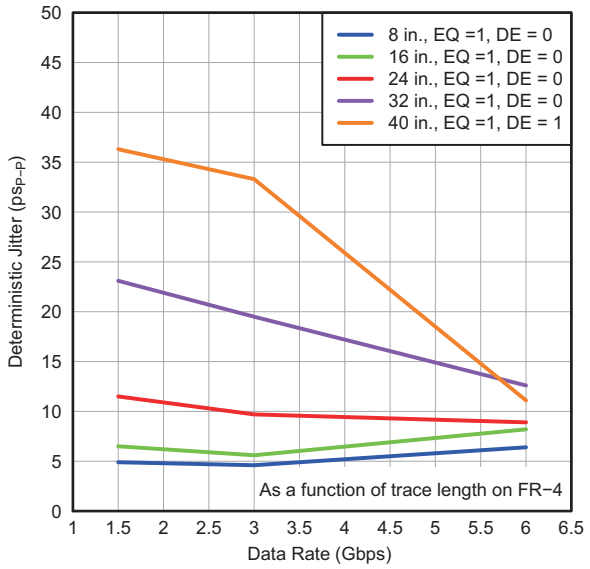


Figure 8. SAS-Mode Deterministic Jitter vs Data Rate

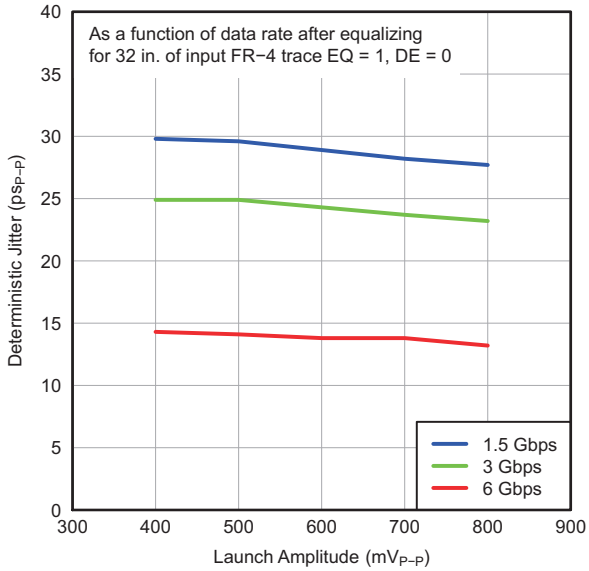
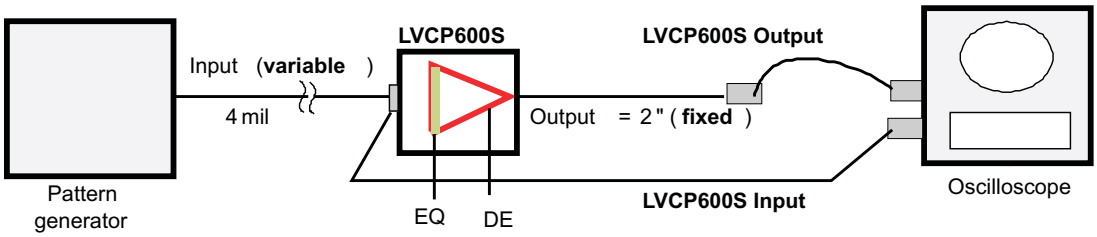


Figure 9. SAS-Mode Deterministic Jitter vs Launch Amplitude

7 Parameter Measurement Information



A. V_{CC} = 3.3 V; INPUT = K28.5 pattern at 1.5 Gbps, 3 Gbps, and 6 Gbps; V_{ID} = 1000 mVpp; TEMP = 25°C; TRACE WIDTH = 4 mil (0.1 mm)

Figure 10. Eye Diagram Measurement Setup for LVCP600S

8 Detailed Description

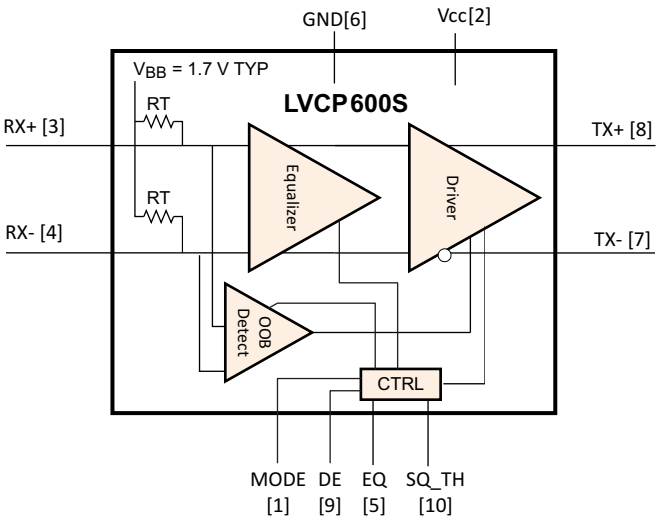
8.1 Overview

The SN75LVCP600S is a single-channel SATA/SAS signal conditioner supporting data rates up to 6 Gbps with an extended temperature range from –40°C to 85°C. The device complies with SATA physical spec rev 3.0 and SAS electrical spec 2.0. The SN75LVCP600S operates from a single 3.3-V supply and has 100-Ω line termination with a self-biasing feature, making the device suitable for AC coupling. The inputs incorporate an out-of-band (OOB) detector, which automatically squelches the output while maintaining a stable common-mode voltage compliant to the SATA/SAS link.

The SN75LVCP600S handles interconnect losses at its input with selectable equalization settings that can be programmed to the match loss in the channel. For data rates of 3 Gbps and lower, the LVCP600S equalizes signals for a span of up to 50 inches of FR4 board material. For data rates of 6 Gbps, the device compensates >40 inches (1 m) of FR4 material. Rx/Tx equalization level is controlled by the setting of signal control pins EQ and DE.

The device is hot-plug capable, preventing device damage during device hot-insertion such as async signal plug/removal, unpowered plug/removal, powered plug/removal, or surprise plug/removal.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Equalization

The SN75LVCP600S supports programmable equalization in its front stage; the equalization settings are shown in Table 1. The input equalizer is designed to recover a signal even when no eye is present at the receiver and effectively supports FR4 trace at the input anywhere from 4 inches (0.1 m) to 40 (1 m) at SATA 6-Gbps speed. In SAS mode, the device meets compliance point IR in a TX/RX connection.

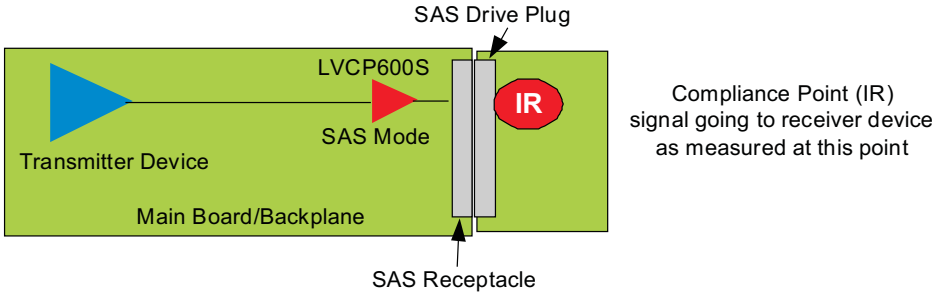


Figure 11. Compliance Point In SAS Mode

8.3.2 Auto Low-Power (ALP) Mode (see Figure 5)

As a redriver, the SN75LVCP600S does not participate in SATA or SAS link power management (PM) states. However, the redriver tracks link-power management mode (partial and slumber) by relying on the link differential voltage, V_{IDp-p}. The SATA/SAS link is continuously sending and receiving data even in long periods of disk inactivity by sending SYNC primitives (logical idle), except when the link enters partial or slumber mode. In these modes, the link is in an electrical-idle state (EID). The device input squelch detector tracks EID status. When the input signal is in the electrical idle state, that is, V_{IDp-p} <VOOB_SATA/VOOB_SAS and stays in this state for > 10 µS, the device automatically enters the low power state. In this state, the output is driven to V_{CM} and the device selectively shuts off internal circuitry to lower power consumption by approximately 90% of its normal operating power. While in ALP mode, the device continues to monitor input signal levels actively; when the input signal exceeds the SATA/SAS OOB upper threshold level, the device reverts to the active state. Exit time from auto low-power mode is <50 ns (maximum).

8.3.3 Out-Of-Band (OOB) Support

The squelch detector circuit within the device enables full detection of OOB signaling as specified in the SATA and SAS specifications. Selection of squelch threshold level is made automatically based on the state of MODE pin, SATA or SAS. Squelch circuit ON/OFF time is 8 ns maximum. While in squelch mode, outputs are held to V_{CM}.

8.4 Device Functional Modes

Table 1. EQ and DE Settings

LEVEL	CONTROL PINS			
	EQ (TYP) dB at 6 Gbps	DE (TYP) dB at 6 Gbps	SQ_TH (SEE V_{OOB} SPEC)	MODE
0 (***default***)	7	0	Full level (normal)	SATA
1	14	–1.3	Reduced level (long channel)	SAS

Trace lengths are suggested values based on TI spice simulations (done over programmable limits of input EQ) to meet SATA/SAS loss and jitter spec.

Actual trace length supported by the LVCP600S may be more or less than suggested values and depends on board layout, trace widths, and number of connectors used in the high-speed signal path. See the *Application Curves* for more placement guidance

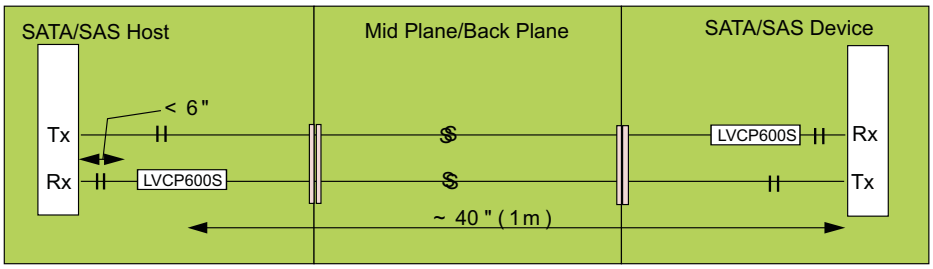


Figure 12. Trace Length Example

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN75LVCP600S is a single-channel SATA/SAS redriver and signal conditioner supporting data rates up to 6 Gbps. The inputs incorporate an OOB (out-of-band) detector, which automatically squelches the output while maintaining a stable common-mode voltage compliant to the SATA/SAS link. This device is designed for applications where an extended temperature range is required.

9.2 Typical Application

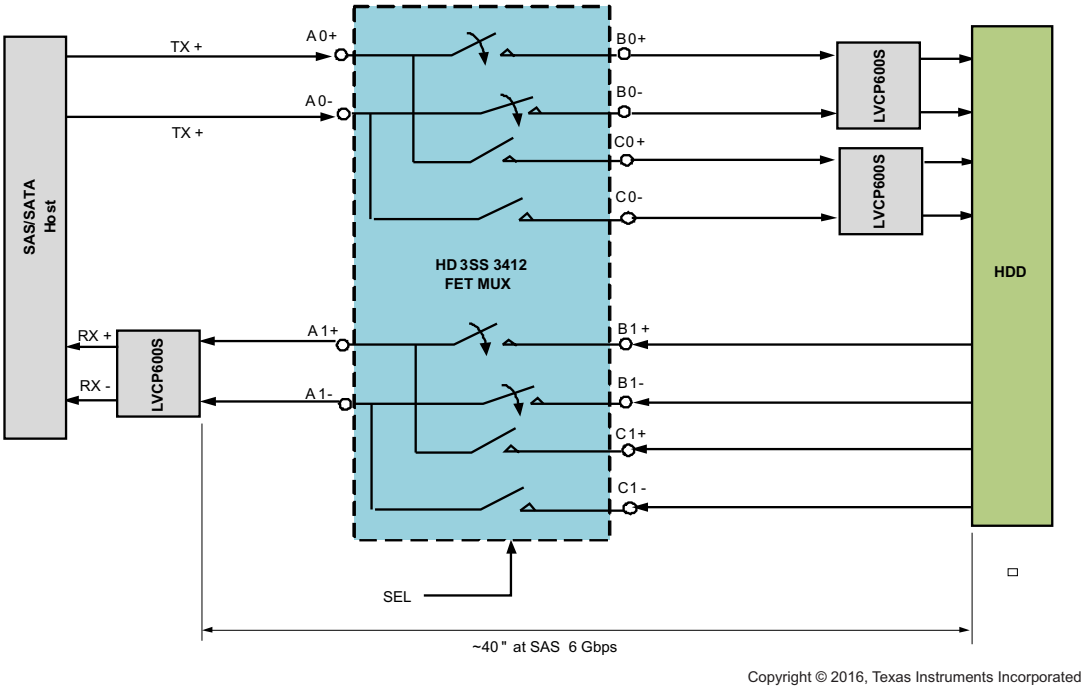


Figure 13. Typical Application

9.2.1 Design Requirements

For this design example, use the values shown in Table 2.

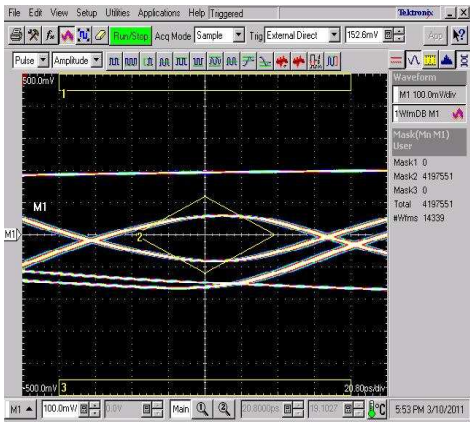
Table 2. Design Parameters

PARAMETER	VALUE
V_{CC}	3.3 V
I_{CC}	32 mA
Input voltage	275 mVpp to 1.6 Vpp
Output voltage	385 mVpp to 1.3 Vpp

9.2.2 Detailed Design Procedure

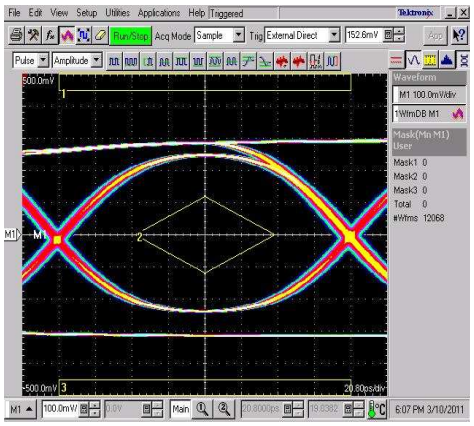
- Determine the loss profile between Host and HDD.
- Based upon loss profile and signal swing, determine the optimal equalization setting EQ pin.
- Select appropriate de-emphasis with DE control pin.
- Depending on loss profile, select squelch threshold using SQ_TH.
- For low level, use 47-kΩ pulldown. For high level, tie pin to V_{CC}.

9.2.3 Application Curves



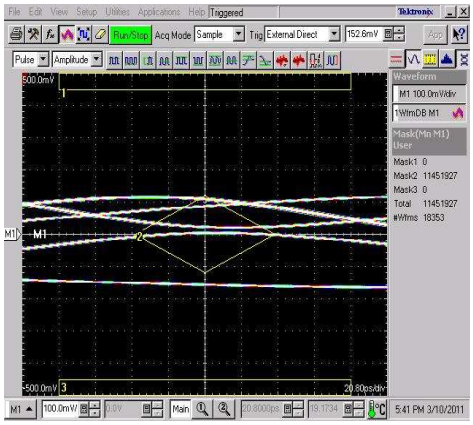
MODE = 0

Figure 14. SATA 6-Gbps Signal After 16 inches (41 cm), Input of LVCP600S



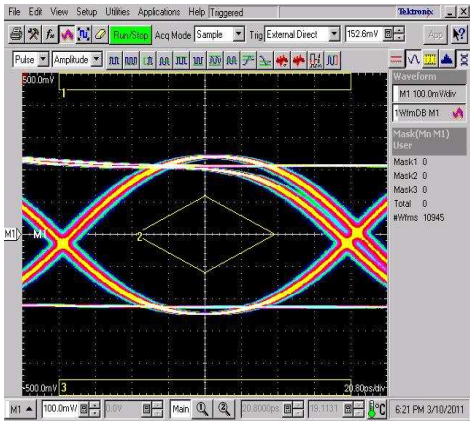
MODE = 0

Figure 15. SATA 6-Gbps, DE = 0, EQ = 1, at Output = 2 Inches (5.1 cm) After Equalizing



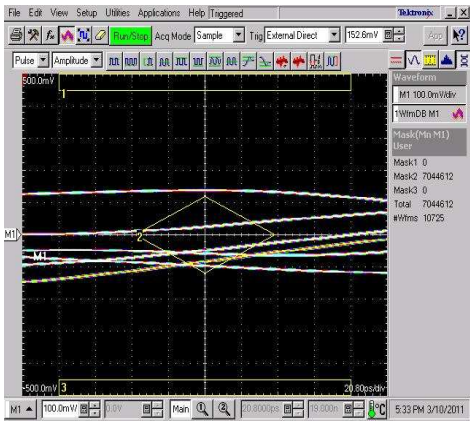
MODE = 0

Figure 16. SATA 6-Gbps Signal After 32 Inches (81 cm) at Input of LVCP600S



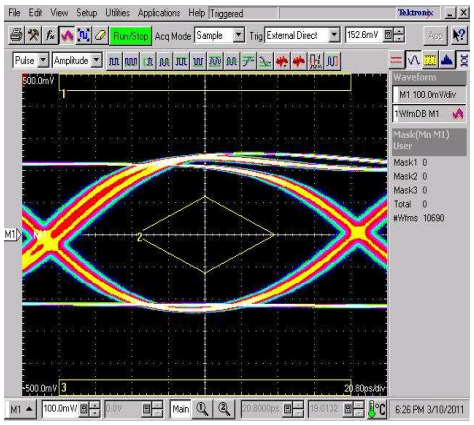
MODE = 0

Figure 17. SATA 6 Gbps, DE = 0, EQ = 1, at Output = 2 Inches (5.1 cm) After Equalizing



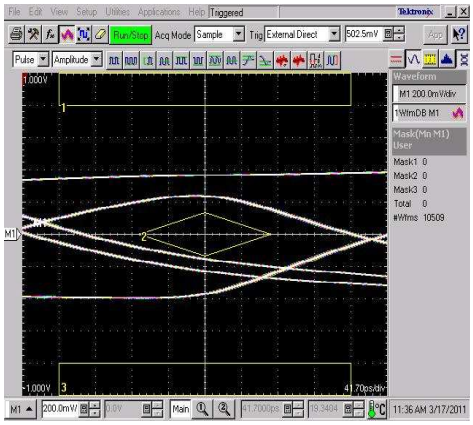
MODE = 0

Figure 18. SATA 6-Gbps Signal After 40 Inches (1 m) at Input of LVCP600S



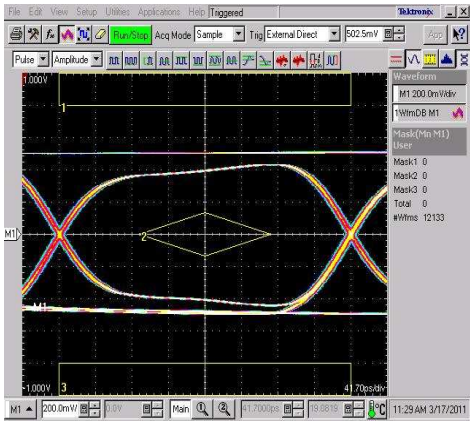
MODE = 0

Figure 19. SATA 6 Gbps, DE = 1, EQ = 1, at Output = 2 Inches (5.1 cm) After Equalizing



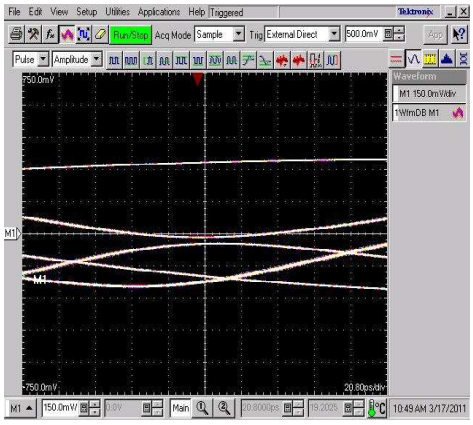
MODE = 1

Figure 20. SAS 3-Gbps Signal After 32 Inches (81 cm) at Input of LVCP600S



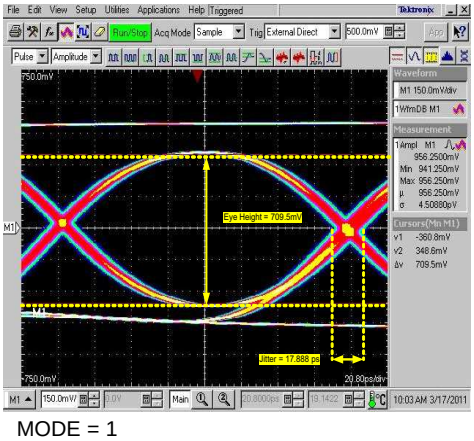
MODE = 1

Figure 21. SAS 3 Gbps, DE = 0, EQ = 1, at Output = 2 Inches (5.1 cm) After Equalizing



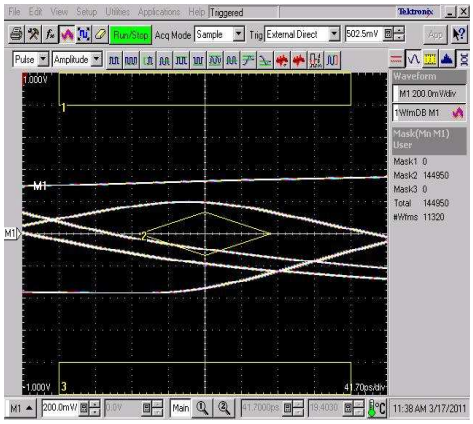
MODE = 1

Figure 22. SAS 6-Gbps Signal after 32 Inches (81 cm) at Input of LVCP600S



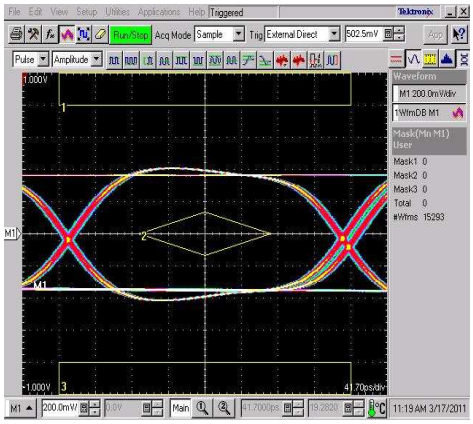
MODE = 1

Figure 23. SAS 6 Gbps, DE = 0, EQ = 1, at Output = 2 Inches) After Equalizing



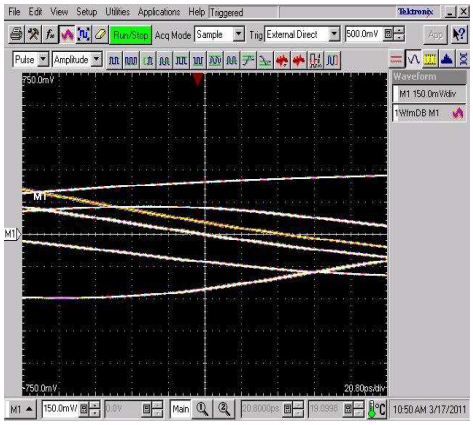
MODE = 1

Figure 24. SAS 3-Gbps Signal After 40 Inches (1 m) at Input of LVCP600S



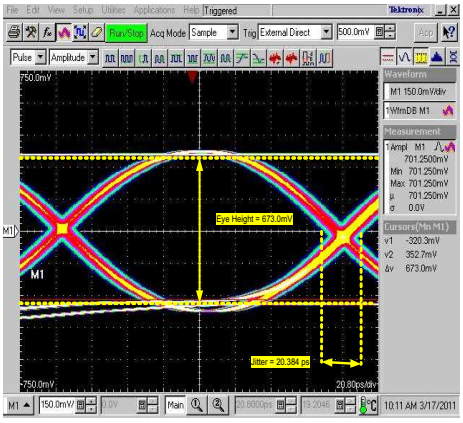
MODE = 1

Figure 25. SAS 3 Gbps, DE = 1, EQ = 1, at Output = 2 Inches (5.1 cm) After Equalizing



MODE = 1

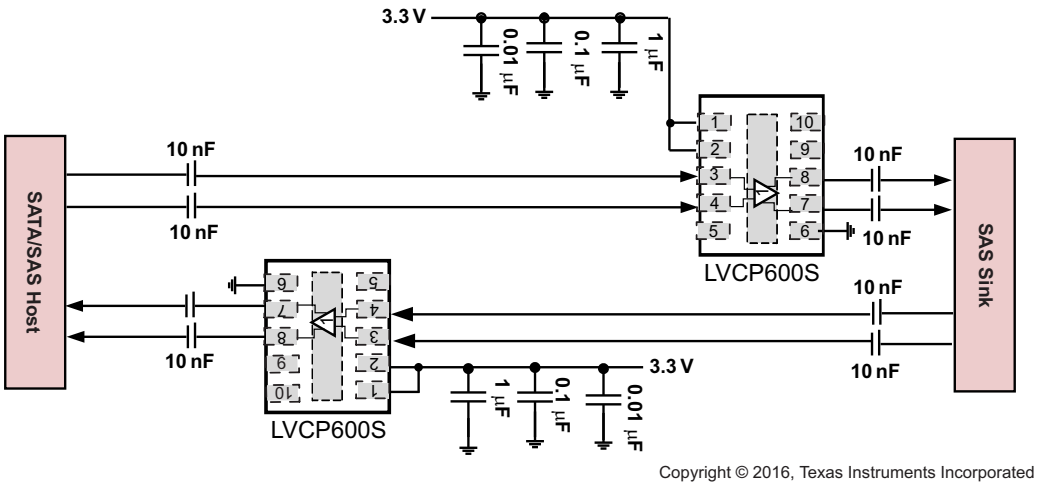
Figure 26. SAS 6-Gbps Signal After 40 Inches (1 m) at Input of LVCP600S



MODE = 1

Figure 27. SAS 6 Gbps, DE = 1, EQ = 1, at Output = 2 Inches (5.1 cm) after Equalizing

9.3 System Examples



A. Place supply capacitors close to device pin

B. EQ selection is set at 7 db, device is set in SAS mode, DE and SQ_TH at default settings

C. Actual EQ settings depend on device placement relative to host and SATA/SAS device.

Figure 28. Typical Device Implementation

10 Power Supply Recommendations

The SN75LVCP600S is designed to operate from a single 3.3-V supply. Always practice the proper power supply sequencing procedure. Apply V_{CC} *first* before any input signals are applied to the device. The power-down sequence is in reverse order.

To minimize the power supply noise floor, provide good decoupling near the SN75LVCP600S power pin. TI recommends placing one 0.01-µF on the power pin. The distance between the SN75LVCP600S and capacitors must be minimized to reduce loop inductance and provide optimal noise filtering. Placing the capacitor underneath the SN75LVCP600S on the bottom of the PCB is often a good choice.

11 Layout

11.1 Layout Guidelines

TI recommends to use at a minimum a four-layer stack-up to accomplish a low-EMI PCB design.

- It is important to match the electrical length of these high-speed traces to minimize both inter-pair and intra-pair skew.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

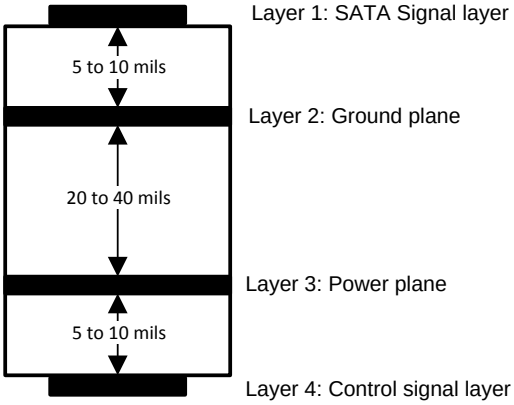


Figure 29. PCB Stack

11.2 Layout Example

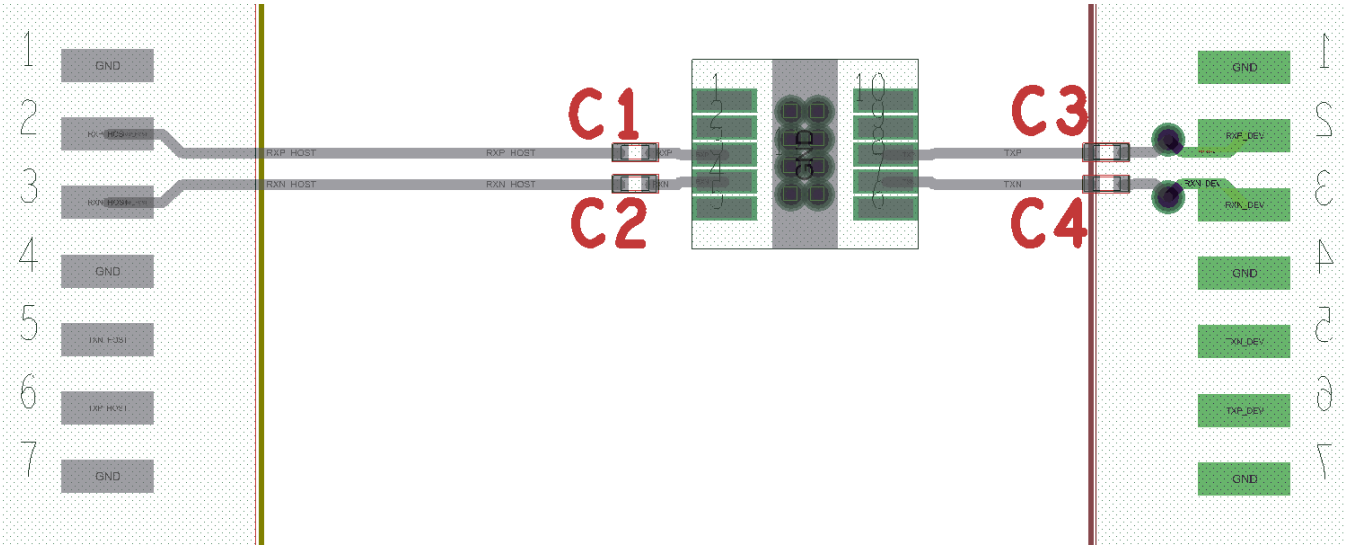


Figure 30. Example Layout

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVCP600SDSKR	ACTIVE	SON	DSK	10	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	600S	Samples
SN75LVCP600SDSKT	ACTIVE	SON	DSK	10	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	600S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

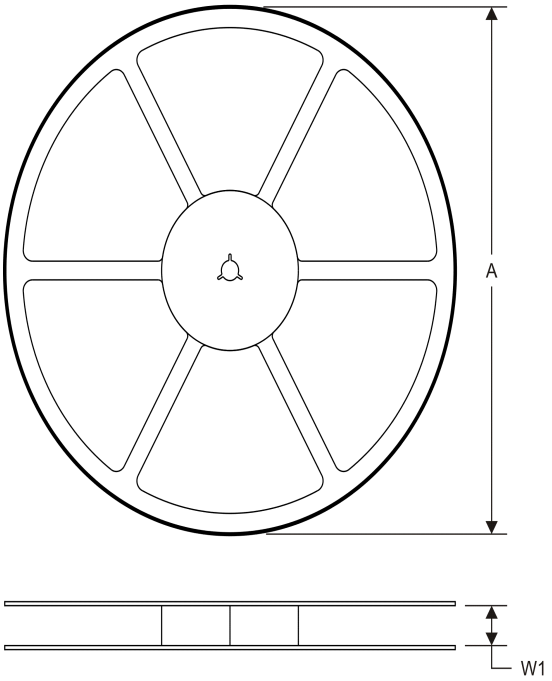
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

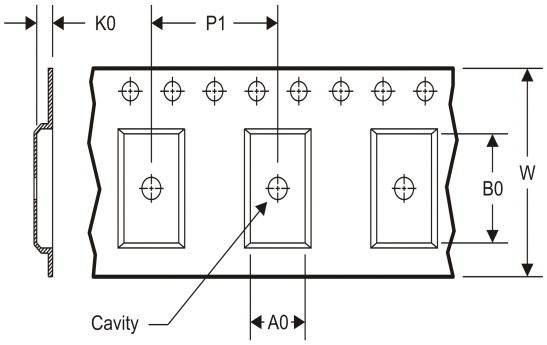
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



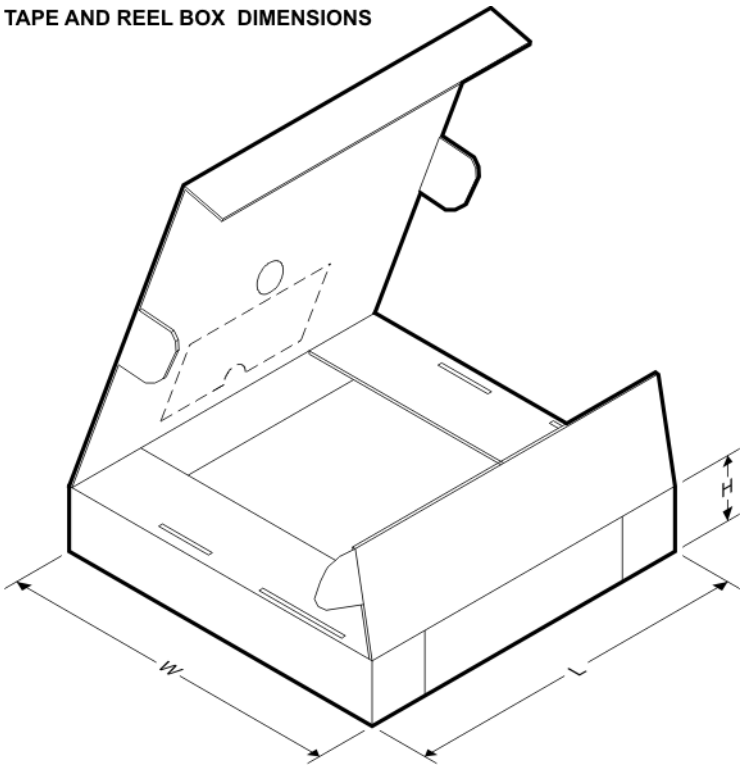
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVCP600SDSKR	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
SN75LVCP600SDSKT	SON	DSK	10	250	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



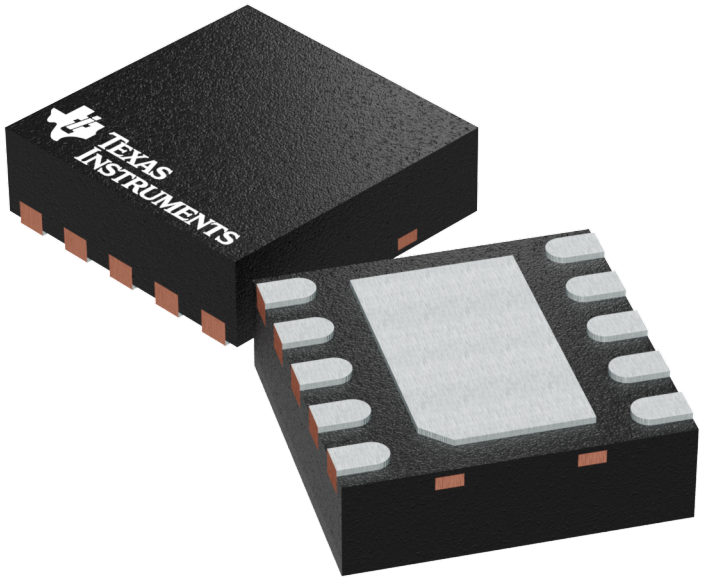
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVCP600SDSKR	SON	DSK	10	3000	210.0	185.0	35.0
SN75LVCP600SDSKT	SON	DSK	10	250	210.0	185.0	35.0

DSK 10 WSON - 0.8 mm max height

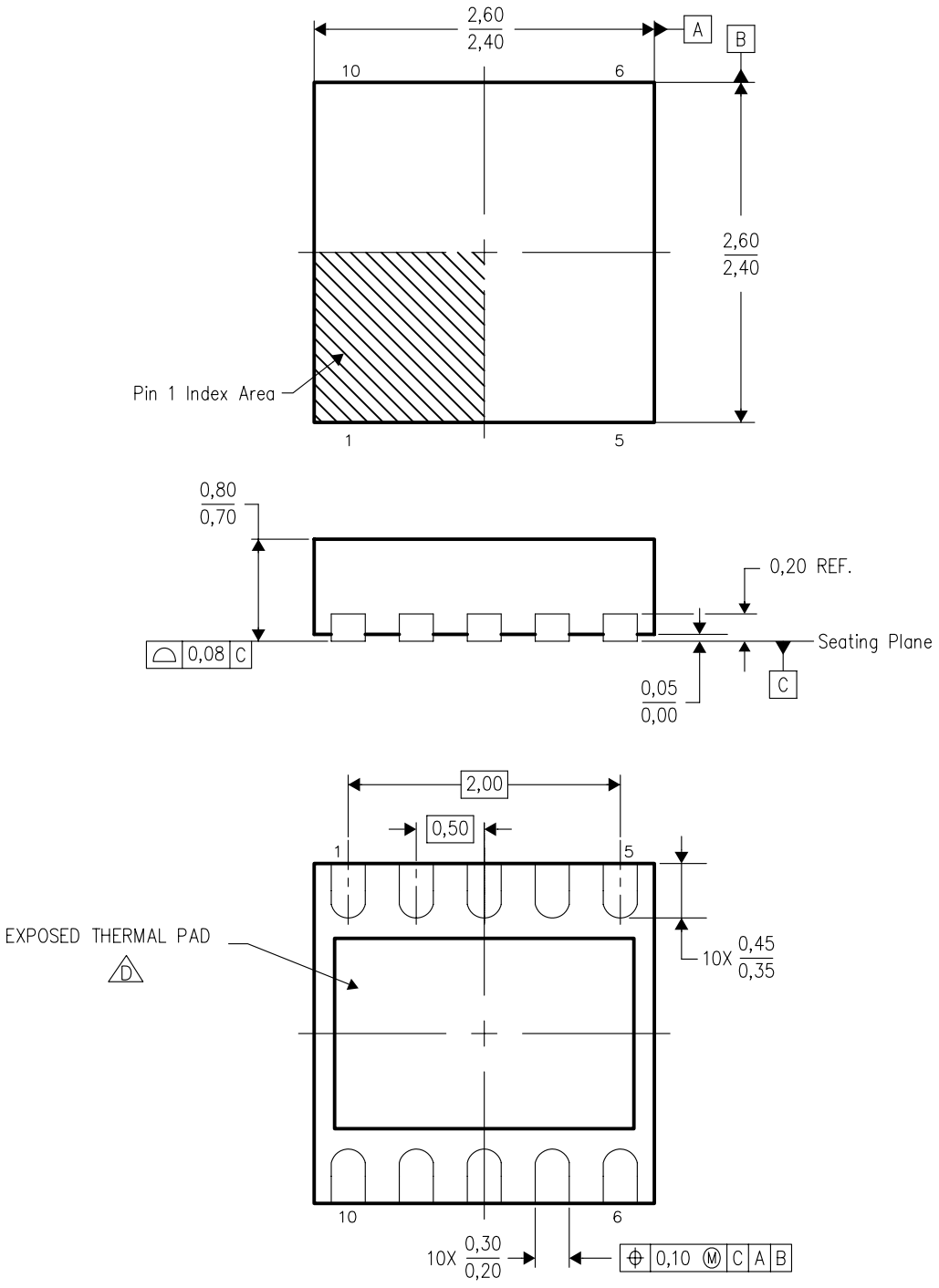
2.5 x 2.5 mm, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DSK (S–PDSO–N10) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

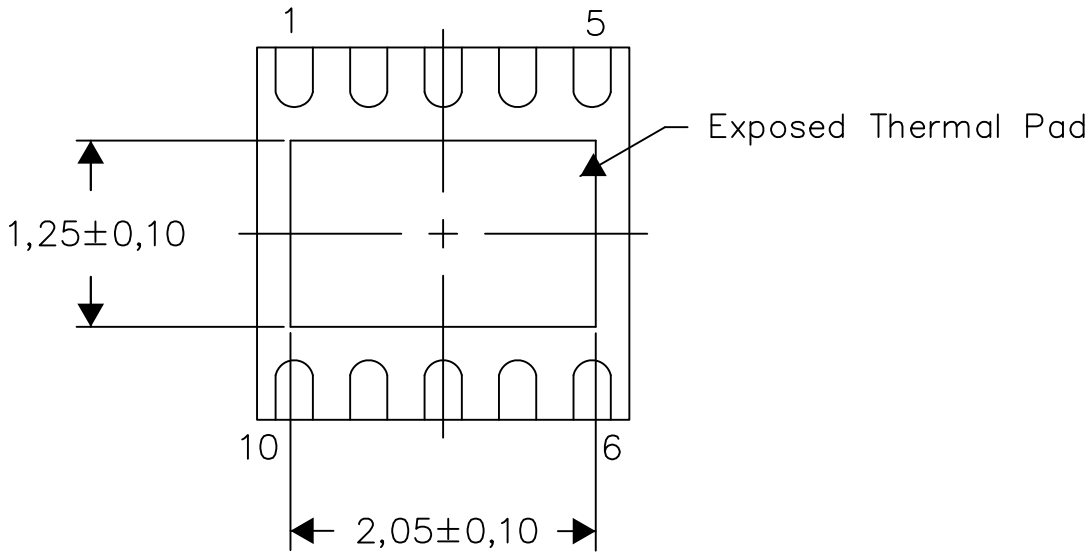
DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



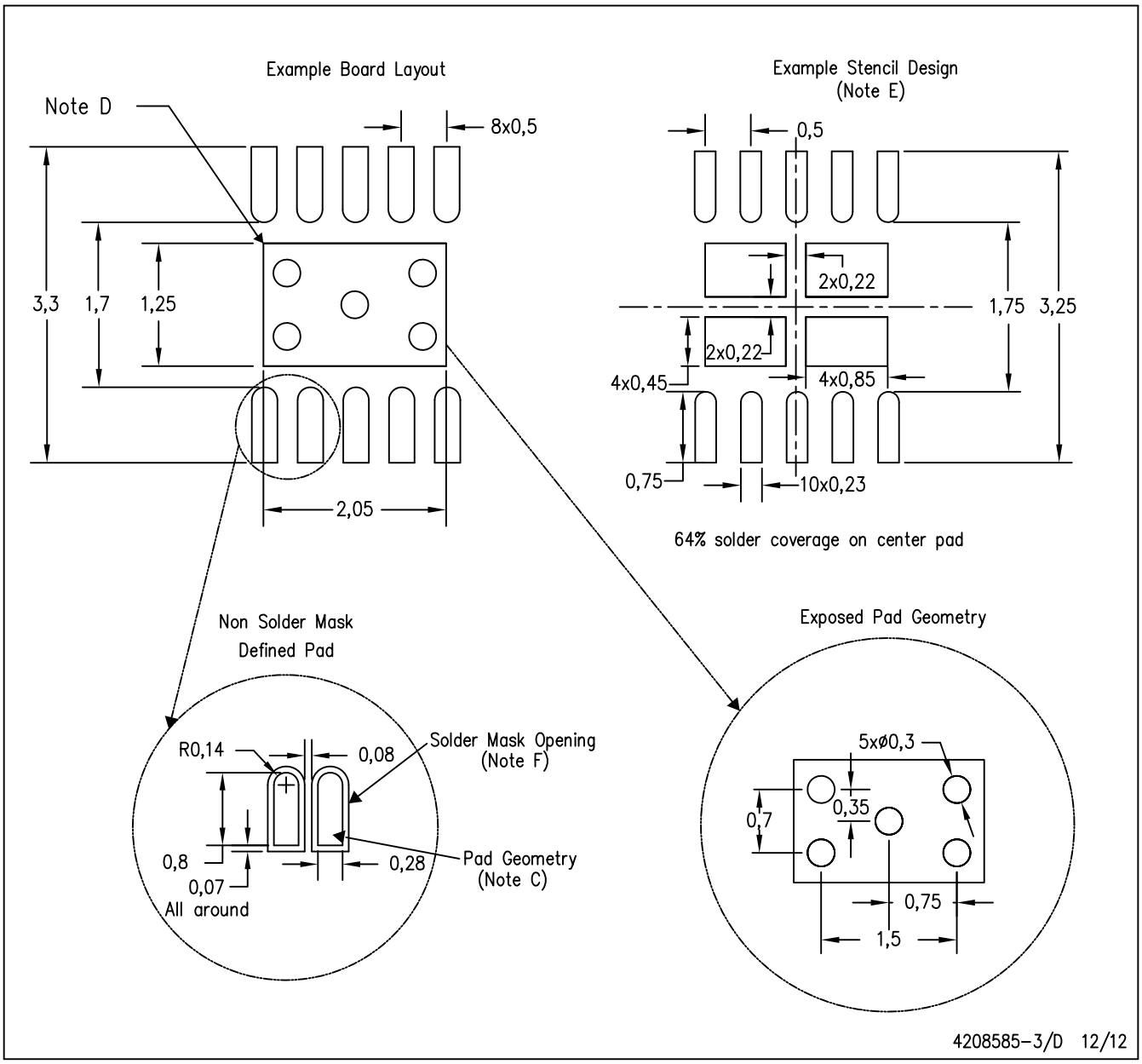
Bottom View

Exposed Thermal Pad Dimensions

4208579–3/E 12/12

NOTE: All linear dimensions are in millimeters

DSK (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265