Octal Channel 12-Bit, 80 MSPS and Low-Power ADC

Check for Samples: ADS5292

FEATURES

- **Maximum Sample Rate: 80 MSPS/12-Bit**
- **High Signal-to-Noise Ratio**
  - **70-dBFS SNR at 5 MHz/80 MSPS**
  - **71.5-dBFS SNR at 5 MHz/80 MSPS and Decimation Filter = 2**
  - **85-dBc SFDR at 5 MHz/80 MSPS**
- **Low Power Consumption**
  - **48 mW/CH at 50 MSPS**
  - **54 mW/CH at 65 MSPS**
  - **66 mW/CH at 80 MSPS (2 LVDS Wire Per Channel)**
- **Digital Processing Block**
  - **Programmable FIR Decimation Filter and Oversampling to Minimize Harmonic Interference**
  - **Programmable IIR High Pass Filter to Minimize DC Offset**
  - **Programmable Digital Gain: 0 dB to 12 dB**
  - **2- or 4- Channel Averaging**
- **Flexible Serialized LVDS Outputs:**
  - **One or Two wires of LVDS Output Lines per Channel Depending on ADC Sampling Rate**
  - **Programmable Mapping Between ADC Input Channels and LVDS Output Pins- Eases Board Design**
  - **Variety of Test Patterns to Verify Data Capture by FPGA/Receiver**
- **Internal and External References**
- **1.8V Operation for Low Power Consumption**
- **Low-Frequency Noise Suppression**
- **Recovery From 6-dB Overload within 1 Clock Cycle**
- **Package: 12-mm × 12-mm 80-Pin QFP**

APPLICATIONS

- **Ultrasound Imaging**
- **Communication Applications**
- **Multi-channel Data Acquisition**

DESCRIPTION

Using CMOS process technology and innovative circuit techniques, the ADS5292 is a low power 80MSPS 8-Channel ADC. Low power consumption, high SNR, low SFDR, and consistent overload recovery allow users to design high performance systems.

The ADS5292 has a digital processing block that integrates several commonly used digital functions for improving system performance. It includes a digital filter module that has built-in decimation filters (with low-pass, high-pass and band-pass characteristics). The decimation rate is also programmable (by 2, by 4, or by 8). This makes it useful for narrow-band applications, where the filters can be used conveniently to improve SNR and knock-off harmonics, while at the same time reducing the output data rate. The device includes an averaging mode where two channels (or even four channels) can be averaged to improve SNR.

Serial LVDS outputs reduce the number of interface lines and enable the highest system integration. The digital data from each channel ADC can be output over one or two wires of LVDS output lines depending on the ADC sampling rate. This 2-wire interface helps keep the serial data rate low, allowing low cost FPGA based receivers to be used even at high sample rate. A unique feature is the programmable mapping module that allows flexible mapping between the input channels and the LVDS output pins. This helps greatly reduce the complexity of LVDS output routing and can potentially result in cheaper system boards by reducing the number of PCB layers.

The device integrates an internal reference trimmed to accurately match across devices. Best performance is expected to be achieved through the internal reference mode. The device can be driven with external references as well.

The device is available in a 12 mm × 12 mm 80-pin QFP. It is specified over a –40°C to 85°C operating temperature range. ADS5292 is completely pin-to-pin and register compatible to ADS5294.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

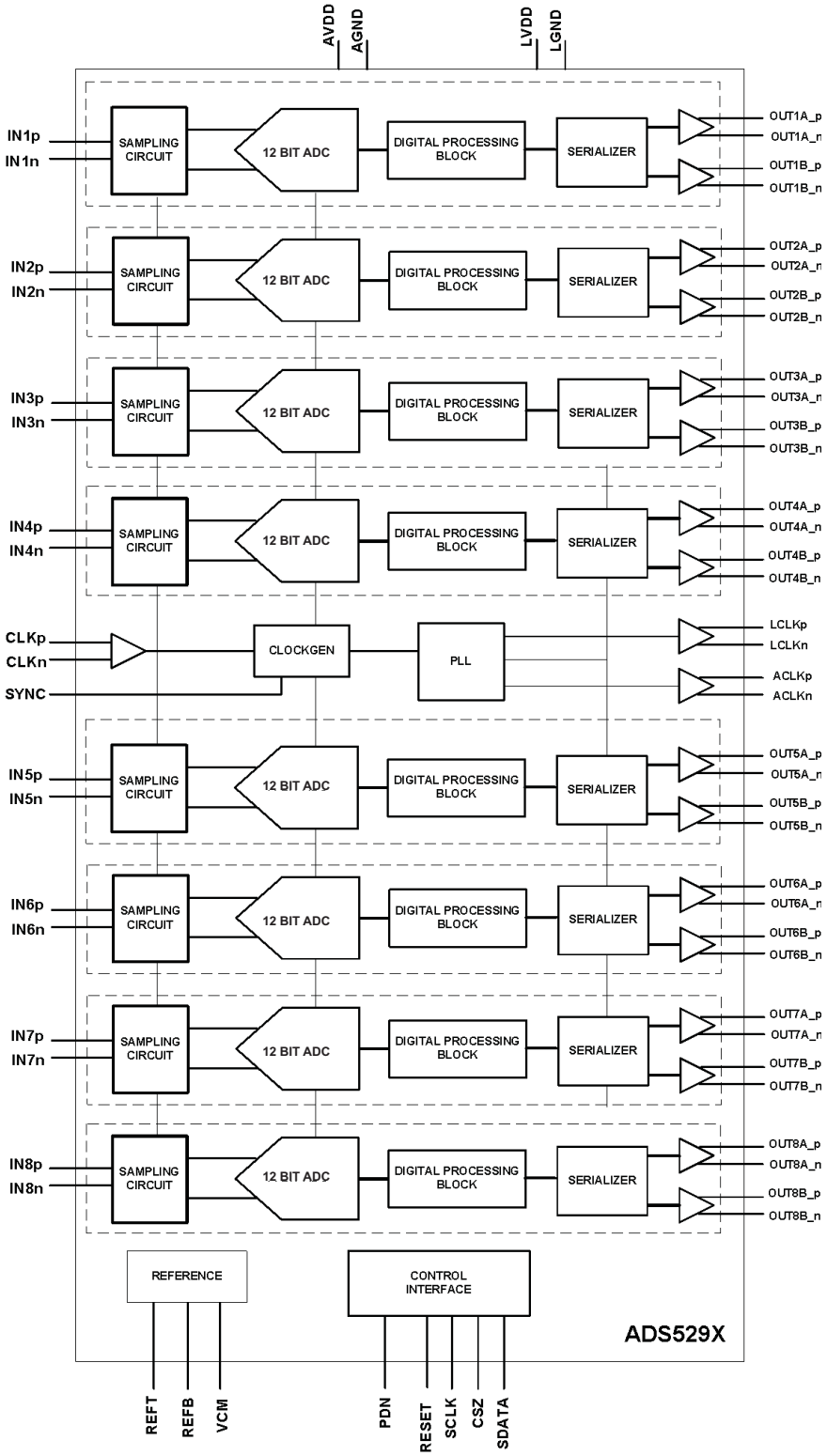
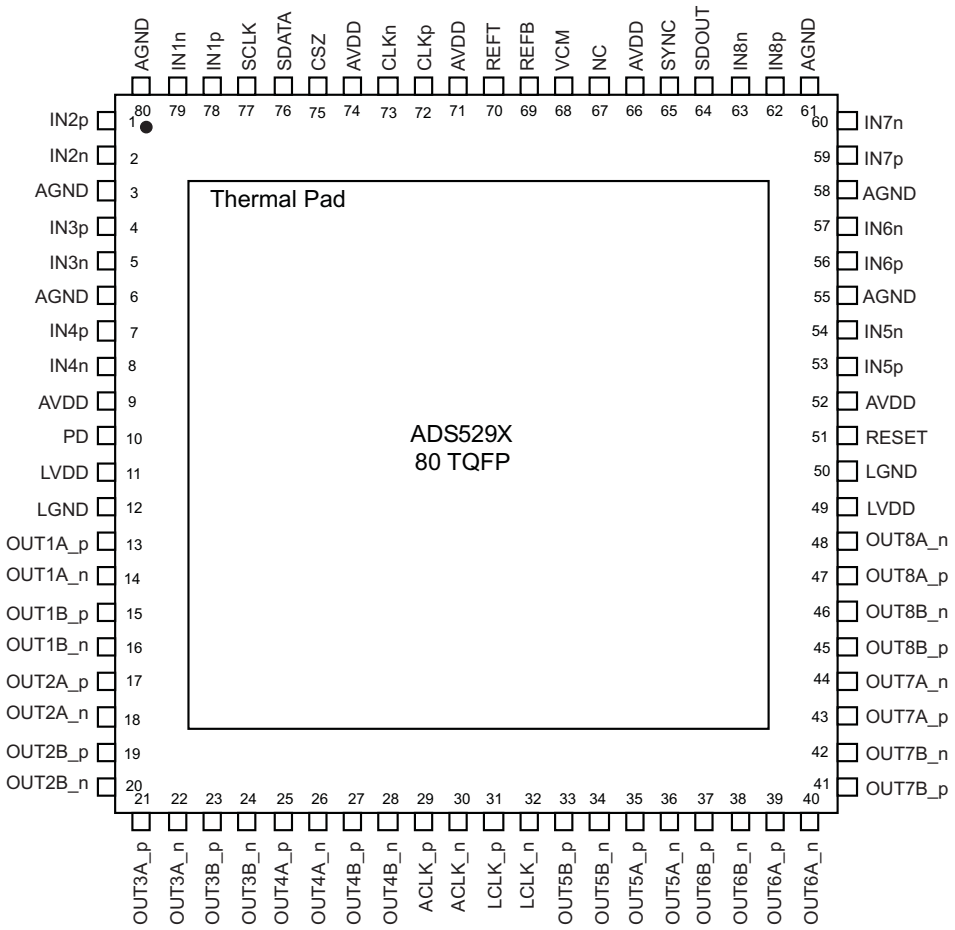


Figure 1. Block Diagram

PIN CONFIGURATION

80-PIN TQFP WITH THERMAL PAD
PFP PACKAGE (TOP VIEW)



PIN FUNCTIONS

NUMBER OF PINS	PIN		DESCRIPTION
	NAME	NUMBER	
5	AVDD	9, 52, 66, 71, 74	Analog power supply, 1.8 V
6	AGND	3, 6, 55, 58, 61, 80	Analog ground
2	LVDD	11, 49	Digital and I/O power supply, 1.8V
2	LGND	12, 50	Digital ground
1	CLKN	73	Negative differential clock –Tie CLKN to GND for single-ended clock
1	CLKP	72	Positive differential clock
2	LCLKP, LCLKN	31, 32	Differential LVDS bit clock (7X)
2	ACLKP, ACLKN	29, 30	Differential LVDS frame clock (1X)
2	IN1P, IN1N	78, 79	Differential input signal, Channel 1
2	IN2P, IN2N	1, 2	Differential input signal, Channel 2
2	IN3P, IN3N	4, 5	Differential input signal, Channel 3
2	IN4P, IN4N	7, 8	Differential input signal, Channel 4
2	IN5P, IN5N	53, 54	Differential input signal, Channel 5
2	IN6P, IN6N	56, 57	Differential input signal, Channel 6
2	IN7P, IN7N	59, 60	Differential input signal, Channel 7
2	IN8P, IN8N	62, 63	Differential input signal, Channel 8
2	OUT1A_P, OUT1A_N	13, 14	Differential LVDS data output, wire 1, channel 1

PIN FUNCTIONS (continued)

NUMBER OF PINS	PIN		DESCRIPTION
	NAME	NUMBER	
2	OUT1B_P, OUT1B_N	15, 16	Differential LVDS data output, wire 2, channel 1
2	OUT2A_P, OUT2A_N	17, 18	Differential LVDS data output, wire 1, channel 2
2	OUT2B_P, OUT2B_N	19, 20	Differential LVDS data output, wire 2, channel 2
2	OUT3A_P, OUT3A_N	21, 22	Differential LVDS data output, wire 1, channel 3
2	OUT3B_P, OUT3B_N	23, 24	Differential LVDS data output, wire 2, channel 3
2	OUT4A_P, OUT4A_N	25, 26	Differential LVDS data output, wire 1, channel 4
2	OUT4B_P, OUT4B_N	27, 28	Differential LVDS data output, wire 2, channel 4
2	OUT5A_P, OUT5A_N	35, 36	Differential LVDS data output, wire 1, channel 5
2	OUT5B_P, OUT5B_N	33, 34	Differential LVDS data output, wire 2, channel 5
2	OUT6A_P, OUT6A_N	39, 40	Differential LVDS data output, wire 1, channel 6
2	OUT6B_P, OUT6B_N	37, 38	Differential LVDS data output, wire 2, channel 6
2	OUT7A_P, OUT7A_N	43, 44	Differential LVDS data output, wire 1, channel 7
2	OUT7B_P, OUT7B_N	41, 42	Differential LVDS data output, wire 2, channel 7
2	OUT8A_P, OUT8A_N	47, 48	Differential LVDS data output, wire 1, channel 8
2	OUT8B_P, OUT8B_N	45, 46	Differential LVDS data output, wire 2, channel 8
1	PD	10	Power down control input. Active High. The pin has an internal 220-kΩ pulldown resistor.
1	REFB	69	Negative reference input/ output
1	REFT	70	Positive reference input/ output
1	VCM	68	Common-mode output pin, 0.95 V output. This pin can be configured as the external reference voltage (1.5 V) input pin as well. See Reg 0x42.
1	RESET	51	Active HIGH RESET input. The pin has an internal 220-kΩ pulldown resistor.
1	SCLK	77	Serial clock input. The pin has an internal 220-kΩ pulldown resistor.
1	SDATA	76	Serial data input. The pin has an internal 220-kΩ pulldown resistor.
1	SDOUT	64	Serial data readout. This pin is in the high-impedance state after reset. When the <READOUT> bit is set, the SDOUT pin becomes active. This is a CMOS digital output running from the AVDD supply.
1	CSZ	75	Serial enable chip select – active low digital input
1	SYNC	65	Input signal to synchronize channels and chips when used with reduced output data rates. If it is not used, add a ≤ 10 KΩ pull-down resistor.
1	NC	67	No Connection. Must leave floated

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage	AVDD	–0.3	2.2	V
	LVDD	–0.3	2.2	V
Voltage	between AGND and LGND	–0.3	0.3	V
	at analog inputs	–0.3	min[2.2, AVDD+0.3]	V
	at digital inputs, CLKN, CLKP(2), RESET, SCLK, SDATA, CSZ	–0.3	min[2.2, AVDD+0.3]	V
	at digital outputs	–0.3	min[2.2,LVDD+0.3]	V
Maximum junction temperature (T_J), any condition			105	°C
Storage temperature range		–55	150	°C
Operating temperature range		-40	85	°C
ESD Ratings	Human Body Model (HBM)		2000	V
	Charged Device Model (CDM)		500	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKN is < |0.3V|. This prevents the ESD protection diodes at the clock input pins from turning on.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS5292	UNITS
		PFP (80 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	30.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	6.3	
θ_{JB}	Junction-to-board thermal resistance	8.3	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	8.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.7	1.8	1.9	V
LVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS / OUTPUTS						
	Differential input voltage range			2		V_{PP}
	Input common-mode voltage			0.95±0.05		V
REF_T	External reference mode			1.45		V
REF_B	External reference mode			0.45		V
VCM	External Reference mode Input			1.5		V
	Common-mode voltage output			0.95		V
	Maximum Input Frequency (1)	2 V_{PP} amplitude		80		MHz
CLOCK INPUTS						
	ADC Clock input sample rate		10		80	MSPS
	Input Clock amplitude differential ($V_{(CLKP)}$ - $V_{(CLKN)}$) peak-to-peak	Sine wave, AC-coupled	0.2	1.5		V_{PP}
		LVPECL, AC-coupled	0.2	1.6		
		LVDS, AC-coupled	0.2	0.7		
V_{IL}	Input Clock CMOS single-ended ($V_{(CLKP)}$)			<0.3		V
V_{IH}				>1.5		V
	Input clock duty cycle		35%	50%	65%	
DIGITAL OUTPUTS						
	ACLKP and ACLKN outputs (LVDS), 1-wire interface			1x (sample rate)		MSPS
	LCLKP and LCLKN outputs (LVDS), 1-wire interface			6x (sample rate)		MSPS
	ACLKP and ACLKN outputs (LVDS), 2-wire interface			0.5x (sample rate)		MSPS
	LCLKP and LCLKN outputs (LVDS), 2-wire interface			3x (sample rate)		MSPS
	Maximum data rate, 2-wire interface			480		MSPS
	Maximum data rate, 1-wire interface			960		MSPS
C_{LOAD}	Maximum external capacitance from each output pin to LGND			5		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs			100		Ω
T_A	Operating free-air temperature		-40		85	°C

(1) See the Large and Small Signal Input Bandwidth section.

ELECTRICAL CHARACTERISTICS DYNAMIC PERFORMANCE

Typical values are at 25°C, AVDD = 1.8V, LVDD = 1.8V, 50% clock duty cycle, –1dBFS differential analog input, 12Bit/80 MSPS, ADC is configured in internal reference mode (unless otherwise noted). MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, LVDD = 1.8 V.

PARAMETERS		CONDITIONS		MIN	TYP	MAX	UNITS
AC PERFORMANCE							
SNR	Signal-to-noise ratio	f_{in} = 5 MHz, 80 MSPS. 14 bits mode			72		dBFS
		f_{in} = 5 MHz, 80 MSPS		67.5	70		
		f_{in} = 30 MHz, 80 MSPS			69.8		
		f_{in} = 5 MHz, 80 MSPS, Decimation filter=2			71.5		
SINAD	Signal-to-noise and distortion ratio	f_{in} = 5 MHz, 80 MSPS			69.8		dBFS
		f_{in} = 30 MHz, 80 MSPS			69.3		
ENOB	Effective number of bits	f_{in} = 5 MHz			11.3		LSB
DNL	Differential nonlinearity	f_{in} = 5 MHz		–0.8	±0.05	0.8	LSB
INL	Integral nonlinearity	f_{in} = 5 MHz			0.4	1	LSB
SFDR	Spurious-free dynamic range	f_{in} = 5 MHz		72.5	85		dBc
		f_{in} = 30 MHz			80		
THD	Total harmonic distortion	f_{in} = 5 MHz		71	81.5		dBc
		f_{in} = 30 MHz			78		
HD2	Second-harmonic distortion	f_{in} = 5 MHz		72.5	88		dBc
		f_{in} = 30 MHz			80		
HD3	Third-harmonic distortion	f_{in} = 5 MHz		72.5	85		dBc
		f_{in} = 30 MHz			78.5		
	Worst spur excluding HD2, HD3	f_{in} = 5 MHz			91		dBc
		f_{in} = 30 MHz			83		
		f_{in} = 65 MHz			76		
IMD3	Intermodualtion distortion	f_{in} = 5 MHz at –7 dBFS, f_2 = 10 MHz at –7 dBFS			82		dBc
	Overload recovery	Recovery to within 1% of full scale value for 6-dB overload with sine wave input			1		Clock Cycle
XTALK	Cross-talk	f_{in} = 10 MHz; V_{OUT} = –1 dBFS signal applied on aggressor channel no signal applied on victim channel	far channel		90		dB
			near channel		85		
	Phase noise	5 MHz, 1 kHz off carrier			–138		dBc/Hz
ANALOG INPUT/OUTPUT							
	Differential input voltage range (0-dB gain)				2		Vpp
Rin	Differential Input Resistance	At DC			2		kΩ
Cin	Differential Input Capacitance	At DC			2.2		pF
	Analog input bandwidth	With a 50 Ω source impedance			550		MHz
	Analog input common-mode current (per input pin)				1.6		µA/MSPS
	VCM common-mode output voltage				0.95		V
	VCM output current capability				5		mA
DC ACCURACY							
	Offset error	Across devices and across channels within a device		–20		20	mV
	Temperature coefficient of offset error				<0.01		mV/°C
E_{GREF}	Gain error due to internal reference inaccuracy alone			–2		2	%FS
E_{GCHAN}	Gain error of channel alone				0.5		%FS
	Temperature coefficent of E_{GCHAN}				<0.01		%FS/°C

ELECTRICAL CHARACTERISTICS DYNAMIC PERFORMANCE (continued)

Typical values are at 25°C, AVDD = 1.8V, LVDD = 1.8V, 50% clock duty cycle, –1dBFS differential analog input, 12Bit/80 MSPS, ADC is configured in internal reference mode (unless otherwise noted). MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, LVDD = 1.8 V.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY					
Power consumption	80 MSPS/12-Bit, 2-wire LVDS		66		mW/CH
	50 MSPS/12 Bit, 1-wire LVDS		48		
	40 MSPS/12 Bit, 1-wire LVDS		43		
	80 MSPS/12 Bit, 1-wire decimation filter = 2, 1-wire LVDS		87		
AVDD	80 MSPS, 12 Bit		182	206	mA
	65 MSPS, 12 Bit		162		
	40 MSPS, 12 Bit		130		
LVDD	80 MSPS/12-Bit, 2-wire LVDS		112	125	mA
	50 MSPS/12 Bit,1-wire LVDS		67		
	40 MSPS/12 Bit,1-wire LVDS		61		
	80 MSPS/12 Bit, Decimation filter = 2, 1-wire LVDS		198		
Power-down power consumption	Partial power down, 80MHz, 2-wire LVDS		175		mW
	Complete power down			50	
Power supply modulation ratio	Carrier = 5 MHz, f_N = 10 kHz at 50 mV_{PP} signal on AVDD		30		dBc
Power supply rejection ratio	AC power supply rejection ratio f = 10 kHz		55		dBc

DIGITAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 1.8V, LVDD = 1.8V

PARAMETERS		CONDITION	MIN	TYP	MAX	UNITS
DIGITAL INPUTS/OUTPUTS						
V_{IH}	Logic high input voltage	All digital inputs support 1.8-V and 3.3-V CMOS logic levels.	1.3			V
V_{IL}	Logic low input voltage				0.4	V
I_{IH}	Logic high input current	V_{HIGH} = 1.8 V		6		µA
I_{IL}	Logic low input current	V_{LOW} = 0 V		<0.1		µA
V_{OH}	Logic high output voltage		AVDD-0.1			V
V_{OL}	Logic low output voltage			0.2		V
LVDS OUTPUTS						
V_{ODH}	High-level output differential voltage	100 Ω external termination	240	350	405	mV
V_{ODL}	Low-level output differential voltage	100 Ω external termination	–240	–350	–405	mV
V_{OCM}	Output common-mode voltage		900	1100	1300	mV

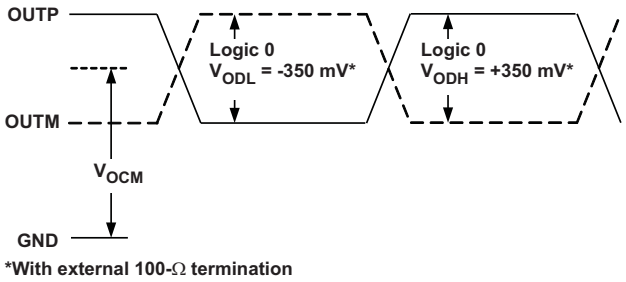


Figure 2. LVDS Output Voltage Levels

TIMING REQUIREMENTS(1)(2)(3)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, sampling frequency = 80 MSPS, 12-bit, sine-wave input clock = 1.5-Vpp clock amplitude, C_{LOAD} = 5 pF, R_{LOAD} = 100 Ω, unless otherwise noted. MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, LVDD = 1.7 V to 1.9 V.

PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
t_a	Aperture delay	The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs		4		ns
	Aperture delay variation	Across channels within the same device		±175		ps
		Across devices at same temperature and LVDD supply voltage		2.5		ns
t_j	Aperture jitter RMS			320		fs rms
t_d	Data latency	1-wire LVDS output interface		11		Clock cycles
		2-wire LVDS output interface		15		Clock cycles
t_{SU}	Data setup time	80 MSPS, 2 wire LVDS, 6x serialization	0.25	0.63		ns
t_H	Data hold time	80 MSPS, 2 wire LVDS, 6x serialization	0.65	1		ns
t_{PROG}	Clock propagation delay	Input clock rising edge(zero cross) to frame clock rising edge(zero cross)		See Table 1 and Table 2		ns
	Variation of t_{PROG}	Between two devices under the same conditions		±0.75		ns
	LVDS bit clock duty cycle			50%		
	Bit clock cycle-to-cycle jitter			40		ps rms
	Frame clock cycle-to-cycle jitter			70		ps rms
t_{RISE}	Data rise time	Rise time is from -100mV to +100mV		0.2		ns
t_{FALL}	Data fall time	Fall time is from +100mV to -100mV		0.2		ns
$t_{CLKRISE}$	Output clock rise time	Rise time is from -100mV to +100mV		0.18		ns
$t_{CLKFALL}$	Output clock fall time	Fall time is from +100mV to -100mV		0.16		ns
t_{WAKE}	Wake-up Time	Time to valid data after coming out of COMPLETE POWER-DOWN mode		100		µs
		Time to valid data after coming out of PARTIAL POWER-DOWN mode (with clock continuing to run during power-down)		5		µs

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(3) Data valid refers to logic HIGH of 100 mV and logic LOW of –100 mV.

Table 1. LVDS Timing at Different Sampling Frequencies - 2 Wire Interface, 5x Serialization(1)

LVDS Output Rate (MSPS)	Setup Time (t_{su}), ns			Hold Time (t_H), ns			t_{PROG} = (11/12) × T + t_{delay}, ns(2)		
Fs(1/T)	Data Valid to Zero-Crossing of LCLKP (both edges)			Zero-Crossing of LCLKP to Data Becoming Invalid (both edges)			t_{PROG} = delay from Input clock zero-cross rising edge to frame clock zero cross rising edge		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	0.25	0.63		0.65	1			8.6	
65	0.42	0.8		1	1.3			8.6	
50	0.85	1.1		1.4	1.7			8.6	
40	1.2	1.5		1.8	2.1			8.6	
30	2.1	2.4		2.3	2.6			8.6	
20	3.5	3.8		3.7	4			8.6	
10	7.7	8		7.8	8.4			8.6	

(1) Bit clock and Frame clock jitter has been included in the Setup and hold timing.
(2) Values below correspond to t_{delay}, NOT t_{PROG}

Table 2. LVDS Timing at Different Sampling Frequencies - 1 Wire Interface, 12x Serialization(1)

LVDS Output Rate (MSPS)	Setup Time (t_{su}), ns			Hold Time (t_H), ns			t_{PROG} = (9/12) × T + t_{delay}, ns (2)		
Fs (1/T)	Data Valid to Zero-Crossing of LCLKP (both edges)			Zero-Crossing of LCLKP to Data Becoming Invalid (both edges)			t_{PROG} = delay from Input clock zero-cross rising edge to frame clock zero cross rising edge)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
65	0.22	0.35		0.21	0.38			9	
50	0.38	0.6		0.45	0.6			9	
40	0.4	0.7		0.7	1			9	
25	1	1.3		1.4	1.7			9	
10	3.6	3.9		3.7	4			9	

(1) Bit clock and Frame clock jitter has been included in the Setup and hold timing.
(2) Values below correspond to t_{delay}, NOT t_{PROG}

LVDS TIMING DIAGRAM

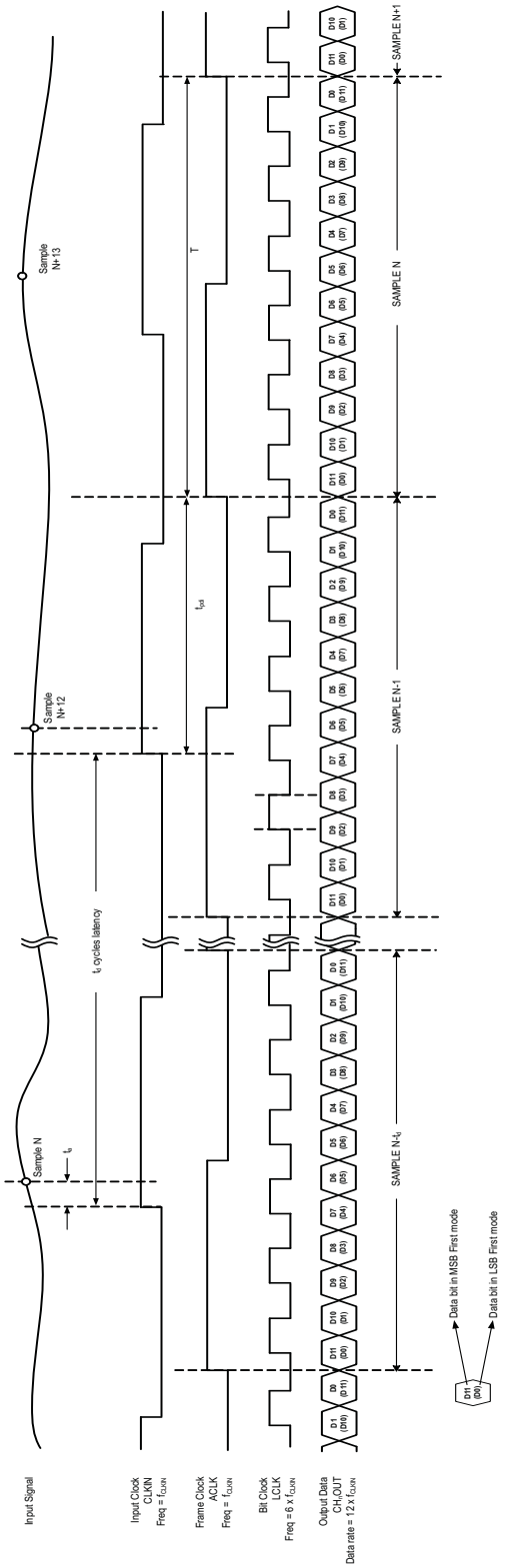


Figure 3. 12-bit 2 wire LVDS Timing Diagram

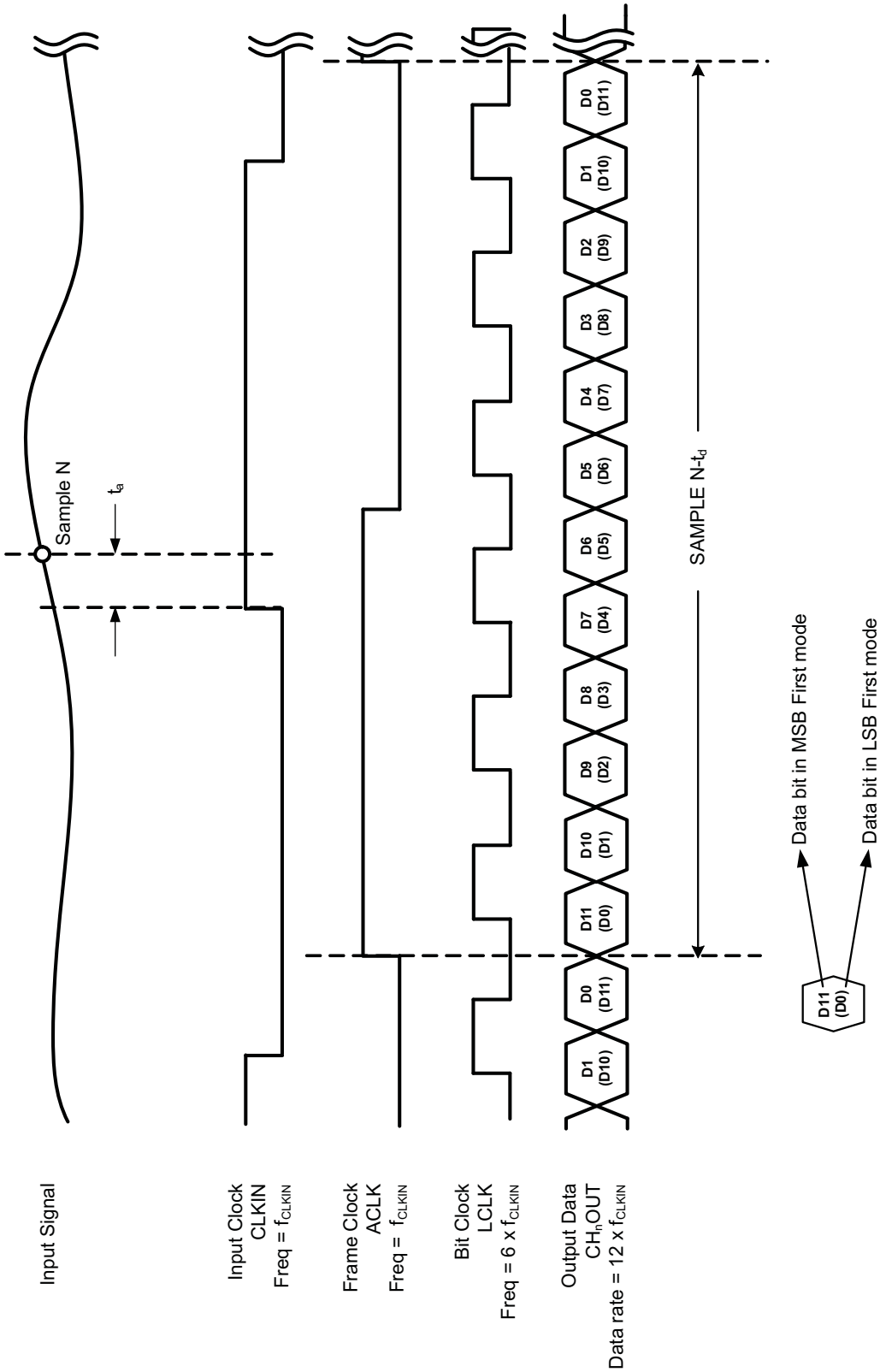


Figure 4. Timing Diagram

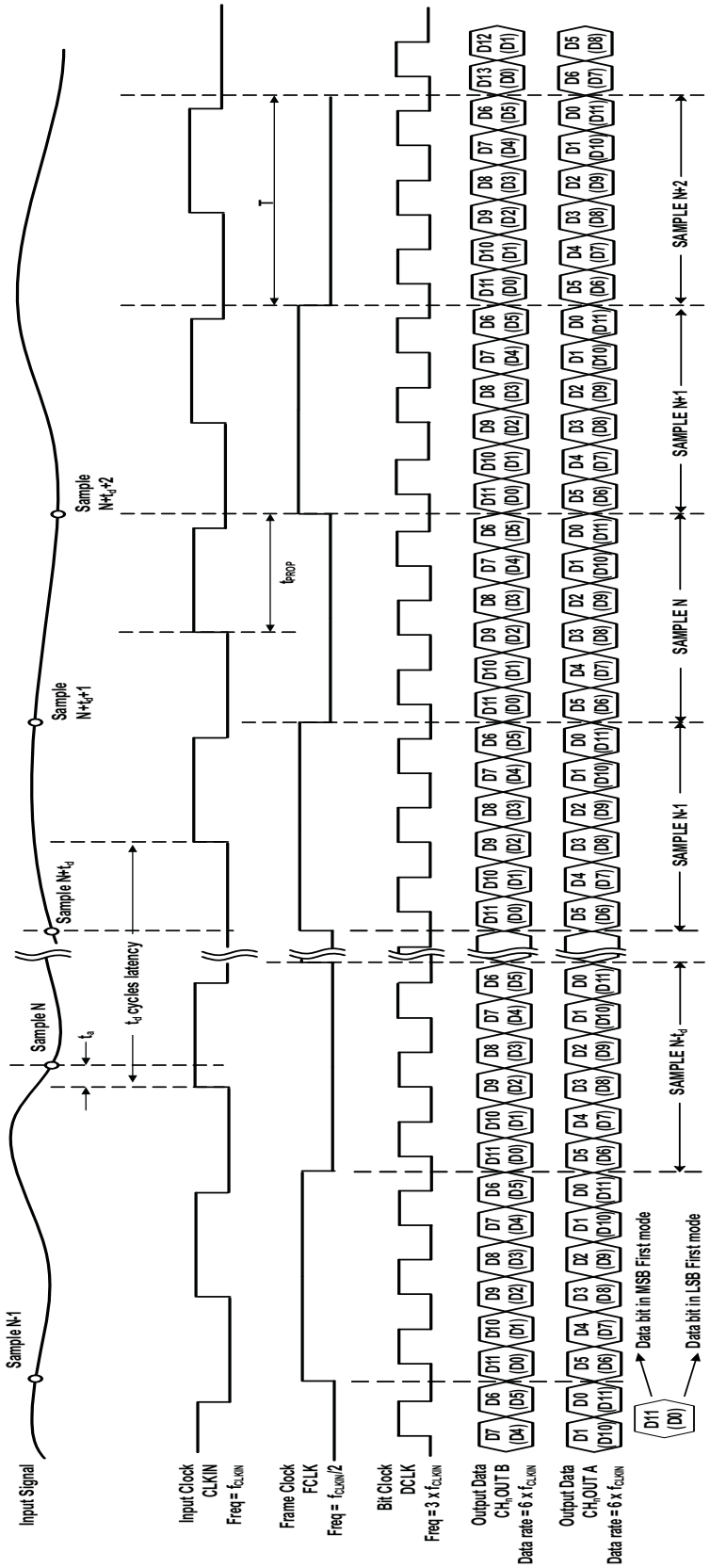


Figure 5.

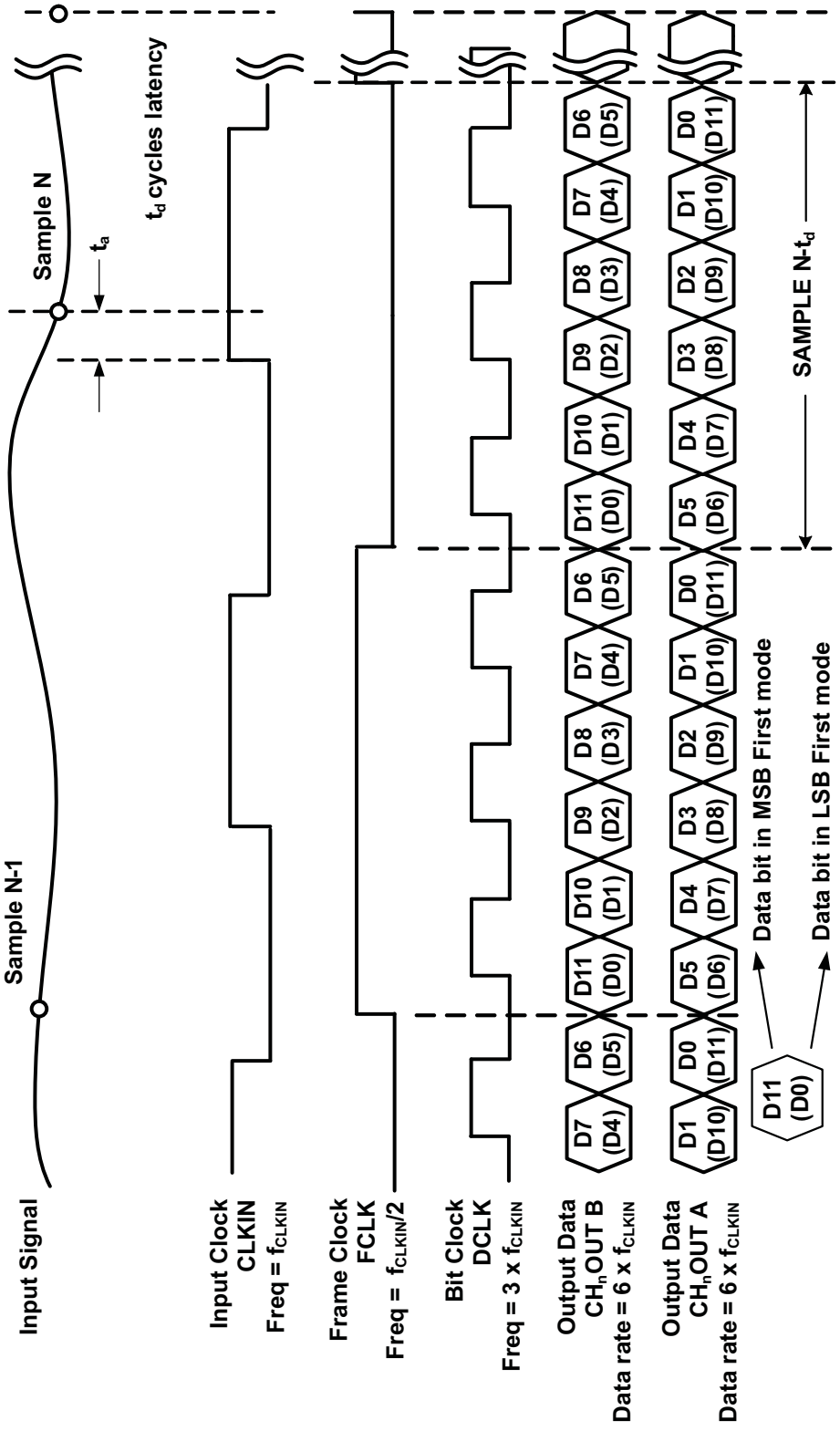


Figure 6. Enlarged 2 Wire LVDS Timing Diagram (12 bit)

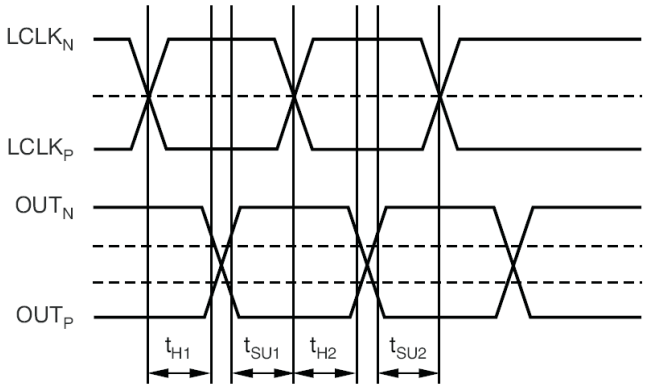


Figure 7. Definition of Setup and Hold Times t_{SU} = min(t_{SU1}, t_{SU2}); t_H = min(t_{H1}, t_{H2})

TYPICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, 12Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

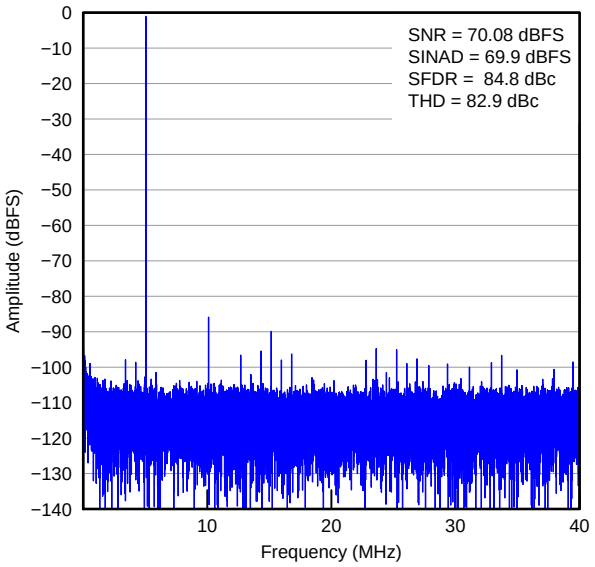


Figure 8. FFT for 5 MHz Input Signal, Sample Rate = 80 MSPS

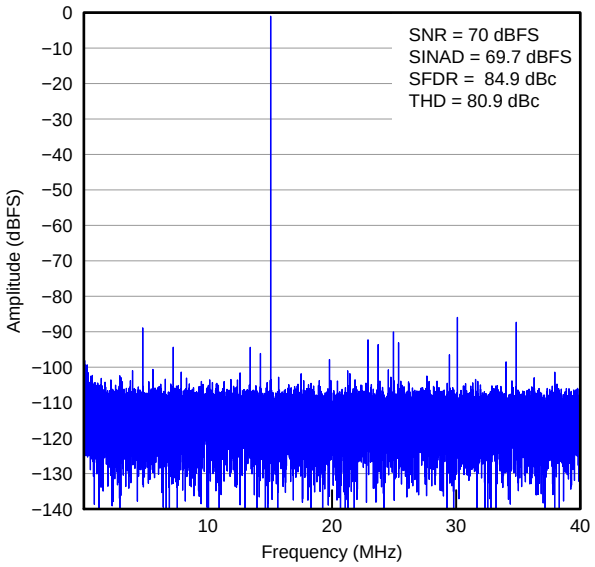


Figure 9. FFT for 15 MHz Input Signal, Sample Rate = 80 MSPS

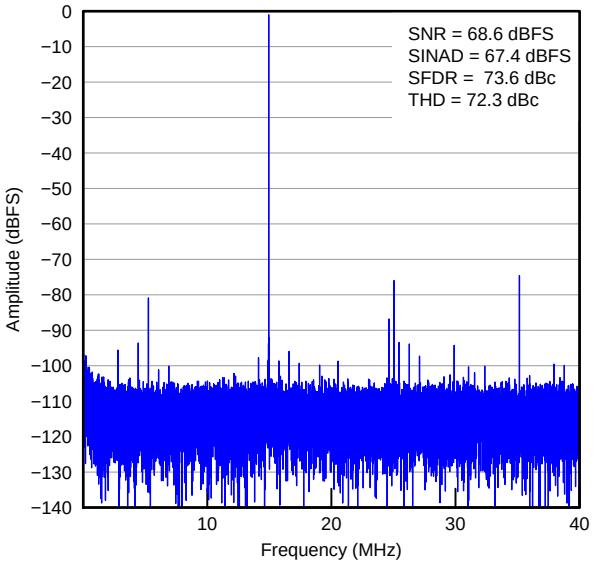


Figure 10. FFT for 65 MHz Input Signal, Sample Rate = 80 MSPS

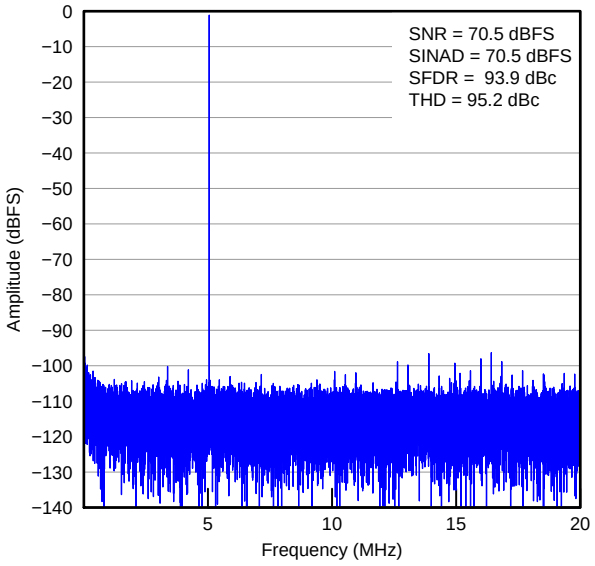


Figure 11. FFT for 5 MHz Input Signal, Sample Rate = 40 MSPS

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, 12Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

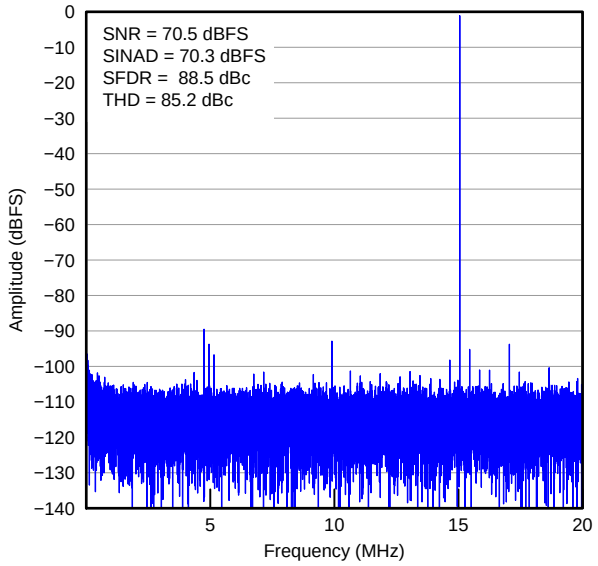


Figure 12. FFT for 15 MHz Input Signal, Sample Rate = 40 MSPS

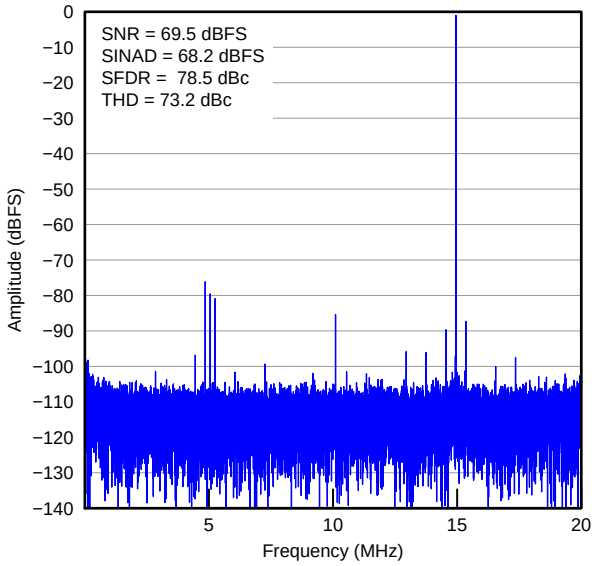


Figure 13. FFT for 65 MHz Input Signal, Sample Rate = 40 MSPS

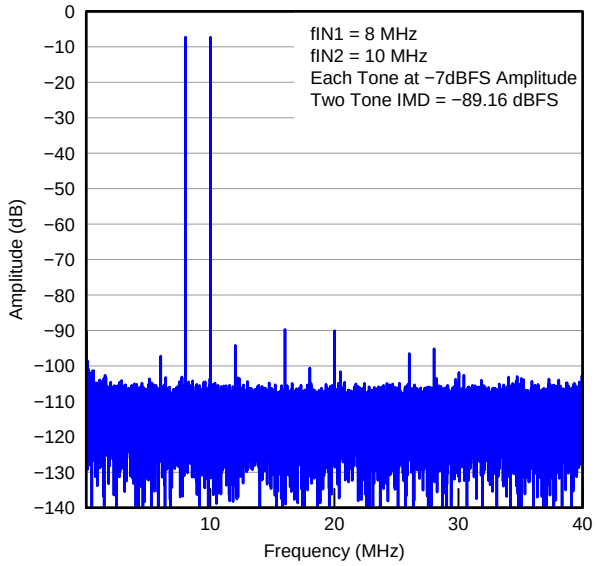


Figure 14. FFT with Two Tone Signal

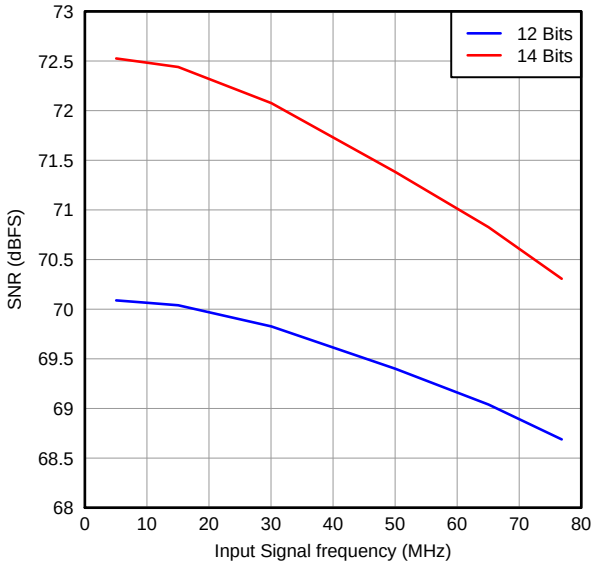


Figure 15. Signal-to-Noise Ratio Across Input Signal Frequency

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, 12Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

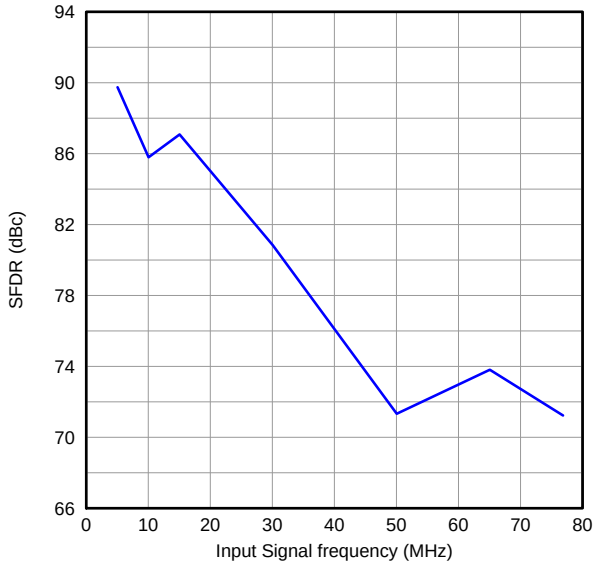


Figure 16. Spurious-Free Dynamic Range

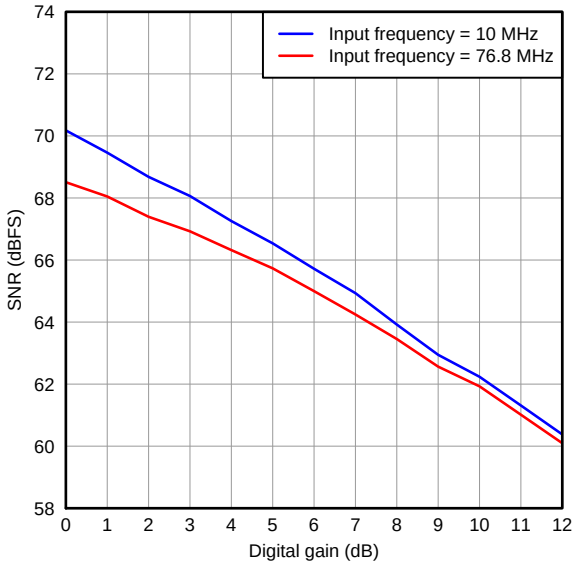


Figure 17. Signal-to-Noise Ratio vs. Digital Gain

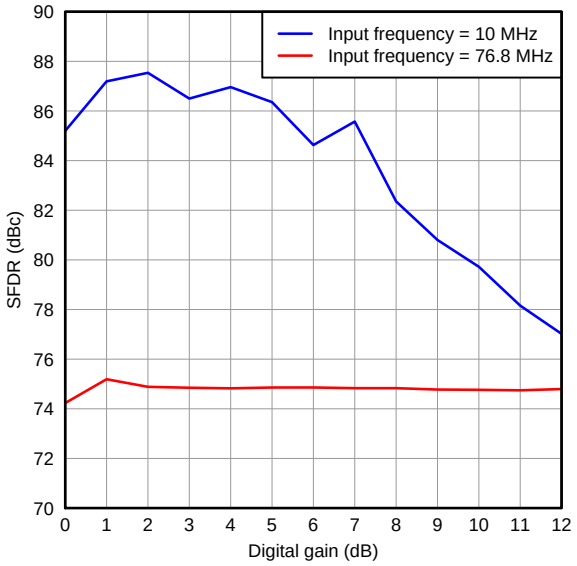


Figure 18. Spurious-Free Dynamic Range vs. Digital Gain

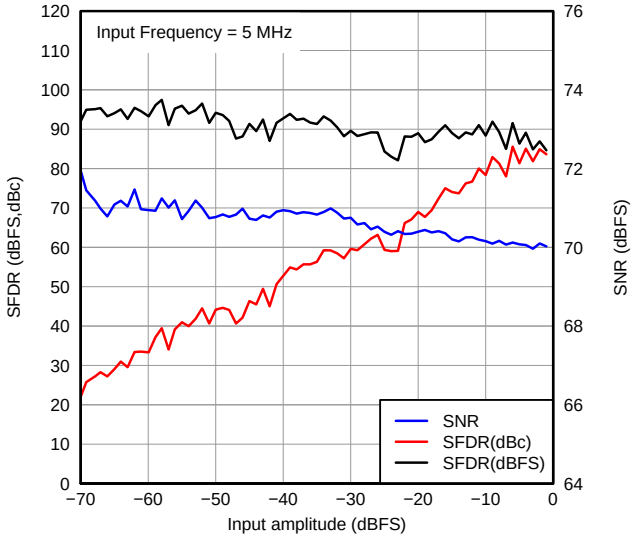


Figure 19. Performance vs. Input Amplitude

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, 12Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

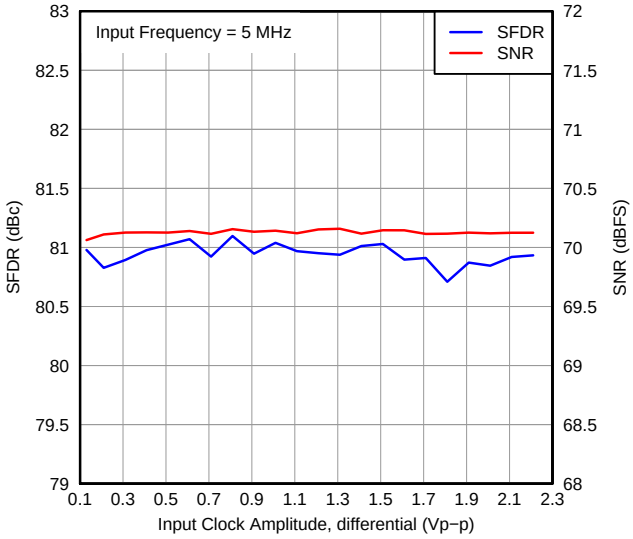


Figure 20. Performance vs. Clock Input Amplitudes

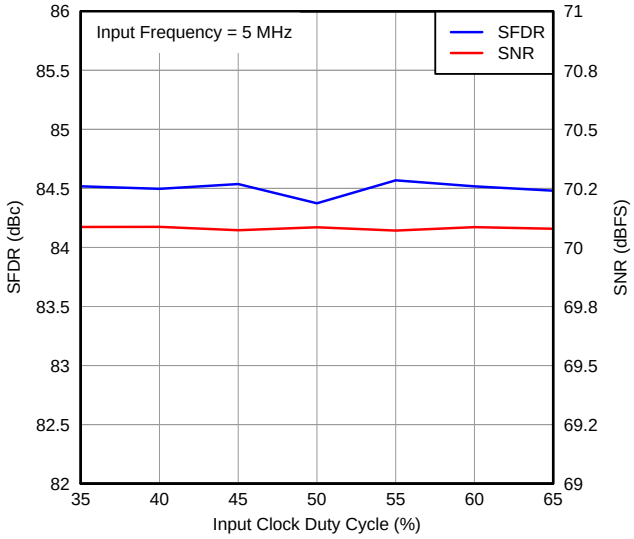


Figure 21. Performance vs. Input Clock Duty Cycle

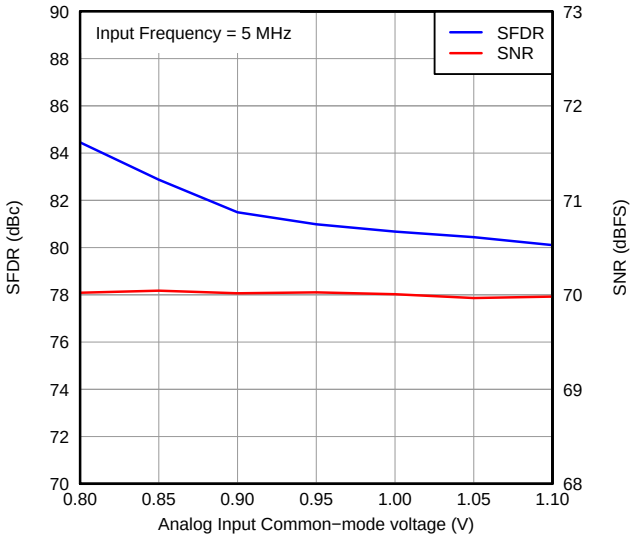


Figure 22. Performance vs. Input VCM

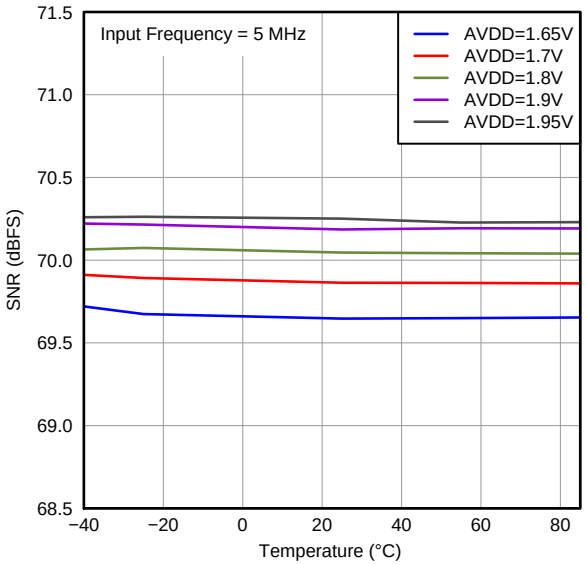


Figure 23. Signal-to-Noise Ratio Across AVDD and Temperature

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, 12Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

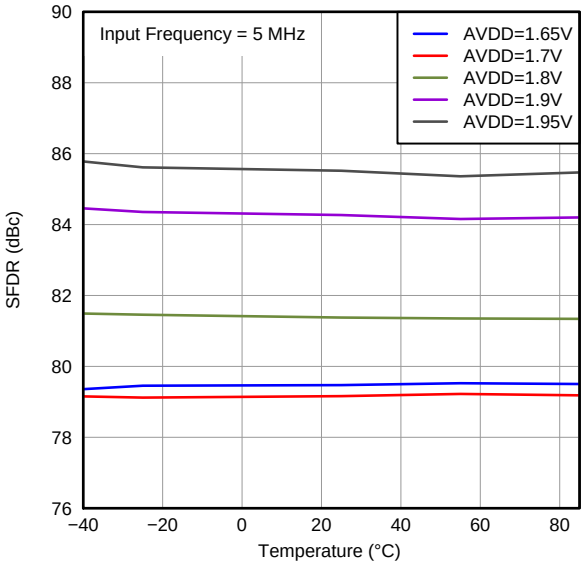


Figure 24. Spurious-Free Dynamic Range Across AVDD and Temperature

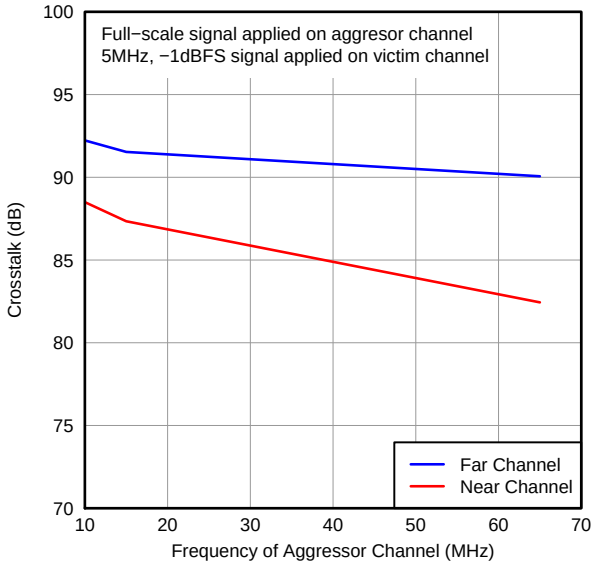


Figure 25. Crosstalk vs. Frequency

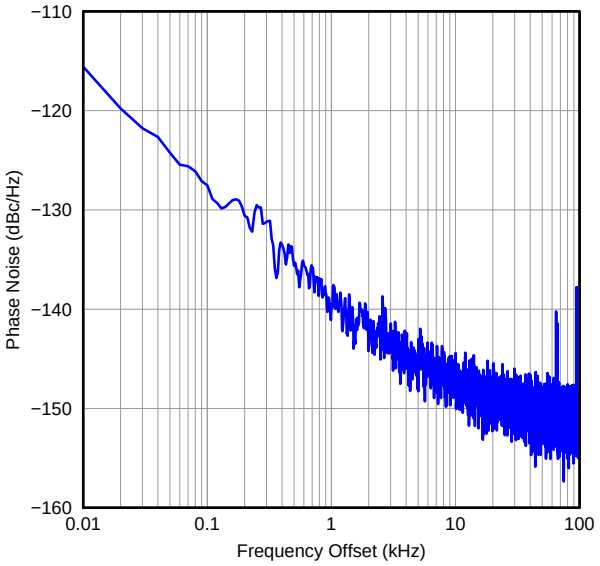


Figure 26. Phase Noise for 5 MHz Input Signal, Sample rate = 80 MSPS

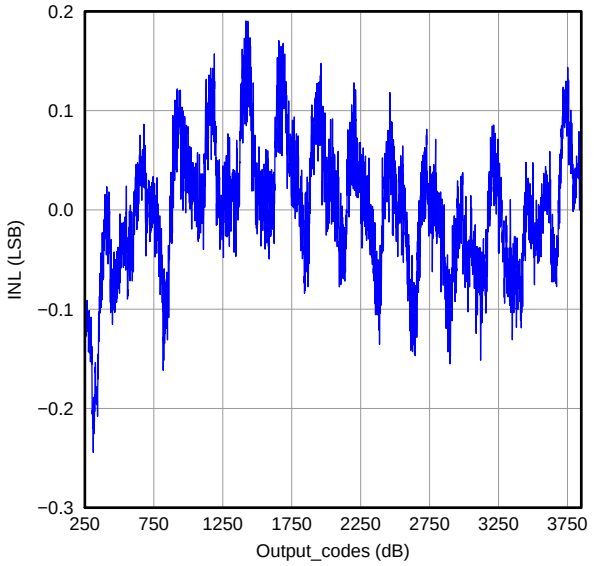


Figure 27. Integral Non-Linearity

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, 12Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

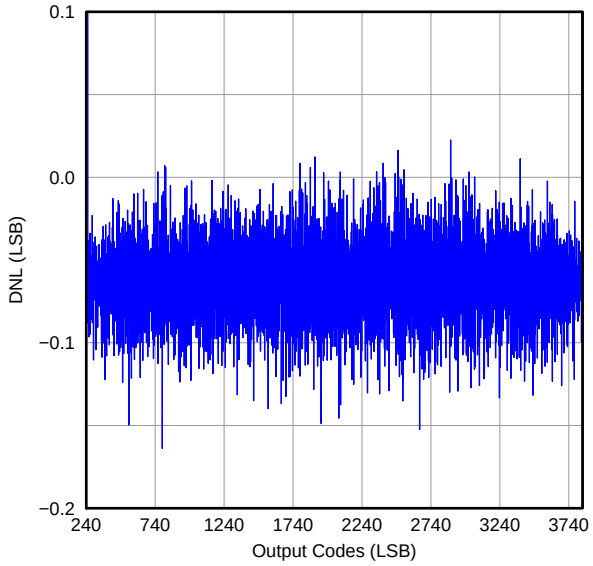


Figure 28. Differential Non-Linearity

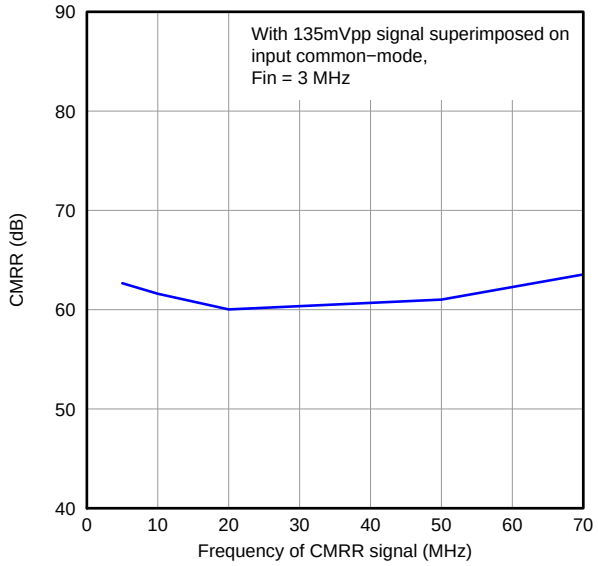


Figure 29. CMRR Across Frequency

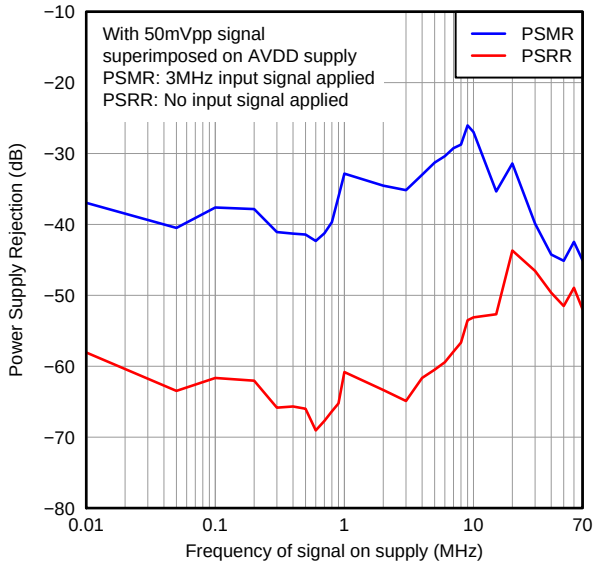


Figure 30. PSRR and PSMR Across Frequency

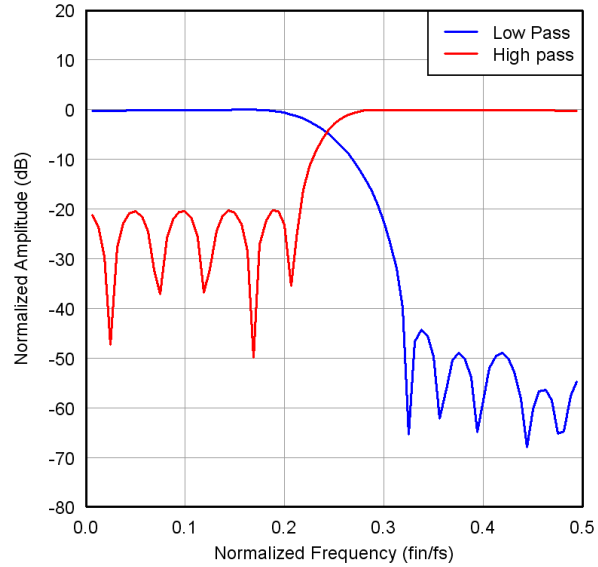


Figure 31. Filter Response, Decimate by 2

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, 12Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

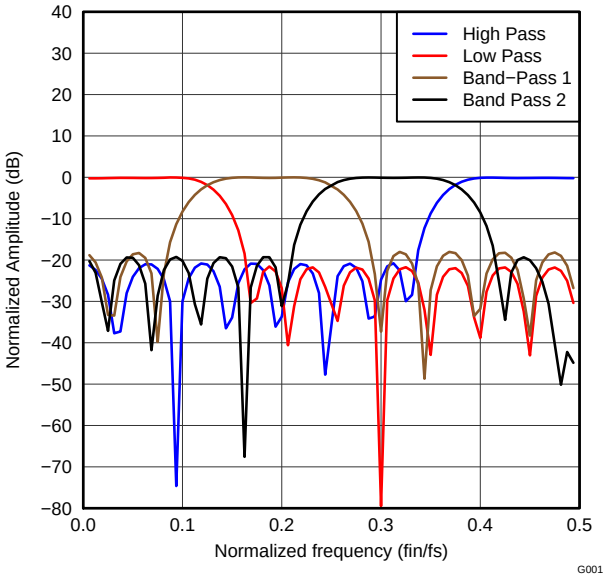


Figure 32. Filter Response, Decimate by 4

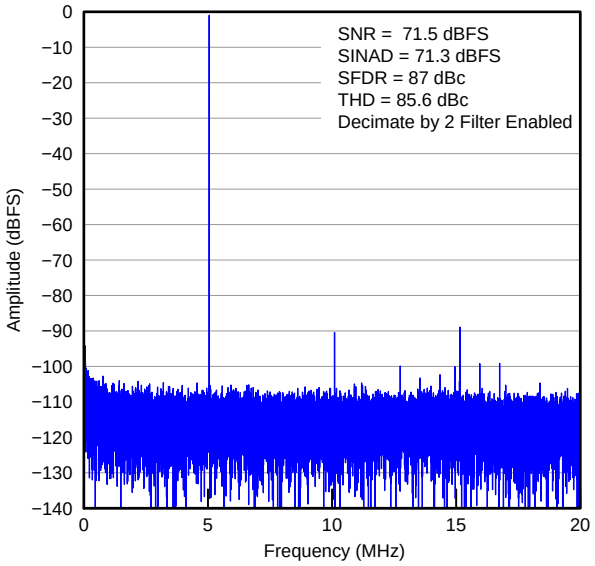


Figure 33. FFT for 5 MHz Input Signal, Sample Rate = 80 MSPS with Decimation Filter = 2

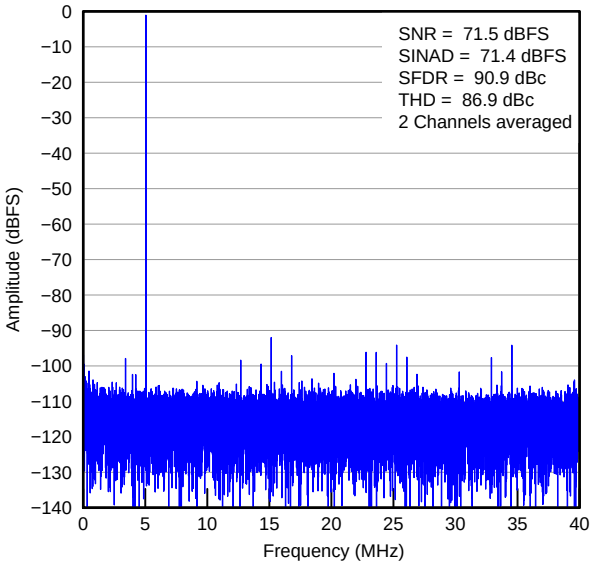


Figure 34. FFT for 5 MHz Input Signal, Sample Rate = 80 MSPS by Averaging 2 Channels

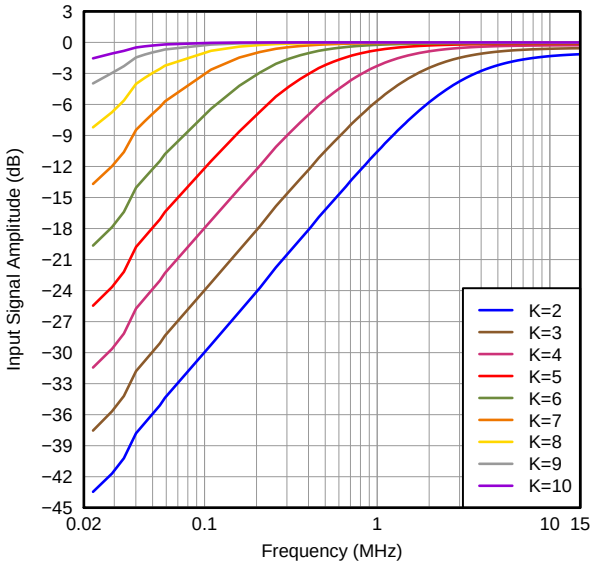


Figure 35. Digital High-Pass Filter Response

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, 12Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

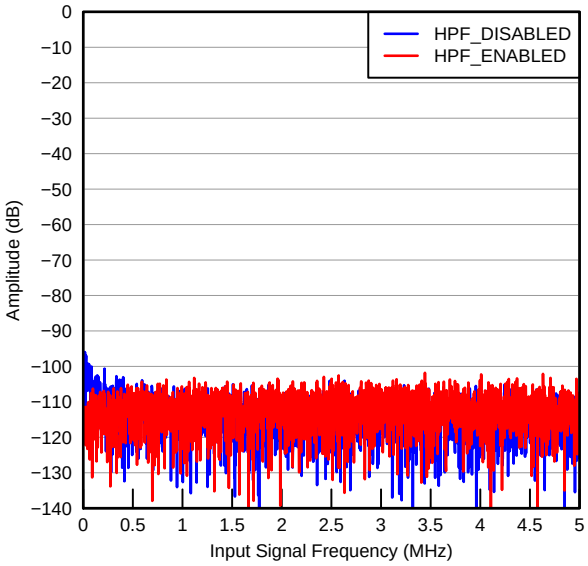


Figure 36. FFT with HPF Enabled and Disabled, No Signal

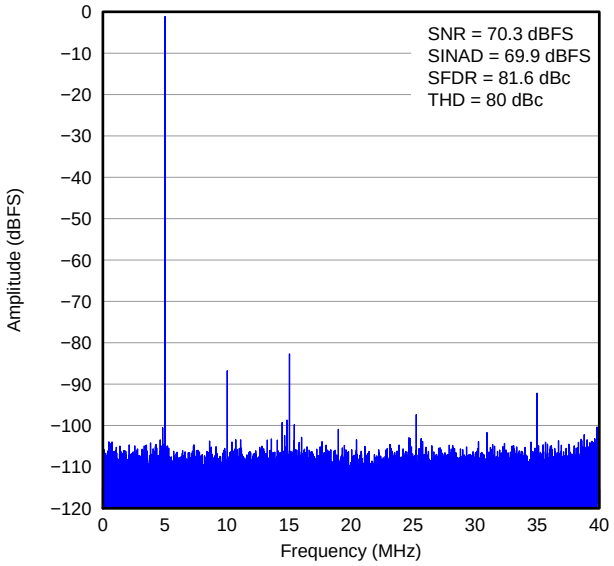


Figure 37. FFT (Full-Band) for 5 MHz Input Signal, Sample Rate = 80 MSPS with Low Frequency Noise Suppression Enabled

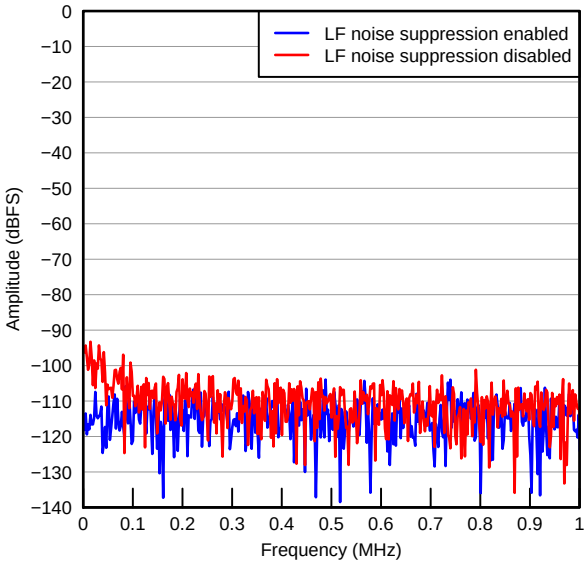


Figure 38. FFT (0 to 1 MHz) for 5 MHz Input Signal, Sample Rate = 80 MSPS with Low Frequency Noise Suppression Enabled

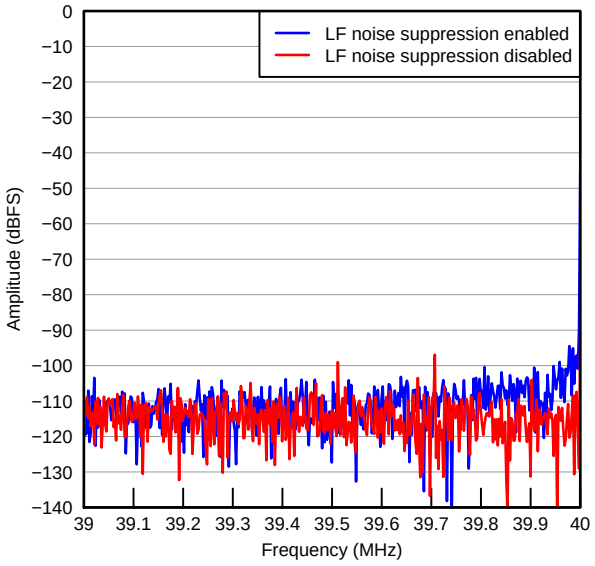


Figure 39. FFT (39 MHz to 40 MHz) for 5 MHz Input Signal, Sample Rate = 80 MSPS with Low Frequency Noise Suppression Enabled

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, 12Bit/80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

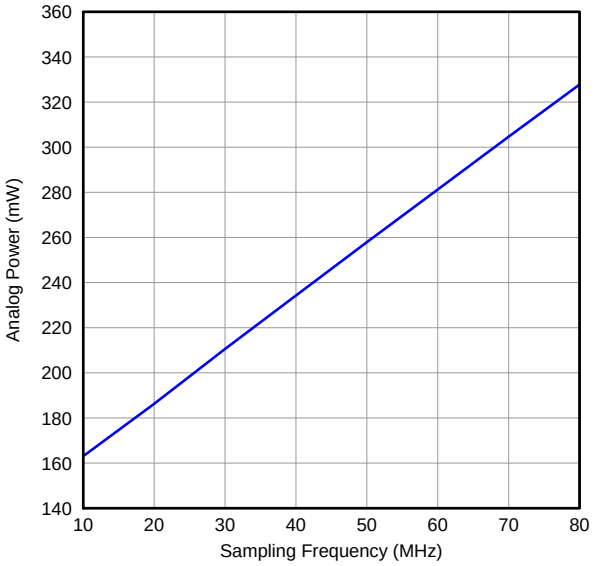


Figure 40. Power Consumption on Analog Supply

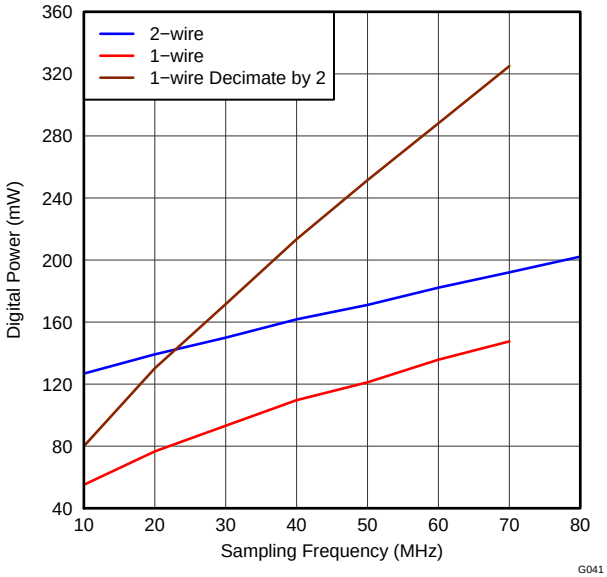


Figure 41. Power Consumption on Digital Supply

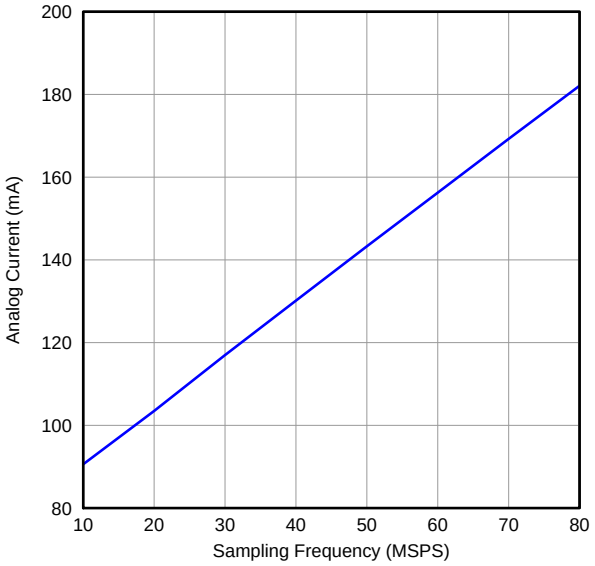


Figure 42. Power Consumption on Analog Supply

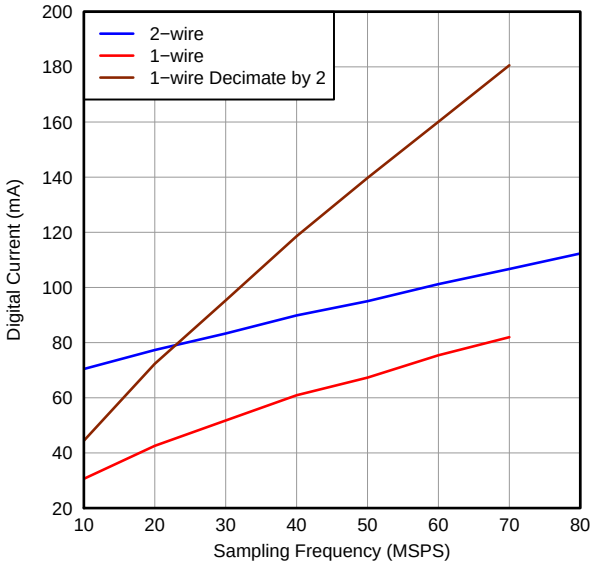


Figure 43. Power Consumption on Digital Supply

SERIAL INTERFACE

ADS5292 has a set of internal registers that can be accessed by the serial interface formed by pins $\overline{CS}$ (Serial interface Enable – Active Low), SCLK (Serial Interface Clock) and SDATA (Serial Interface Data).

When $\overline{CS}$ is low,

- Serial shift of bits into the device is enabled.
- Serial data (SDATA) is latched at every rising edge of SCLK.
- SDATA is loaded into the register at every 24th SCLK rising edge

If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active $\overline{CS}$ pulse. The first eight bits form the register address & the remaining 16 bits the register data. The interface can work with SCLK frequencies from 15 MHz down to very low speeds (few Hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to the respective default values. Initialization can be done in one of two ways:

1. Through a hardware reset, by applying a high pulse on the RESET pin; or
2. Through a software reset; using the serial interface, set the RST bit high. Setting this bit initializes the internal registers to the respective default values and then self-resets the bit low. In this case, the RESET pin stays low (inactive).

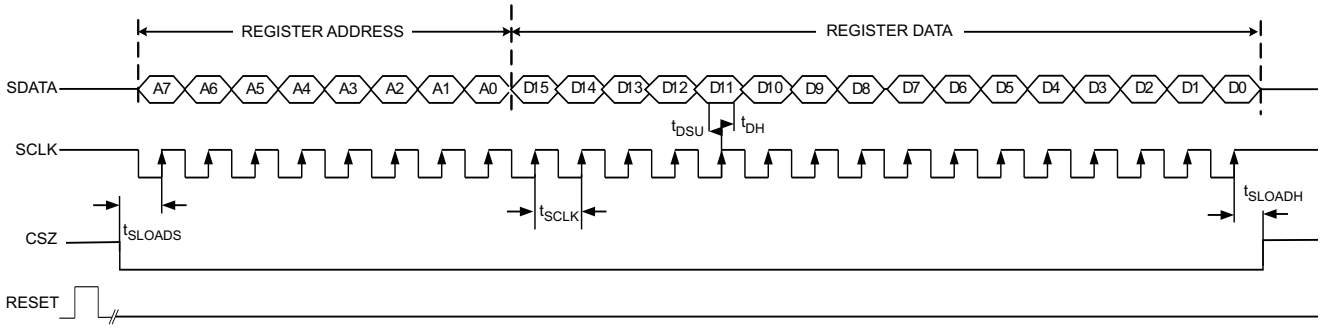


Figure 44. Serial Interface Timing

SERIAL INTERFACE TIMING CHARACTERISTICS

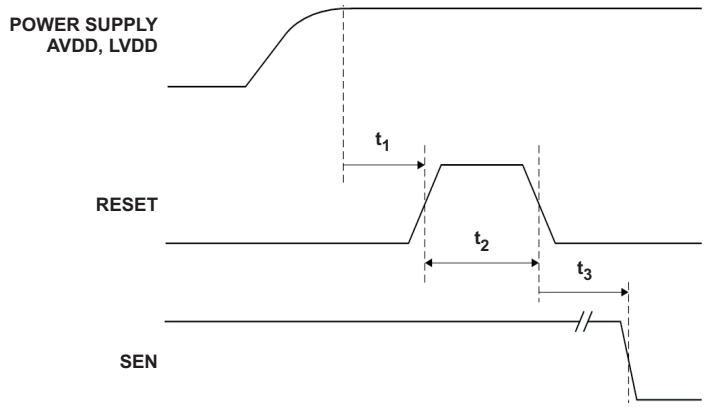
Typical values at 25°C, MIN and MAX values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, LVDD = 1.8 V, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (= 1/ t_{SCLK})	> DC		15	MHz
t_{SLOADS}	$\overline{CS}$ to SCLK setup time	33			ns
t_{SLOADH}	SCLK to $\overline{CS}$ hold time	33			ns
t_{DS}	SDATA setup time	33			ns
t_{DH}	SDATA hold time	33			ns

RESET TIMING

Typical values at 25°C, MIN and MAX values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power up of AVDD and LVDD to RESET pulse active		1		ms
t_2	Reset pulse duration	Pulse duration of active RESET signal	50			ns
t_3	Register write delay	Delay from RESET disable to $\overline{CS}$ active		100		ns



NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET has to be tied permanently HIGH.

Figure 45. Reset Timing Diagram

Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back on SDOUT pin. This may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

By default, after power up and device reset, the SDOUT pin is in the high-impedance state. When the readout mode is enabled using the register bit <READOUT>, SDOUT outputs the contents of the selected register serially, described as follows.

- Set register bit <READOUT> = 1 to put the device in serial readout mode. This disables any further writes into the internal registers, EXCEPT the register at address 1. Note that the <READOUT> bit itself is also located in register 1.
  The device can exit readout mode by writing <READOUT> to 0.
  Only the contents of register at address 1 cannot be read in the register readout mode.
- Initiate a serial interface cycle specifying the address of the register (A7-A0) whose content is to be read.
- The device serially outputs the contents (D15–D0) of the selected register on the SDOUT pin.
- The external controller can latch the contents at the rising edge of SCLK.
- To exit the serial readout mode, reset register bit <READOUT> = 0, which enables writes into all registers of the device. At this point, the SDOUT pin enters the high-impedance state.

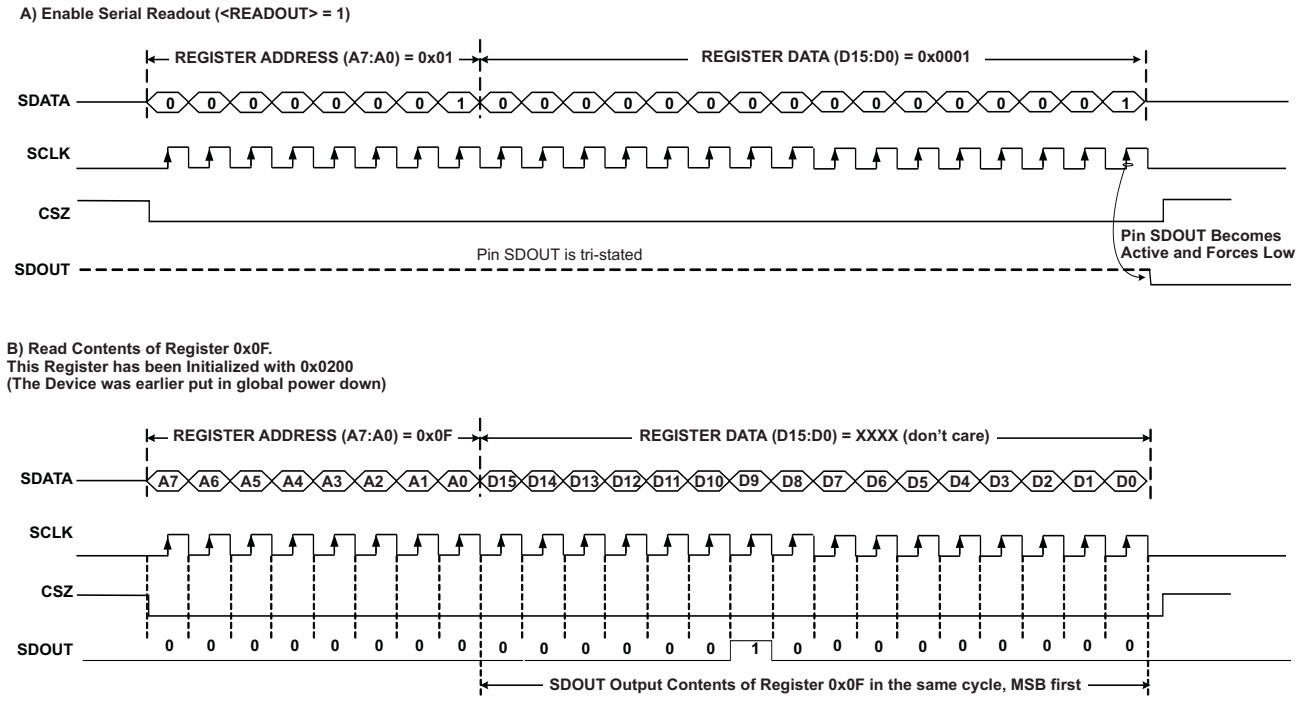


Figure 46. Serial Readout Timing

DEFAULT STATES AFTER RESET

- Device is in normal operation mode with 12-bit ADC enabled for all channels.
- Output interface is 1-wire, 12× serialization with 6×bit clock and 1×frame clock frequency
- Serial readout is disabled
- PDN pin is configured as global power-down pin
- Digital gain is set to 0 dB.
- Digital modes such as LFNS, digital filters, and so on, are disabled.

Register Map

Table 3. Summary of Functions Supported by Serial Interface (1)(2)(3)(4)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
00																X	RST	1: Self-clearing software RESET; . After reset, this bit is set to 0 0: Normal operation.
01																X	EN_READOUT	1: READOUT of registers mode;0: Normal operation
												X					EN_HIGH_ADDRS	0 – Disable access to register at address 0xF0 1 – Enable access to register at address 0xF0
02			X														EN_SYNC	1:Enable SYNC feature to synchronize the test patterns; 0: SYNC feature is disabled for the test patterns. Note: this bit needs to be set as 1 when software or hardware test pattern SYNC feature is used. see Reg.0x25[8] and 0x25[15].
0A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	RAMP_PAT_RESET_VAL	Ramp pattern reset value
0F									X	X	X	X	X	X	X	X	PDN_CH<8:1>	1:Channel-specific ADC power-down mode; 0: Normal operation
								X									PDN_PARTIAL	1:Partial power-down mode - fast recovery from power-down; 0: Normal operation
							X										PDN_COMPLETE	1:Register mode for complete power-down - slower recovery; 0: Normal operation
						X											PDN_PIN_CFG	1:Configures PD pin for partial power-down mode; 0:Configures PD pin for complete power-down mode
14									X	X	X	X	X	X	X	X	LFNS_CH<8:1>	1: Channel-specific low frequency noise suppression mode enable; 0: LFNS disabled
1C		X															EN_FRAME_PAT	1: Enables output frame clock to be programmed through a pattern; 0: Normal operation on frame clock
			X	X	X	X	X	X	X	X	X	X	X	X	X	X	ADCLKOUT<13:0>	14-bit pattern for frame clock on ADCLKP/ADCLKN pins
23	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PRBS_SEED<15:0>	PRBS pattern starting seed value lower 16 bits
24									X	X	X	X	X	X	X	X	INVERT_CH<8:1>	1: Swaps the polarity of the analog input pins electrically; 0: Normal configuration
	X	X	X	X	X	X	X										PRBS_SEED<22:16>	PRBS seed starting value upper 7 bits

(1) The unused bits in each register (identified as blank table cells) must be programmed as '0'.
(2) X = Register bit referenced by the corresponding name and description
(3) Bits marked as '0' should be forced to 0, and bits marked as '1' should be forced to 1 when the particular register is programmed.
(4) Multiple functions in a register can be programmed in a single write operation.

Table 3. Summary of Functions Supported by Serial Interface [1][2][3][4] (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
25										X	0	0					EN_RAMP	1: Enables a repeating full scale ramp pattern on the outputs; 0: Normal operation
										0	X	0					DUALCUSTOM_PAT	1:Enables mode wherein output toggles between 2 defined codes; 0: Normal operation
										0	0	X					SINGLE_CUSTOM_PAT	1: Enables mode wherein output is a constant specified code; 0: Normal operation
															X	X	BITS_CUSTOM1<13:12>	2 MSBs for single custom pattern (and for the first code of the dual custom patterns)
													X	X			BITS_CUSTOM2<13:12>	2 MSBs for second code of the dual custom patterns
								X									TP_SOFT_SYNC	1: Software sync bit for Test patterns on all 8 CHs; 0: No sync. Note: in order to synchronize the digital filters using the SYNC pin, this bit must be set as 0.
				X													PRBS_TP_EN	1: PRBS test pattern enable bit; 0: PRBS test pattern disabled
			X														PRBS_MODE_2	PRBS 9 bit LFSR (23bit LFSR is default)
		X															PRBS_SEED_FROM_REG	1: Enable PRBS seed to be chosen from register 0x23 and 0x24; 0: Disabled
	X																TP_HARD_SYNC	1: Enable the external SYNC feature for syncing test patterns. 0: Inactive. Note: in order to synchronize the digital filters using the SYNC pin, this bit must be set as 0.
26	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM1<11:0>	12 lower bits for single custom pattern (and for the first code of the dual custom pattern).
27	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM2<11:0>	12 lower bits for second code of the dual custom pattern
28	X																EN_BITORDER	Enables the bit order output. 0 = Byte wise, 1 = Word wise
	0							X									BIT_WISE	Selects between bytewise and bit wise 1: bit-wise, odd bits come out on one wire and even bits come out on other wire 0: byte-wise, upper bits on one wire and lower bits on other wire. Note: D15 must be set to '0' for this mode
	1								X	X	X	X	X	X	X	X	EN_WORDWISE__BY_CH<7:0>	1: Output format is one sample on one LVDS wire and next sample on other LVDS wire. 0: Data comes out in two-wire mode with upper set of bits on one channel and lower set of bits on the other. Note: D15 must set '1' for this mode.
29															X		GLOBAL_EN_FILTER	1: Enables filter blocks - global control; 0: Inactive
																X	EN_CHANNEL_AVG	1: Enables channel averaging mode; 0: Inactive
2A													X	X	X	X	GAIN_CH1<3:0>	Programmable gain - Channel 1
									X	X	X	X					GAIN_CH2<3:0>	Programmable gain - Channel 2
					X	X	X	X									GAIN_CH3<3:0>	Programmable gain - Channel 3
	X	X	X	X													GAIN_CH4<3:0>	Programmable gain - Channel 4

Table 3. Summary of Functions Supported by Serial Interface (1)(2)(3)(4) (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
2B	X	X	X	X													GAIN_CH5<3:0>	Programmable gain - Channel 5
					X	X	X	X									GAIN_CH6<3:0>	Programmable gain - Channel 6
									X	X	X	X					GAIN_CH7<3:0>	Programmable gain - Channel 7
													X	X	X	X	GAIN_CH8<3:0>	Programmable gain - Channel 8
2C						X	X										AVG_CTRL4<1:0>	1: Averaging control for what comes out on LVDS output OUT4
									X	X							AVG_CTRL3<1:0>	Averaging control for what comes out on LVDS output OUT3
												X	X				AVG_CTRL2<1:0>	Averaging control for what comes out on LVDS output OUT2
															X	X	AVG_CTRL1<1:0>	Averaging control for what comes out on LVDS output OUT1
2D						X	X										AVG_CTRL8<1:0>	Averaging control for what comes out on LVDS output OUT8
									X	X							AVG_CTRL7<1:0>	Averaging control for what comes out on LVDS output OUT7
												X	X				AVG_CTRL6<1:0>	Averaging control for what comes out on LVDS output OUT6
															X	X	AVG_CTRL5<1:0>	Averaging control for what comes out on LVDS output OUT5
2E							X	X	X								FILTER1_COEFF_SET<2:0>	Select stored coefficient set for filter 1
										X	X	X					FILTER1_RATE<2:0>	Set decimation factor for filter 1
														X			ODD_TAP1	Use odd tap filter 1
																X	USE_FILTER1	1: Enables filter for channel 1; 0: Disables
			X	X	X	X											HPF_CORNER _CH1	HPF corner in values k from 2 to 10
		X															HPF_EN_CH1	1: HPF filter enable for the channel; 0: Disables
2F							X	X	X								FILTER2_COEFF_SET<2:0>	Select stored coefficient set for filter 2
										X	X	X					FILTER2_RATE<2:0>	Set decimation factor for filter 2
														X			ODD_TAP2	Use odd tap filter 2
																X	USE_FILTER2	1: Enables filter for channel 2; 0: Disables
			X	X	X	X											HPF_CORNER _CH2	HPF corner in values k from 2 to 10
		X															HPF_EN_CH2	1: HPF filter enabled for the channel; 0: Disabled
30							X	X	X								FILTER3_COEFF_SET<2:0>	Select stored coefficient set for filter 3
										X	X	X					FILTER3_RATE<2:0>	Set decimation factor for filter 3
														X			ODD_TAP3	Use odd tap filter 3
																X	USE_FILTER3	1: Enables filter for channel 3; 0: Disables
			X	X	X	X											HPF_CORNER _CH3	HPF corner in values k from 2 to 10
		X															HPF_EN_CH3	1: HPF filter enabled for the channel; 0: Disabled

Table 3. Summary of Functions Supported by Serial Interface [1][2][3][4] (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
31							X	X	X								FILTER4_COEFF_SET<2:0>	Select stored coefficient set for filter 4
										X	X	X					FILTER4_RATE<2:0>	Set decimation factor for filter 4
														X			ODD_TAP4	Use odd tap filter 4
																X	USE_FILTER4	1: Enables filter for channel 4; 0: Disables
			X	X	X	X											HPF_CORNER _CH4	HPF corner in values k from 2 to 10
		X															HPF_EN_CH4	1: HPF filter enabled for the channel; 0: Disabled
32							X	X	X								FILTER5_COEFF_SET<2:0>	Select stored coefficient set for filter 5
										X	X	X					FILTER5_RATE<2:0>	Set decimation factor for filter 5
														X			ODD_TAP5	Use odd tap filter 5
																X	USE_FILTER5	1: Enables filter for channel 5; 0: Disables
			X	X	X	X											HPF_CORNER _CH5	HPF corner in values k from 2 to 10
		X															HPF_EN_CH5	1: HPF filter enabled for the channel; 0: Disabled
33							X	X	X								FILTER_TYPE6<2:0>	Select stored coefficient set for filter 6
										X							DECBY8_6	Enables decimate by 8 filter 6
											X	X					FILTER_MODE6<1:0>	Set decimation factor for filter 6
														X			ODD_TAP6	Use odd tap filter 6
																X	USE_FILTER6	Enables filter for channel 6
			X	X	X	X											HPF_CORNER _CH6	HPF corner in values k from 2 to 10
		X															HPF_EN_CH6	Hpf filter enable for the channel
34							X	X	X								FILTER_TYPE7<2:0>	Select stored coefficient set for filter 7
										X							DECBY8_7	Enables decimate by 8 filter 7
											X	X					FILTER_MODE7<1:0>	Set decimation factor for filter 7
														X			ODD_TAP7	Use odd tap filter 7
																X	USE_FILTER7	Enables filter for channel 7
			X	X	X	X											HPF_CORNER _CH7	HPF corner in values k from 2 to 10
		X															HPF_EN_CH7	Hpf filter enable for the channel
35							X	X	X								FILTER_TYPE8<2:0>	Select stored coefficient set for filter 8
										X							DECBY8_8	Enables decimate by 8 filter 8
											X	X					FILTER_MODE8<1:0>	Set decimation factor for filter 8
														X			ODD_TAP8	Use odd tap filter 8
																X	USE_FILTER8	1: Enables filter for channel 8; 0: Disables
			X	X	X	X											HPF_CORNER_CH8	HPF corner in values k from 2 to 10
		X															HPF_EN_CH8	1: HPF filter enable for the channel; 0: Disables
38															X	X	DATA_RATE<1:0>	Select output frame clock rate

Table 3. Summary of Functions Supported by Serial Interface (1)(2)(3)(4) (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
42	X												X				EXT_REF_VCM	Drive external reference mode through: D15=D3=1: the VCM pin; D15=D3=0: REFT/REFB pins. Note: 0xF[15] should be set as '1' to enable the external reference mode
										X	X						PHASE_DDR<1:0>	Controls phase of LCLK output relative to data
45															0	X	PAT_DESKEW	1: Enable deskew pattern mode; 0: Inactive
															X	0	PAT_SYNC	1: Enable sync pattern mode; 0: Inactive
46	1															X	EN_2WIRE	1: 2 wire LVDS output; 0: 1 wire LVDS output
	1													X			BTC_MODE	1: 2's complement; (ADC data output format) 0: Binary Offset (ADC data output format)
	1												X				MSB_FIRST	1: MSB First; 0: LSB First
	1											X					EN_SDR	1:SDR Bit Clock; 0: DDR Bit Clock
	1				0	0	X										EN_12BIT	1: Enable 12 bit serialization mode; 0: Inactive
	1				0	X	0										EN_14BIT	1: Enable 14 bit serialization mode; 0: Inactive
	1				X	0	0										EN_16BIT	1: Enable 16 bit serialization mode; 0: Inactive Note: 16 bit can be used when average mode or decimation mode is enabled for better SNR.
	1		X														FALL_SDR	1: Controls LCLK rising or falling edge comes in the middle of data window when operating in SDR output mode; 0: At the edge of data window.
50	1												X	X	X	X	MAP_Ch1234_to_OUT1A	OUT1A Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch1234_to_OUT1B	OUT1B Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch1234_to_OUT2A	OUT2A Pin pair to channel data mapping selection
51	1												X	X	X	X	MAP_Ch1234_to_OUT2B	OUT2B Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch1234_to_OUT3A	OUT3A Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch1234_to_OUT3B	OUT3B Pin pair to channel data mapping selection
52	1												X	X	X	X	MAP_Ch1234_to_OUT4A	OUT4A Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch1234_to_OUT4B	OUT4B Pin pair to channel data mapping selection
53	1												X	X	X	X	MAP_Ch5678_to_OUT5B	OUT5B Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch5678_to_OUT5A	OUT5A Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch5678_to_OUT6B	OUT6B Pin pair to channel data mapping selection
54	1												X	X	X	X	MAP_Ch5678_to_OUT6A	OUT6A Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch5678_to_OUT7B	OUT7B Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch5678_to_OUT7A	OUT7A Pin pair to channel data mapping selection

Table 3. Summary of Functions Supported by Serial Interface (1)(2)(3)(4) (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
55	1												X	X	X	X	MAP_Ch5678_to_OUT8B	OUT8B Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch5678_to_OUT8A	OUT8A Pin pair to channel data mapping selection
F0	X																EN_EXT_REF	0 - Default: internal reference mode 1 - Enable external reference mode. the voltage reference can be applied on either REFP/B pins or VCM pin

DESCRIPTION OF SERIAL REGISTERS

POWER-DOWN MODES

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
0F									X	X	X	X	X	X	X	X	PDN_CH<8:1>
								X									PDN_PARTIAL
							X										PDN_COMPLETE
						X											PDN_PIN_CFG

Each of the 8 channels can be individually powered down. PDN_CH<N> controls the power-down mode for ADC channel <N>. In addition to channel-specific power-down, the ADS5292 also has two global power-down modes:

1. The partial power-down mode. It partially powers down the chip; recovery from this mode is faster in 5 µs, provided that the clock has been running for at least 50 µs before exiting this mode.
2. The complete power-down mode. It completely powers down the chip, and involves a much longer recovery time 100 µs.

In addition to programming the chip in either of these two power-down modes (through either the PDN_PARTIAL or PDN_COMPLETE bits), the PD pin itself can be configured as either a partial power-down pin or a complete power-down pin control. For example, if PDN_PIN_CFG=0 (default), when the PD pin is high, the device enters complete power-down mode. However, if PDN_PIN_CFG=1, when the PD pin is high, the device enters partial power-down mode.

LOW FREQUENCY NOISE SUPPRESSION MODE

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
14									X	X	X	X	X	X	X	X	LFNS_CH<8:1>

The low frequency noise suppression mode is specifically useful in applications where good noise performance is desired in the frequency band of 0 to 1 MHz (around DC). Setting this mode shifts the low-frequency noise of the ADS5292 to approximately Fs/2, thereby, moving the noise floor around DC to a much lower value. LFNS_CH<8:1> enables this mode individually for each channel. See Figure 38 and Figure 39.

ANALOG INPUT INVERT

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
24									X	X	X	X	X	X	X	X	INVERT_CH<8:1>

Normally, IN_P pin represents the positive analog input pin, and INN represents the complementary negative input. Setting the bits marked INVERT_CH<8:1> (individual control for each channel) causes the inputs to be swapped. IN_N now represents the positive input, and IN_P the negative input.

LVDS TEST PATTERNS

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
23	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PRBS_SEED<15:0>
24	X	X	X	X	X	X	X										PRBS_SEED<22:16>
										X	0	0					EN_RAMP
										0	X	0					DUALCUSTOM_PAT
										0	0	X					SINGLE_CUSTOM_PAT
25															X	X	BITS_CUSTOM1<13:12>
													X	X			BITS_CUSTOM2<13:12>
								X									TP_SOFT_SYNC
				X													PRBS_TP_EN
			X														PRBS_MODE_2
		X															PRBS_SEED_FROM_REG
	X																TP_HARD_SYNC
26	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM1<11:0>
27	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM2<11:0>
45															0	X	PAT_DESKEW
															X	0	PAT_SYNC

The ADS5292 can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. All these patterns can be synchronized across devices by the sync function either through the hardware SYNC pin or the software sync bit TP_SOFT_SYNC bit in register 0x25. TP_HARD_SYNC bit when set enables the Test patterns to be synchronized by the hardware SYNC Pin. When the software sync bit TP_SOFT_SYNC bit is set, special timing is needed.

- Setting EN_RAMP to 1 causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1 LSB every clock cycle. After hitting the full scale code, it returns back to zero code and ramps again.
- The device can also be programmed to output a constant code by setting SINGLE_CUSTOM_PAT to 1, and programming the desired code in BITS_CUSTOM1<13:0>. In this mode, BITS_CUSTOM1<13:0> take the place of the 12-bit ADC data at the output, and are controlled by LSB-first and MSB-first modes the same way as normal ADC data are.
- The device may also be made to toggle between two consecutive codes, by programming DUAL_CUSTOM_PAT to 1. The two codes are represented by the contents of BITS_CUSTOM1<13:0> and BITS_CUSTOM2<13:0>.
- In addition to custom patterns, the device may also be made to output two preset patterns:
  - **Deskew patten –** Set using PAT_DESKEW, this mode replaces the 12-bit ADC output D<13:0> with the 0101010101010101 word.
  - **Sync pattern –** Set using PAT_SYNC, the normal ADC word is replaced by a fixed 11111110000000 word.
  - **PRBS patterns:** The device can give 9 bit or 23 bit LFSR Pseudo random pattern on the channel outputs that are controlled by the register 0x25. To enable the PRBS pattern **PRBS_TP_EN** bit in the register 0x25 needs to be set. Default is the 23 bit LFSR but 9 bit LFSR can be chosen by setting **PRBS_MODE_2** bit. The seed value for the PRBS patterns can be chosen by enabling the **PRBS_SEED_FROM_REG** bit to 1 and the value written to the PRBS_SEED registers in 0x24 and 0x23.

Note that only one of the above patterns should be active at any given instant.

BIT-BYTE-WORD WISE OUTPUT

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
28	x																EN_BITORDER
	0							x									BIT_WISE
	1								X	X	X	X	X	X	X	X	EN_WORDWISE_BY_CH<7:>

Register 0x28 can select the LVDS ADC output as bit-wise,byte-wise or word-wise in the two wire mode. Figure 47 and Figure 48 illustrate the details.

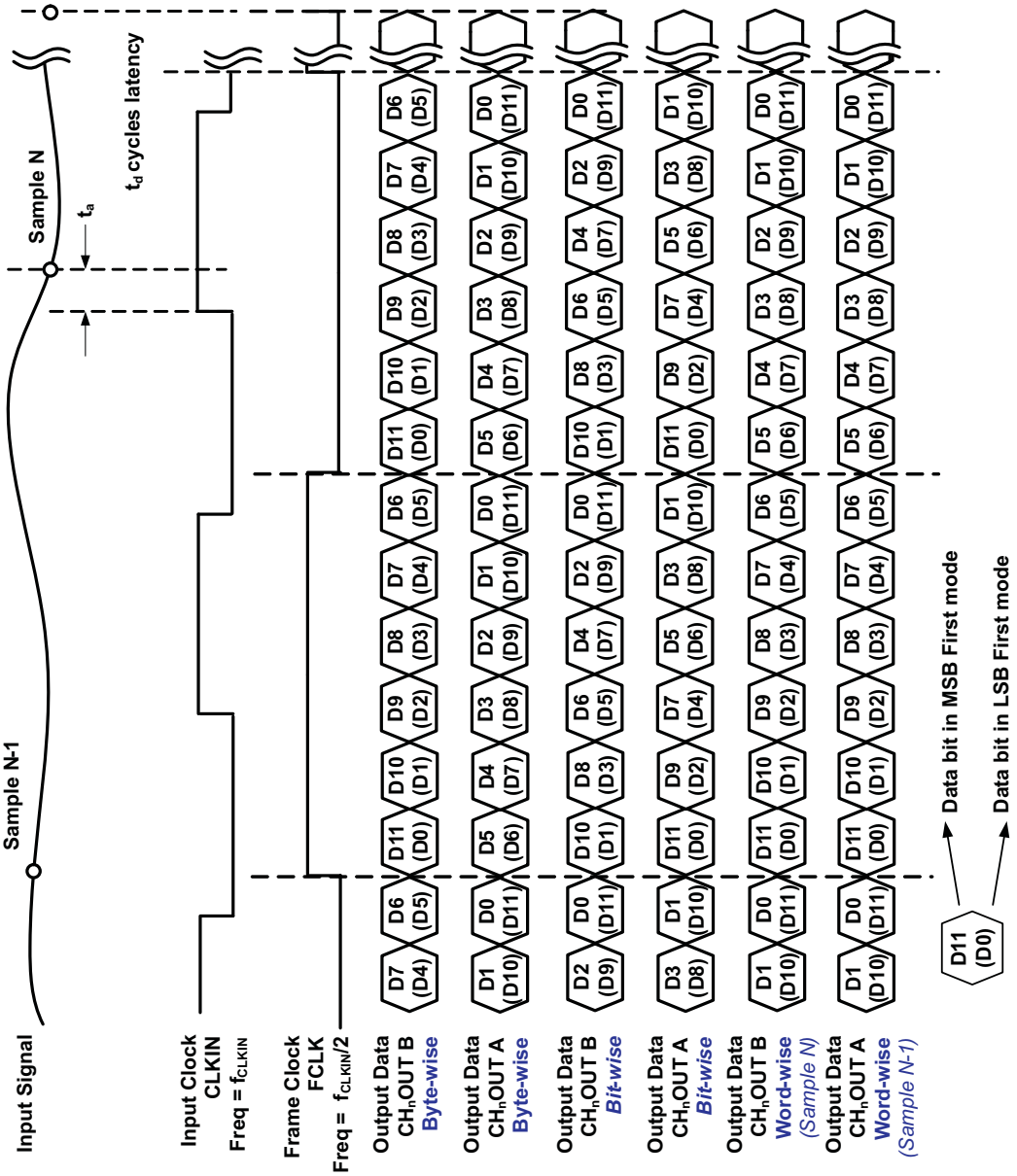


Figure 47. 12-Bit Word Wise

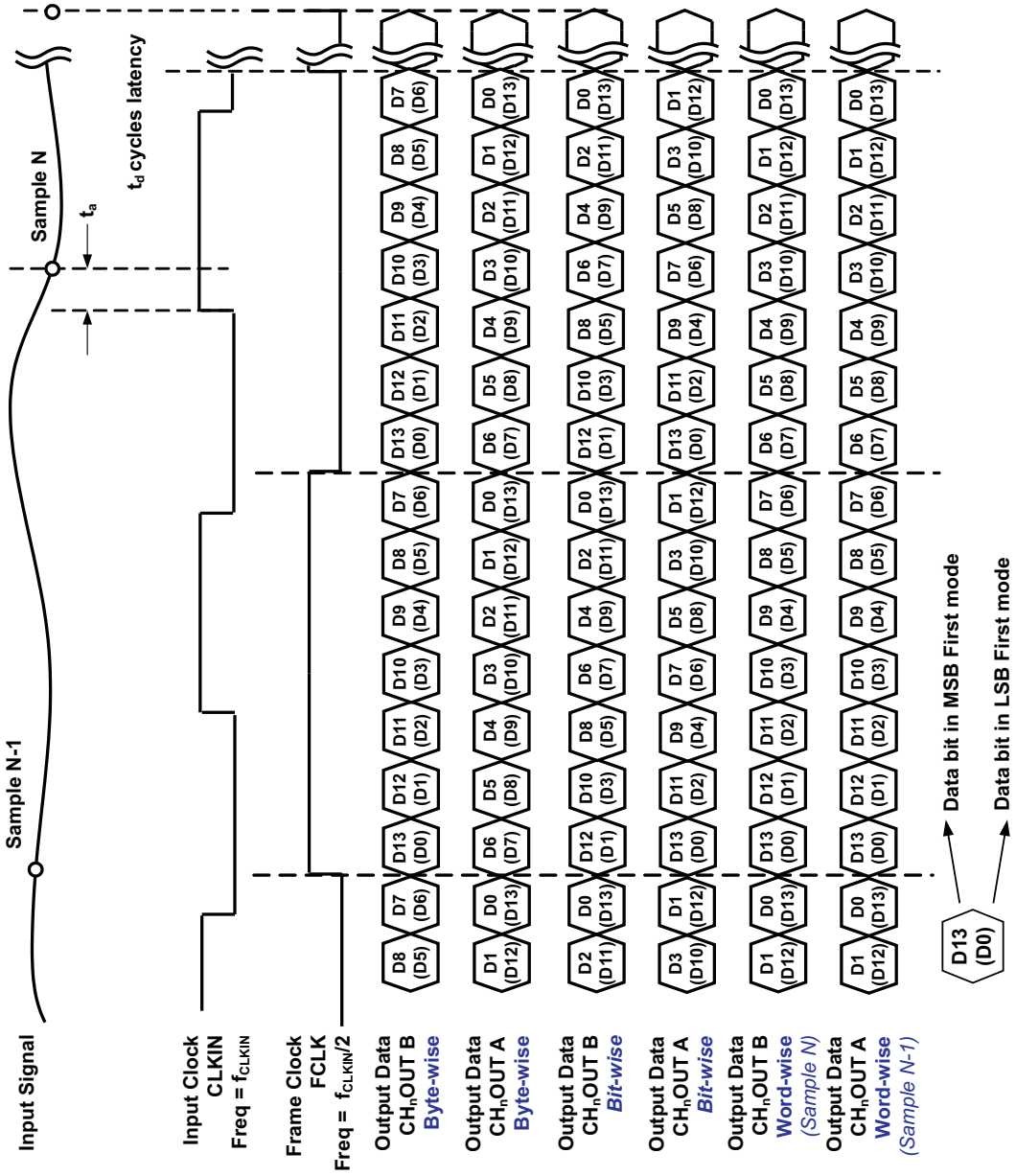


Figure 48. 14-Bit Word Wise

DIGITAL PROCESSING BLOCKS

The ADS5292 integrates a set of commonly useful digital functions that can be used to ease system design. These functions are shown in the digital block diagram of Figure 49 and described in the following sections.

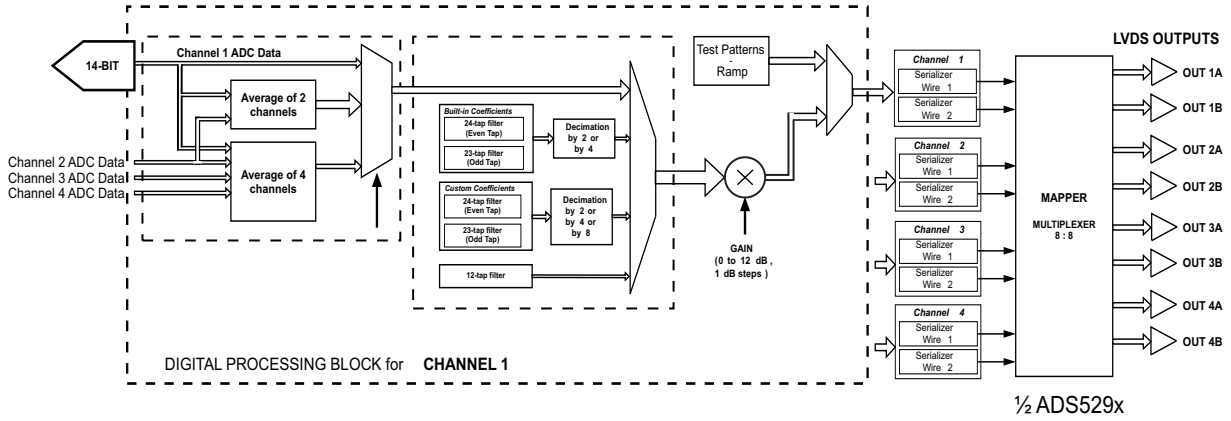


Figure 49. Digital Processing Block Diagram

PROGRAMMABLE DIGITAL GAIN

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
2A													X	X	X	X	GAIN_CH1<3:0>
									X	X	X	X					GAIN_CH2<3:0>
					X	X	X	X									GAIN_CH3<3:0>
	X	X	X	X													GAIN_CH4<3:0>
2B	X	X	X	X													GAIN_CH5<3:0>
					X	X	X	X									GAIN_CH6<3:0>
									X	X	X	X					GAIN_CH7<3:0>
													X	X	X	X	GAIN_CH8<3:0>

In applications where the full scale swing of the analog input signal is much less than the 2 V_{PP} range supported by the ADS5292, a programmable digital gain can be set to achieve the full-scale output code even with a lower analog input swing. The programmable gain for each channel can be individually set using a set of four bits, indicated as GAIN_CHN<3:0> for Channel N. The gain setting is coded in binary from 0-12 dB as shown in Table 4.

Table 4. Gain Setting for Channel N

GAIN_CHN<3>	GAIN_CHN<2>	GAIN_CHN<1>	GAIN_CHN<0>	CHANNEL N GAIN SETTING
0	0	0	0	0 dB
0	0	0	1	1 dB
0	0	1	0	2 dB
0	0	1	1	3 dB
0	1	0	0	4 dB
0	1	0	1	5 dB
0	1	1	0	6 dB
0	1	1	1	7 dB
1	0	0	0	8 dB
1	0	0	1	9 dB
1	0	1	0	10 dB
1	0	1	1	11 dB
1	1	0	0	12 dB
1	1	0	1	Do not use
1	1	1	0	Do not use
1	1	1	1	Do not use

CHANNEL AVERAGING

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
29																X	EN_CHANNEL_AVG
2C						X	X										AVG_CTRL4<1:0>
									X	X							AVG_CTRL3<1:0>
												X	X				AVG_CTRL2<1:0>
															X	X	AVG_CTRL1<1:0>
2D						X	X										AVG_CTRL8<1:0>
									X	X							AVG_CTRL7<1:0>
												X	X				AVG_CTRL6<1:0>
															X	X	AVG_CTRL5<1:0>

In the default mode of operation, the LVDS outputs <8..1> contain the data of the ADC Channels <8..1>. By setting the EN_CHANNEL_AVG bit to '1', the outputs from multiple channels can be averaged. The resulting outputs from the Channel averaging block (which is bypassed in the default mode) are referred to as Bins. The contents of the Bins <8..1> come out on the LVDS outputs <8..1>. The contents of each of the 8 bins are determined by the register bits marked AVG_CTRL*n*<1:0> where n stands for the Bin number. The different settings are shown below:

AVG_CTRL1<1>	AVG_CTRL1<0>	Contents of Bin 1
0	0	Zero
0	1	ADC Channel 1
1	0	Average of ADC Channel 1, 2
1	1	Average of ADC Channel 1, 2, 3, 4
AVG_CTRL2<1>	**AVG_CTRL2<0>**	**Contents of Bin 2**
0	0	Zero
0	1	ADC Channel 2
1	0	ADC Channel 3
1	1	Average of ADC Channel 3, 4
AVG_CTRL3<1>	**AVG_CTRL3<0>**	**Contents of Bin 3**
0	0	Zero
0	1	ADC Channel 3
1	0	ADC Channel 2
1	1	Average of ADC Channel 1, 2
AVG_CTRL4<1>	**AVG_CTRL4<0>**	**Contents of Bin 4**
0	0	Zero
0	1	ADC Channel 4
1	0	Average of ADC Channel 3, 4
1	1	Average of ADC Channel 1, 2, 3, 4
AVG_CTRL5<1>	**AVG_CTRL5<0>**	**Contents of Bin 5**
0	0	Zero
0	1	ADC Channel 5
1	0	Average of ADC Channel 5, 6
1	1	Average of ADC Channel 5, 6, 7, 8
AVG_CTRL6<1>	**AVG_CTRL6<0>**	**Contents of Bin 6**
0	0	Zero
0	1	ADC Channel 6
1	0	ADC Channel 7
1	1	Average of ADC Channel 7, 8
AVG_CTRL7<1>	**AVG_CTRL7<0>**	**Contents of Bin 7**
0	0	Zero

AVG_CTRL1<1>	AVG_CTRL1<0>	Contents of Bin 1
0	1	ADC Channel 7
1	0	ADC Channel 6
1	1	Average of ADC Channel 6, 5
AVG_CTRL8<1>	**AVG_CTRL8<0>**	**Contents of Bin 8**
0	0	Zero
0	1	ADC Channel 8
1	0	Average of ADC Channel 7, 8
1	1	Average of ADC Channel 5, 6, 7, 8

When the contents of a particular bin is set to Zero, then the LVDS buffer corresponding to that bin gets automatically powered down.

DECIMATION FILTER

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
29															X		GLOBAL_EN_FILTER
2E							X	X	X								FILTER1_COEFF_SET<2:0>
										X	X	X					FILTER1_RATE<2:0>
														X			ODD_TAP1
																X	USE_FILTER1
2F							X	X	X								FILTER2_COEFF_SET<2:0>
										X	X	X					FILTER2_RATE<2:0>
														X			ODD_TAP2
																X	USE_FILTER2
30							X	X	X								FILTER3_COEFF_SET<2:0>
										X	X	X					FILTER3_RATE<2:0>
														X			ODD_TAP3
																X	USE_FILTER3
31							X	X	X								FILTER4_COEFF_SET<2:0>
										X	X	X					FILTER4_RATE<2:0>
														X			ODD_TAP4
																X	USE_FILTER4
32							X	X	X								FILTER5_COEFF_SET<2:0>
										X	X	X					FILTER5_RATE<2:0>
														X			ODD_TAP5
																X	USE_FILTER5
33							X	X	X								FILTER6_COEFF_SET<2:0>
										X	X	X					FILTER6_RATE<2:0>
														X			ODD_TAP6
																X	USE_FILTER6
34							X	X	X								FILTER7_COEFF_SET<2:0>
										X	X	X					FILTER7_RATE<2:0>
														X			ODD_TAP7
																X	USE_FILTER7
35							X	X	X								FILTER8_COEFF_SET<2:0>
										X	X	X					FILTER8_RATE<2:0>
														X			ODD_TAP8
																X	USE_FILTER8

The decimation filter is implemented as 24-tap FIR with symmetrical coefficients (each coefficient is 12-bit signed). The filter equation is:

$$y(n) = \left(\frac{1}{2^{11}}\right) \times \left[(h_0 \times x(n) + h_1 \times x(n-1) + h_2 \times x(n-2) + \ldots + h_{11} \times x(n-11) + h_{11} \times x(n-12) \ldots + h_1 \times x(n-22) + h_0 \times x(n-23)\right] \quad (1)$$

By setting the register bit <ODD_TAPn> = 1, a 23-tap FIR is implemented:

$$y(n)=\left(\frac{1}{2^{11}}\right)\times\left[(h_0\times x(n)+h_1\times x(n-1)+h_2\times x(n-2)+\ldots+h_{10}\times x(n-10)+h_{11}\times x(n-11)+h_{10}\times x(n-12)\ldots+h_1\times x(n-21)+h_0\times x(n-22)\right] \quad (2)$$

In Equation 1 and Equation 2, *h0, h1 …h_{11}* are 12 bit signed representation of the coefficients, *x(n)* is the input data sequence to the filter and *y(n)* is the filter output sequence.

A decimation filter can be introduced at the output of each channel. To enable this feature, the GLOBAL_EN_FILTER should be set to '1'. Setting this bit to '1' increases the overall latency of each channel to 20 clock cycles irrespective of whether the filter for that particular channel has been chosen or not (using the USE_FILTER bit). The bits marked FILTER*n*_COEFF_SET<2:0>, FILTER*n*_RATE<2:0>, ODD_TAP*n* and USE_FILTER*n* represent the controls for the filter for Channel *n*. Note that these bits are functional only when the GLOBAL_EN_FILTER gets set to '1'. For illustration, the controls for channel 1 are listed in Table 5:

The USE_FILTER1 bit determines whether the filter for Channel 1 is used or not. When this bit is set to '1', the filter for channel 1 is enabled. When this bit is set to '0', the filter for channel 1 is disabled but the channel data passes through a dummy delay so that the overall latency of channel 1 is 20 clock cycles. With the USE_FILTER1 bit set to '1', the characteristics of the filter can be set by using the other sets of bits.

The ADS5292 has 6 sets of filter coefficients stored in memory. Each of these sets define a unique pass band in the frequency domain and contain 12 coefficients (each coefficient is 12-bit long). These 12 coefficients are used to implement either a symmetric 24-tap (even-tap) filter, or a symmetric 23-tap (odd-tap) filter. Setting the register bit ODD_TAP1 to '1' enables the odd-tap configuration (the default is even tap with this bit set to '0') for Channel 1. The bits FILTER1_COEFF_SET<2:0> can be used to choose the required set of coefficients for Channel 1.

The passbands corresponding to of each of these filter coefficient sets is shown in Figure 50

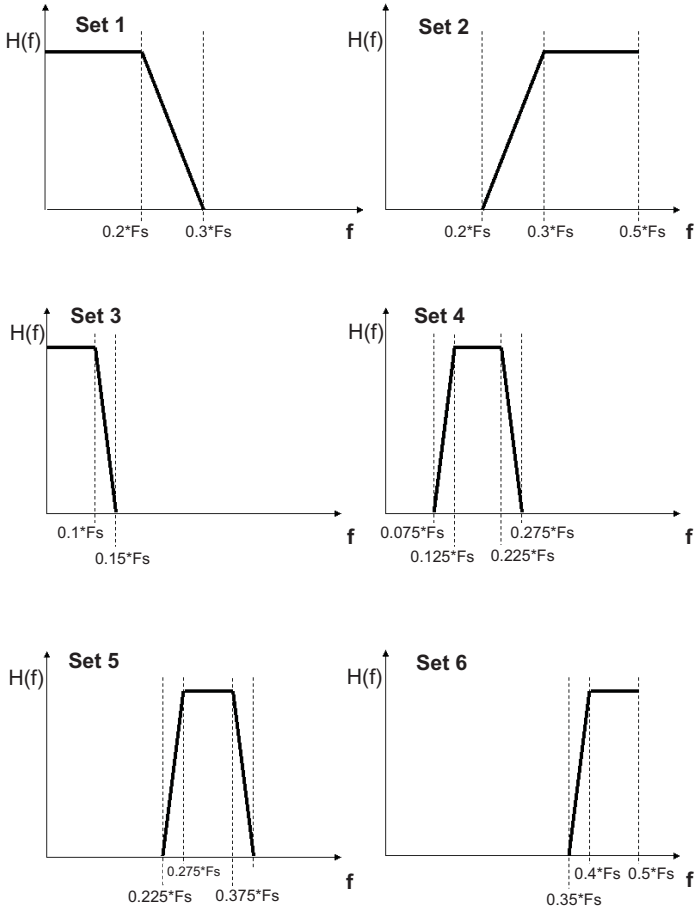


Figure 50. Filter Types

Coefficient Sets 1 and 2 are the most appropriate when Decimation by a factor of 2 is required, whereas Coefficient Sets 3,4,5,6 are appropriate when Decimation by a factor of 4 is desired. The computation rate of the filter output can be independently set using the bits FILTERn_RATE<2:0>. The settings are shown in Table 5.

Table 5. Digital Filters

DECIMATION	TYPE OF FILTER	<DATA RATE>	FILTERn RATE>	<FILTERn COEFF SET>	<ODD TAP>	<USE FILTER CHn>	<EN CUSTOM FILT>
Decimate by 2	Built-in **low-pass odd-tap** filter (pass band = 0 to f_S/4)	001	000	000	1	1	0
	Built-in **high-pass odd-tap** filter (pass band = 0 to f_S/4)	001	000	001	1	1	0
Decimate by 4	Built-in **low-pass even-tap** filter (pass band = 0 to f_S/8)	010	001	010	0	1	0
	Built-in first **band pass even tap** filter(pass band = f_S/8 to f_S/4)	010	001	011	0	1	0
	Built-in second **band pass even tap** filter(pass band = f_S/4 to 3 f_S/8)	010	001	100	0	1	0
	Built-in **high pass odd tap** filter (pass band = 3 f_S/8 to f_S/2)	010	001	101	1	1	0
Decimate by 2	Custom filter (user programmablecoefficients)	001	000	000	0 and 1	1	1
Decimate by 4	Custom filter (user programmablecoefficients)	010	001	000	0 and 1	1	1
Decimate by 8	Custom filter (user programmablecoefficients)	011	100	000	0 and 1	1	1
Bypass decimation	Custom filter (user programmablecoefficients)				0 and 1	1	1

The choice of the odd/even tap setting, filter coefficient set and the filter rate uniquely determines the filter to be used. In addition to the preset filter coefficients, the coefficients for each of the eight filter channels can be programmed by the user. Each of the eight channels has 12 programmable coefficients, each 12-bit long. The 96 registers with addresses from 5A (Hex) to B9 (Hex) are used to program these 8 sets of 12 programmable coefficients. Registers 5A to 65 are used to program the 1st filter, with the 1st coefficient occupying the bits D11..D0 of register 5A, the 2nd coefficient occupying the bits D11..D0 of register 5B, and so on. Similarly registers 66(Hex) to 71(Hex) are used to program the 2nd filter, and so on.

When programming the filter coefficients, the D15 bit of each of the 12 registers corresponding to that filter should be set to '1'. If the D15 bit of these 12 registers is set to '0', then the preset coefficient (as programmed by FILTERn_COEFF_SET<2:0>) is used even if the bits D11..D0 get programmed. By setting or not setting the D15 bits of individual filter channels to '1', some filters can be made to operate with preset coefficient sets, and some others can be made to simultaneously operate with programmed coefficient sets.

HIGH PASS FILTER

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
2E			X	X	X	X											HPF_corner_CH1
2E		X															HPF_EN_CH1
2F			X	X	X	X											HPF_corner_CH2
2F		X															HPF_EN_CH2
30			X	X	X	X											HPF_corner_CH3
30		X															HPF_EN_CH3
31			X	X	X	X											HPF_corner_CH4
31		X															HPF_EN_CH4
32			X	X	X	X											HPF_corner_CH5
32		X															HPF_EN_CH5
33			X	X	X	X											HPF_corner_CH6
33		X															HPF_EN_CH6
34			X	X	X	X											HPF_corner_CH7
34		X															HPF_EN_CH7
35			X	X	X	X											HPF_corner_CH8
35		X															HPF_EN_CH8

This group of registers controls the characteristics of a digital high pass transfer function applied to the output data, useing Equation 3:

$$y(n) = \frac{2^k}{2^k+1}[x(n) - x(n-1) + y(n-1)] \quad (3)$$

Where k is set as described by the HPF_corner registers (one for each channel). Also the HPF_EN bit in each register needs to be set to enable the HPF feature for each channel.

BIT CLOCK PROGRAMMABILITY

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
42										X	X						PHASE_DDR<1:0>
46	1											X					EN_SDR
46	1		X														FALL_SDR

The output interface of the ADS5292 is normally a DDR interface, with the LCLK rising edge and falling edge transitions in the middle of alternate data windows. This default phase is shown in Figure 51.

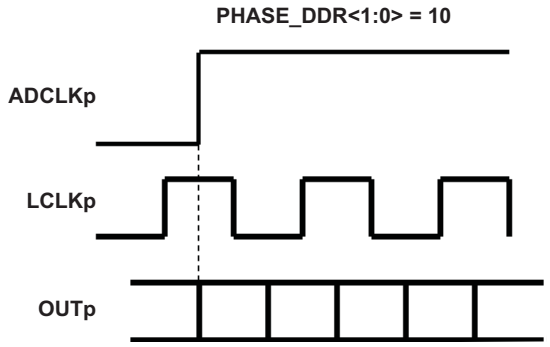


Figure 51. Default Phase of LCLK

The phase of LCLK can be programmed relative to the output frame clock and data using bits PHASE_DDR<1:0>. The LCLK phase modes are shown in Figure 52.

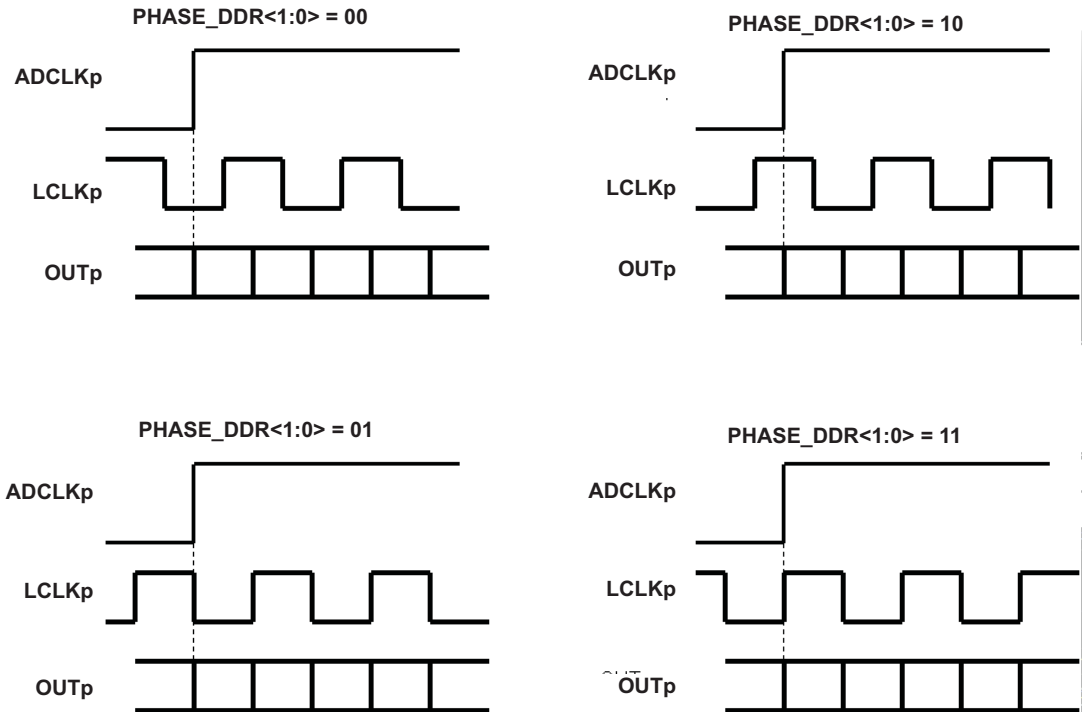


Figure 52. Phase Programmability Modes for LCLK

In addition to programming the phase of the LCLK in the DDR mode, the device can also be made to operate in SDR mode by setting bit EN_SDR to 1. In the mode, the bit clock (LCLK) is output at 14X times the input clock, or twice the rate as in DDR mode. Depending on the state of FALL_SDR, the LCLK may be output in either of the two manners shown in Figure 53. As can be seen in Figure 53, only the LCLK rising (or falling edge) is used to capture the output data in SDR mode. The SDR mode does not work well beyond 40 MSPS because the LCLK frequency will become very high.

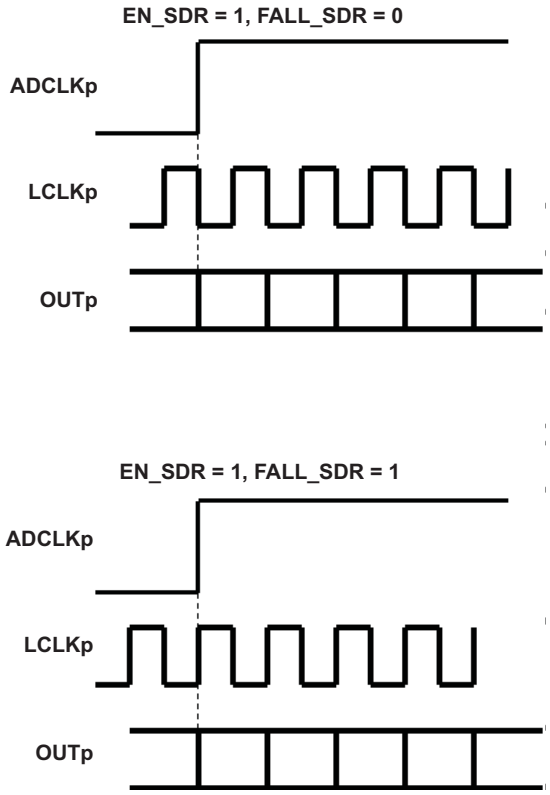


Figure 53. SDR Interface Modes

OUTPUT DATA RATE CONTROL

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
38															DATA_RATE<1>	DATA_RATE<0>

In the default mode of operation, the data rate at the output of the ADS5292 is at the sampling rate of the ADC. This is true even when the custom pattern generator is enabled. In addition, both output data rate and sampling rate can also be configured to a sub-multiple of the input clock rate.

With the DATA_RATE<1:0> control, the output data rate can be programmed to be a sub-multiple of the ADC sampling rate. This feature can be used to lower the output data rate, for example when the decimation filter is used. Without enabling the decimation filter, the sub-multiple ADC sampling rate feature still can be used.

The different settings are listed below:

DATA_RATE<1>	DATA_RATE<0>	Output data rate
0	0	Same as ADC sampling rate
0	1	1/2 of ADC sampling rate
1	0	1/4 of ADC sampling rate
1	1	1/8 of ADC sampling rate

SYNCHRONIZATION PULSE

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
25	TP_HARD_SYNC															
02			EN_SYNC													

The SYNC pin can be used to synchronize the data output from channels within the same chip or from channels across chips when decimation filters are used with reduced output data rate.

When the decimation filters are used (for example, the decimate by two filter is enabled), then, effectively, the device outputs one digital code for every two analog input samples. If the SYNC function is not enabled, then the filters are not synchronized (even within a chip) – this means that one channel may be sending out codes corresponding to input samples N, N+1 and so on, while another may be sending out code corresponding to N+1, N+2 and so on.

To achieve synchronization, the SYNC pulse must arrive at all the ADS529x chips at the same time instant (as shown in the timing diagram of Figure 54

The ADS5292 generates an internal synchronization signal which is used to reset the internal clock dividers used by the decimation filter.

Using the SYNC signal in this way ensures that all channels will output digital codes corresponding to the same set of input samples.

SYNC Timings:

Synchronizing the filters using the SYNC pin is enabled by default. No register bits are required to be written. Even EN_SYNC bit is not required.It is important for register bit TP_HARD_SYNC to be0 for this mode to work. As shown by Figure 54, the SYNC rising edge can be positioned anywhere within the window. The width of the SYNC must be at least one clock cycle.

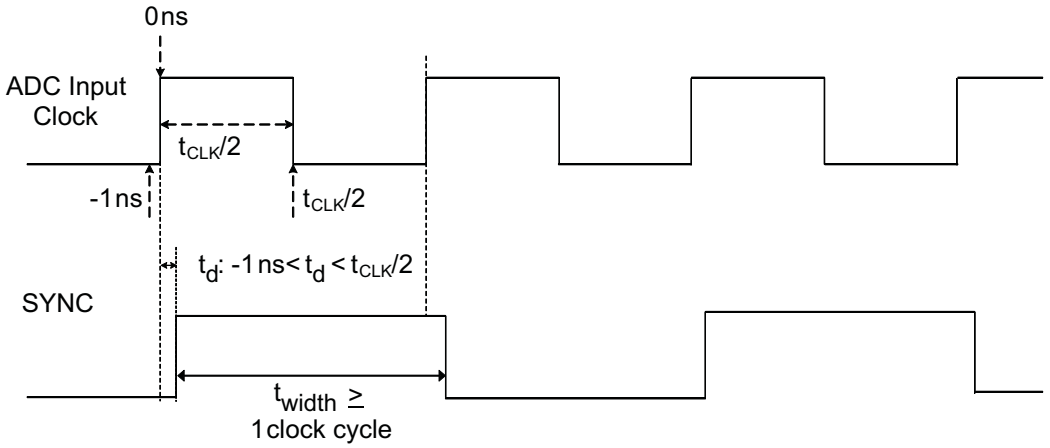


Figure 54. Synchronization Pulse Timing

Note that the SYNC DOES NOT synchronize the sampling instants of the ADC across chips. All channels within a single chip sample their analog inputs simultaneously. To ensure that channels across two chips will sample their analog inputs simultaneously, the input clock needs to be routed to both chips with identical length. This ensuring that the input clocks arrive at both the chips at the same time. This needs to be taken care of in the board design and routing. The SYNC pin cannot be used to synchronize the sampling instants.

In addition to the above, the SYNC can also be used to synchronize the RAMP test patterns across channels. In order to synchronize the test patterns, TP_HARD_SYNC must be set as 1. Setting TP_HARD_SYNC =1 actually disables the sync of the filters.

External Reference Mode of Operation

The ADS5292 supports an external reference mode of operation in one of two ways:

a. By forcing the reference voltages on the REFT and REFB pins.
b. By applying the reference voltage on VCM pin.

This mode can be used to operate multiple ADS5292 chips with the same (externally applied) reference voltage.

Using the REF pins:

For normal operation, the device requires two reference voltages, REFT and REFB. By default, the device generates these two voltages internally. To enable the external reference mode, set the register bits as shown in Table 6 . This powers down the internal reference amplifier and the two reference voltages can be forced directly on the REFT and REFB pins as VREFT = 1.45 V ± 50 mV and VREFB = 0.45 V ±50 mV.

Note that the relation between the ADC full-scale input voltage and the applied reference voltages is

Full-scale input voltage = 2 x (VREFT – VREFB) (4)

Using the VCM pin:

In this mode, an external reference voltage VREFIN can be applied to the VCM pin such that

Full-scale input voltage = 2 x VREFIN (5)

To enable this mode, set the register bits as shown in Table 6. This changes the function of the VCM pin to an external reference input pin. The voltage applied on VCM must be 1.5V ±50mV.

Table 6. External reference function

Function	EN_HIGH_ADDRS	EN_EXT_REF	EXT_REF_VCM
External reference using REFT/REFB pins	1	1	00
External reference using VCM pin	1	1	11

DATA OUTPUT FORMAT MODES

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
46	1													X			BTC_MODE
46	1												X				MSB_FIRST

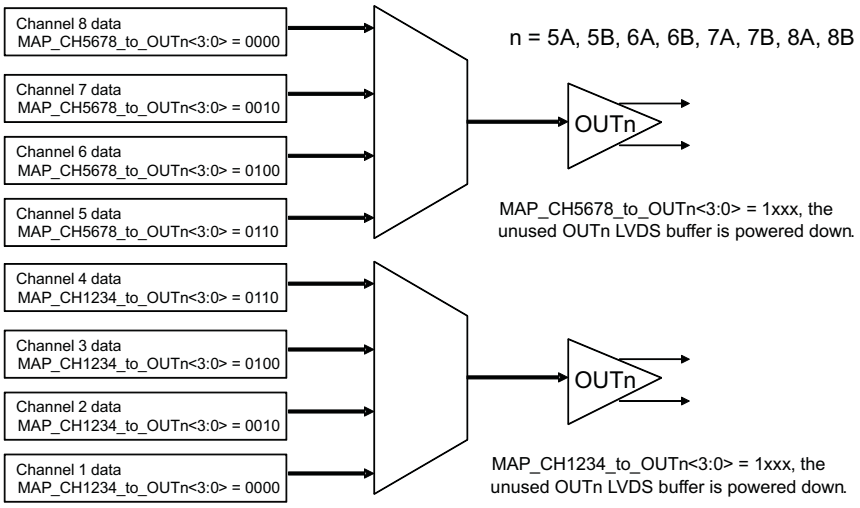
The ADC output, by default, is in Straight offset binary mode. Programming the BTC_MODE bit to '1' inverts the MSB, and the output becomes Binary 2's complement mode. Also, by default, the first bit of the frame (following the rising edge of CLKP) is the LSB of the ADC output. Programming the MSB_FIRST mode inverts the bit order in the word, and the MSB is output as the first bit following CLKP rising edge.

PROGRAMMABLE MAPPING BETWEEN INPUT CHANNELS AND OUTPUT PINS

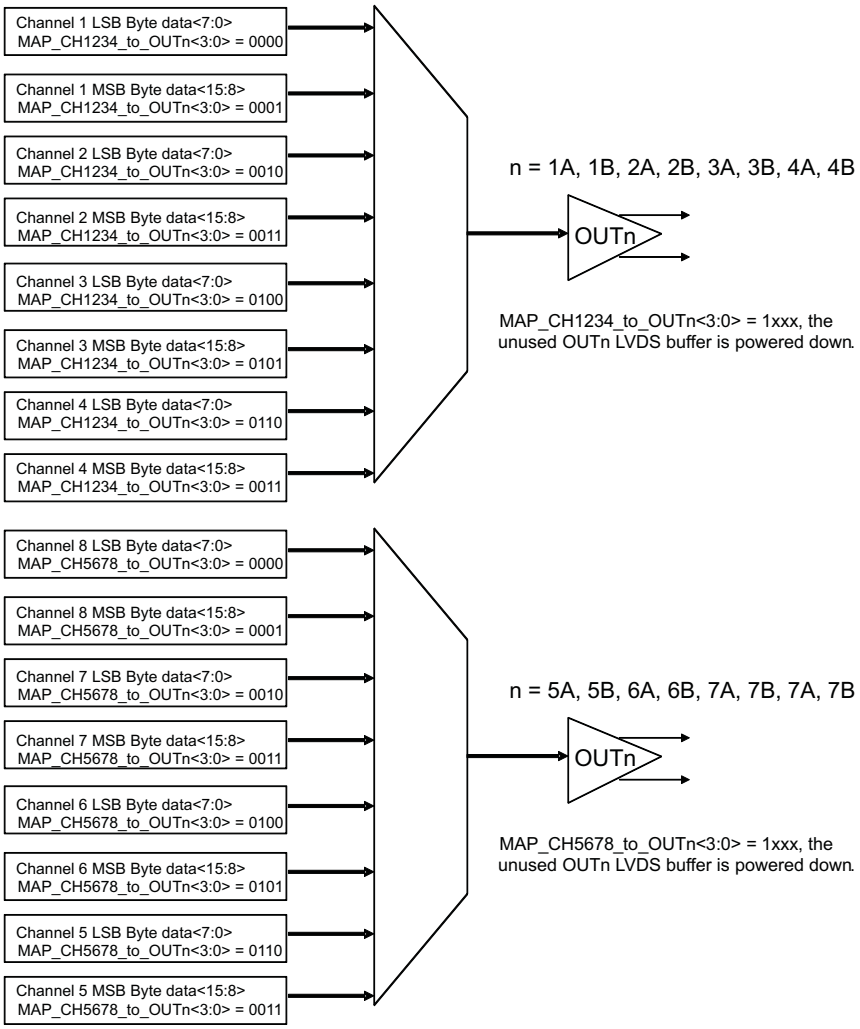
ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
50	1												X	X	X	X	MAP_CH1234_TO_OUT1A
	1								X	X	X	X					MAP_CH1234_TO_OUT1B
	1				X	X	X	X									MAP_CH1234_TO_OUT2A
51	1												X	X	X	X	MAP_CH1234_TO_OUT2B
	1								X	X	X	X					MAP_CH1234_TO_OUT3A
	1				X	X	X	X									MAP_CH1234_TO_OUT3B
52	1												X	X	X	X	MAP_CH1234_TO_OUT4A
	1								X	X	X	X					MAP_CH1234_TO_OUT4B
53	1												X	X	X	X	MAP_CH5678_TO_OUT5B
	1								X	X	X	X					MAP_CH5678_TO_OUT5A
	1				X	X	X	X									MAP_CH5678_TO_OUT6B
54	1												X	X	X	X	MAP_CH5678_TO_OUT6A
	1								X	X	X	X					MAP_CH5678_TO_OUT7B
	1				X	X	X	X									MAP_CH5678_TO_OUT7A
55	1												X	X	X	X	MAP_CH5678_TO_OUT8B
	1								X	X	X	X					MAP_CH5678_TO_OUT8A

The ADS5292 has 16 pairs of LVDS channel outputs. The mapping of ADC channels to LVDS output channels is programmable to allow for flexibility in board layout. The 16 LVDS channel outputs are split in to 2 groups of 8 LVDS pairs. Within each group 4 ADC input channels can be multiplexed in to the 8 LVDS pairs depending on the modes of operation whether it is 1 wire mode or 2 wire mode.

Input channels 1 to 4 can be mapped to any of the LVDS outputs OUT1A/B to OUT4A/B (using the MAP_CH1234_TO_OUTnA/B). Similarly, input channels 5 to 8 can be mapped to any of the LVDS outputs OUT5A/B to OUT8A/B (using the MAP_CH5678_TO_OUTnA/B). The block diagram of the mapping is listed in Figure 55.



(a) 1-wire mode



(b) 2-wire mode

Figure 55. Input and Output Channel Mapping

Registers 0x50 to 0x55 control the multiplexing options as below:

MAP_CH1234_to_OUTn<3:0>	Mapping	Used in 1-wire mode?	Used in 2-wire mode?
0000	ADC input channel IN1 to OUTn	Y	Y, for LSB byte
0001	ADC input channel IN1 to OUTn (2-wire only)	N	Y, for MSB byte
0010	ADC input channel IN2 to OUTn	Y	Y, for LSB byte
0011	ADC input channel IN2 to OUTn (2-wire only)	N	Y, for MSB byte
0100	ADC input channel IN3 to OUTn	Y	Y, for LSB byte
0101	ADC input channel IN3 to OUTn (2-wire only)	N	Y, for MSB byte
0110	ADC input channel IN4 to OUTn	Y	Y, for LSB byte
0111	ADC input channel IN4 to OUTn (2-wire only)	N	Y, for MSB byte
1xxx	LVDS output buffer OUTn is powered down		

MAP_CH5678_to_OUTn<3:0>	Mapping	Used in 1-wire mode?	Used in 2-wire mode?
0000	ADC input channel IN8 to OUTn	Y	Y, for LSB byte
0001	ADC input channel IN8 to OUTn (2-wire only)	N	Y, for MSB byte
0010	ADC input channel IN7 to OUTn	Y	Y, for LSB byte
0011	ADC input channel IN7 to OUTn (2-wire only)	N	Y, for MSB byte
0100	ADC input channel IN6 to OUTn	Y	Y, for LSB byte
0101	ADC input channel IN6 to OUTn (2-wire only)	N	Y, for MSB byte
0110	ADC input channel IN5 to OUTn	Y	Y, for LSB byte
0111	ADC input channel IN5 to OUTn (2-wire only)	N	Y, for MSB byte
1xxx	LVDS output buffer OUTn is powered down		

The default mapping for 1-wire and 2-wire modes is:

Table 7. Mapping for 1-wire Mode

Analog Input channel	LVDS Output
Channel IN1	OUT1A
Channel IN2	OUT2A
Channel IN3	OUT3A
Channel IN4	OUT4A
Channel IN5	OUT5A
Channel IN6	OUT6A
Channel IN7	OUT7A
Channel IN8	OUT8A
Note: In the single wire mode, with default register settings, ADC data is available only on OUTnA.	

Table 8. Mapping for 2-wire Mode

Analog Input channel	LVDS Output
Channel IN1	OUT1A, OUT1B
Channel IN2	OUT2A, OUT2B
Channel IN3	OUT3A, OUT3B
Channel IN4	OUT4A, OUT4B
Channel IN5	OUT5A, OUT5B
Channel IN6	OUT6A, OUT6B
Channel IN7	OUT7A, OUT7B
Channel IN8	OUT8A, OUT8B
Note: In the 2-wire mode, the ADC data is available on both OUTnA and OUTnB.	

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5292 is an octal channel, 12-bit high-speed ADC with sample rate up to 80 MSPS that runs off a single 1.8 V supply. All eight channels of the ADS5292 simultaneously sample their analog inputs at the rising edge of the input clock. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock, edge the sample propagates through the pipeline resulting in a data latency of 11 clock cycles.

The 14 data bits of each channel are serialized and sent out in either 1-wire (one pair of LVDS pins are used) or 2-wire (two pairs of LVDS pins are used) mode, depending on the LVDS output rate. When the data is output in the 2-wire mode, it can reduce the serial data rate of the outputs, especially at higher sampling rates. Hence, low cost FPGAs can be used to capture 80 MSPS/12bit data. Alternately, at lower sample rates, the 12-bit data can be output as a single data stream over one pair of LVDS pins (1-wire mode). The device outputs a bit clock at 7x and frame clock at 1x times the sample frequency in the 12-bit mode.

This 12-bit ADC achieves 70 dBFS SNR at 80MSPS. Its output resolution can be configured as 14-bit and 10-bit if necessary. 72 dBFS and 61 dBFS SNRs are achieved when the ADS5292's output resolution is 12-bit and 10-bit respectively.

ANALOG INPUT

The analog inputs consist of a switched-capacitor based, differential sample and hold architecture. This differential topology results in very good AC performance even for high input frequencies at high sampling rates. The INP and INM pins are internally biased around a common-mode voltage of Vcm (0.95 V). For a full-scale differential input, each input pin (INP and INM) must swing symmetrically between Vcm + 0.5V and Vcm - 0.5V, resulting in a 2 V_{PP} differential input swing. Figure 56 illustrates the equivalent circuit of the input sampling circuit.

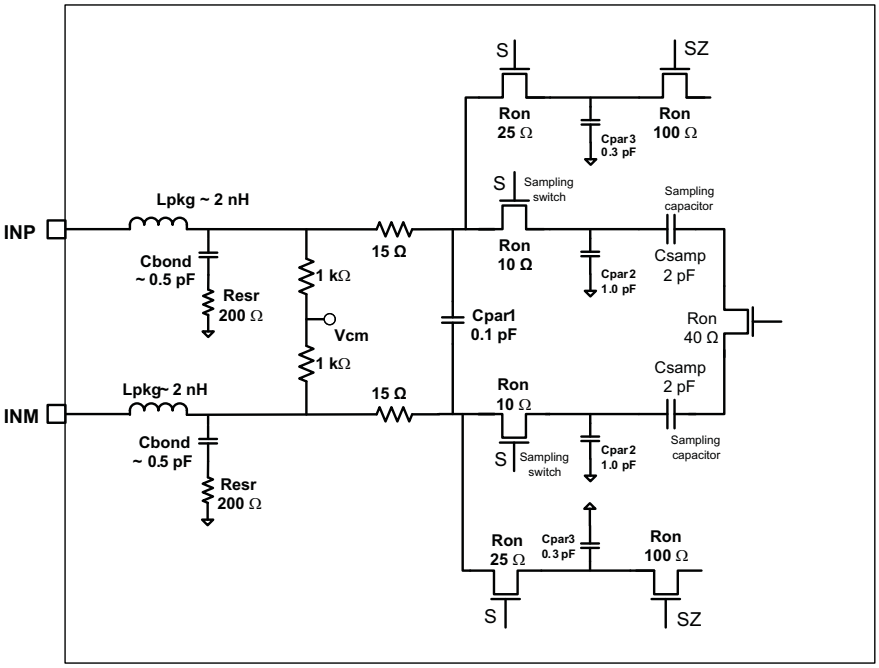


Figure 56. Analog Input Circuit Model

DRIVE CIRCUIT

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection. A 5 Ω to 15 Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitic.

The drive circuit shows an R-C filter across the analog input pins. The purpose of the filter is to absorb the glitches caused by the opening and closing of the sampling capacitors.

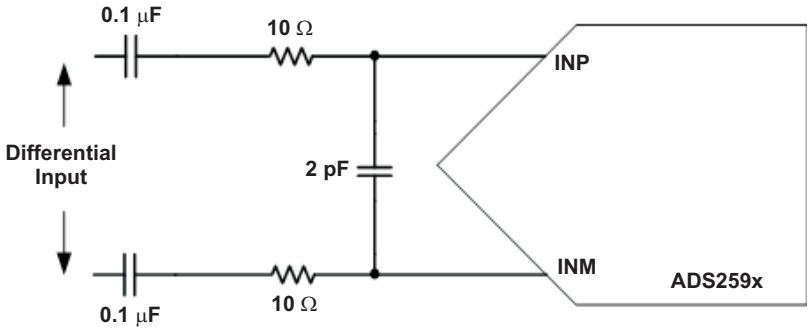


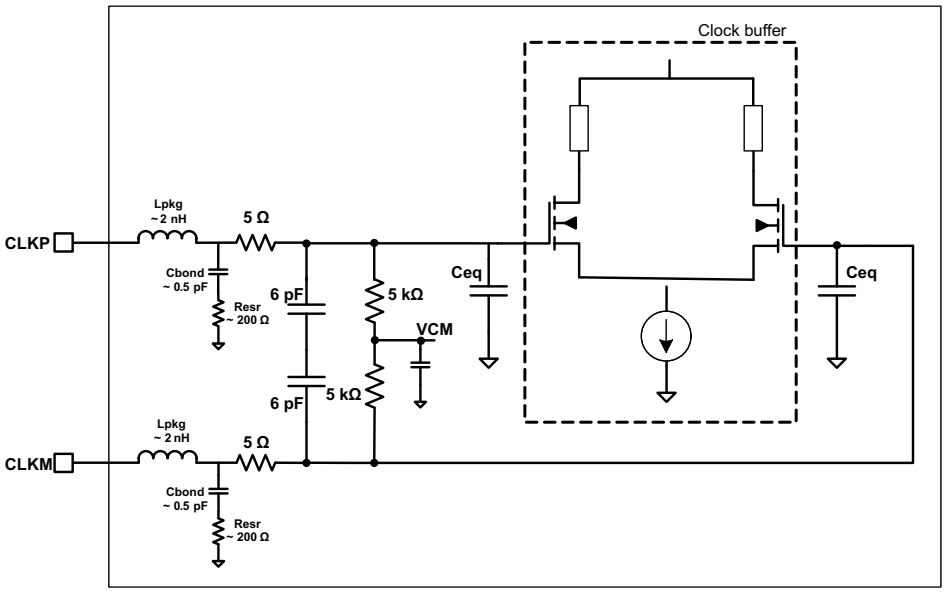
Figure 57. Drive Circuit

Large and Small Signal Input Bandwidth

The small signal bandwidth of the analog input circuit is high, around 550 MHz. When using an amplifier to drive the ADS5292, the total noise of the amplifier up to the small signal bandwidth must be considered. The large signal bandwidth of the device depends on the amplitude of the input signal. The ADS5292 supports 2 VPP amplitude for input signal frequency up to 80 MHz. For higher frequencies (80 MHz), the amplitude of the input signal must be decreased proportionally. For example, at 160 MHz, the device supports a maximum of 1 VPP signal.

INPUT CLOCK

The ADS5292 is configured by default to operate with a single-ended input clock – CLKP is driven by a CMOS clock and CLKM is tied to GND. The device can automatically detect a single-ended or differential clock. If CLKM is grounded, the device treats clock as a single-ended clock. Operating with a low-jitter differential clock usually gives better SNR performance, especially at input frequencies greater than 30 MHz. Typical clock termination structures are listed in Figure 58 and Figure 59.



Ceq is approximately 1 to 3 pF, equivalent input capacitance of clock buffer.

Figure 58. Equivalent Circut of the Input Clock Circuit

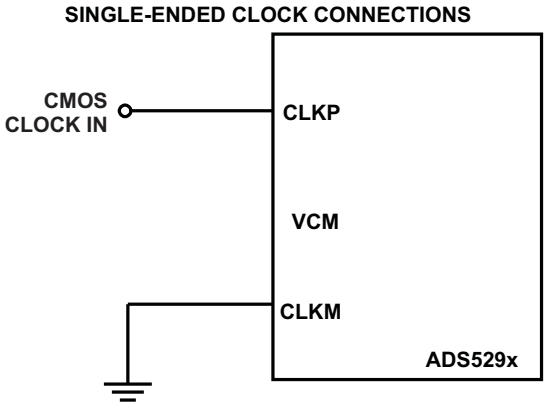
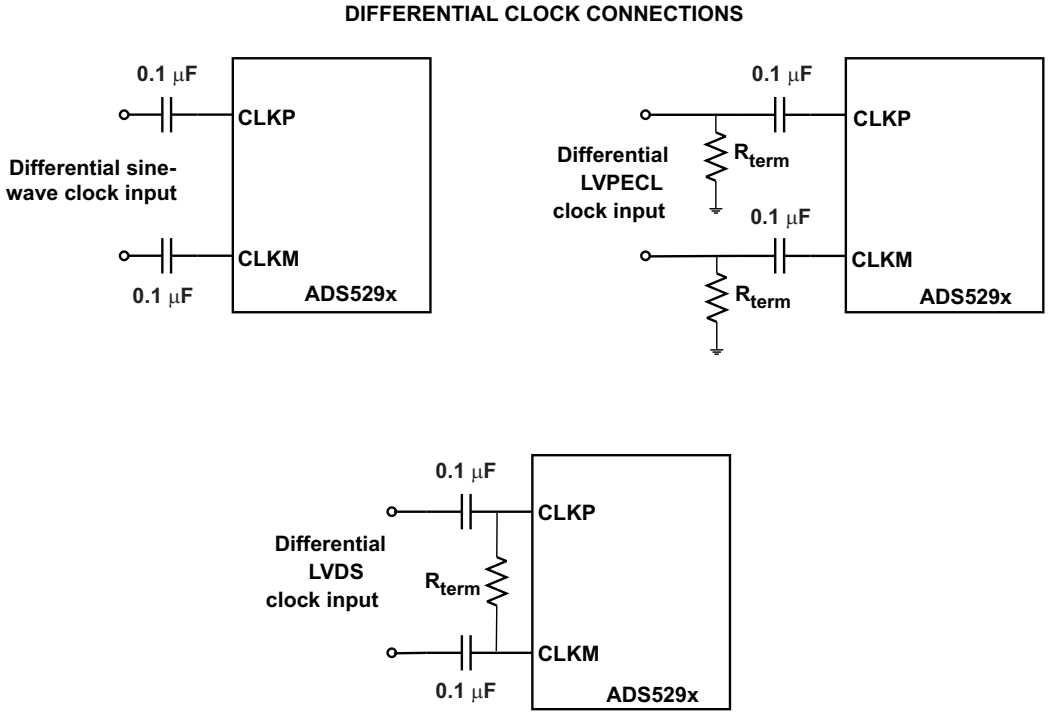


Figure 59. Drive Circuit

DIFFERENTIAL CLOCK CONNECTIONS



DIGITAL HIGH PASS IIR FILTER

DC offset is often observed at ADC input signals. For example, in ultrasound applications, the DC offset from VGA (variable Gain amplifier) varies at different gains. Such a variable offset can introduce artifacts in ultrasound images especially in Doppler modes. Analog filter between ADC and VGA can be used with added noise and power. Digital filter achieves the same performance as analog filters and has more flexibility in fine tuning multiple characteristics.

ADS5292 includes optional 1st order digital high-pass IIR filter. Its block diagram is shown in Figure 60 as well as its transfer function

$$y(n) = \frac{2^k}{2^k+1}[x(n) - x(n-1) + y(n-1)] \quad (6)$$

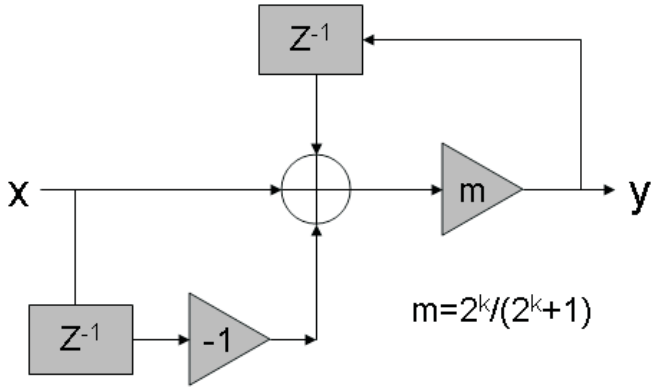


Figure 60. HP Filter Block Diagram

Figure 61 shows its characteristics at K = 2 to 10.

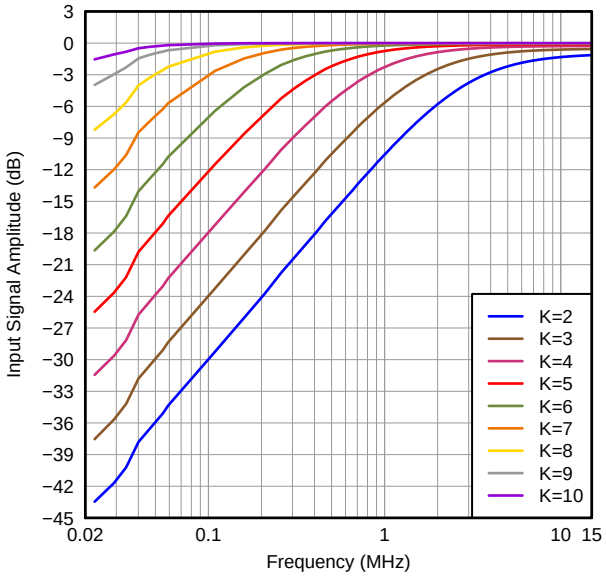


Figure 61. HP Filter Amplitude Response at K = 2 to 10

DECIMATION FILTER

ADS5292 includes an option to decimate the ADC output data using filters. Once the decimation is enabled, the decimation rate, frequency band of the filter can be programmed. In addition, the user can select either the pre-defined or custom coefficients.

Table 9. Digital Filters

DECIMATION	TYPE OF FILTER	<DATA RATE>	FILTERn RATE>	<FILTERn COEFF SET>	<ODD TAP>	<USE FILTER CHn>	<EN CUSTOM FILT>
Decimate by 2	Built-in **low-pass odd-tap** filter (pass band = 0 to $f_S/4$)	001	000	000	1	1	0
	Built-in **high-pass odd-tap** filter (pass band = 0 to $f_S/4$)	001	000	001	1	1	0
Decimate by 4	Built-in **low-pass even-tap** filter (pass band = 0 to $f_S/8$)	010	001	010	0	1	0
	Built-in first **band pass even tap** filter(pass band = $f_S/8$ to $f_S/4$)	010	001	011	0	1	0
	Built-in second **band pass even tap** filter(pass band = $f_S/4$ to 3 $f_S/8$)	010	001	100	0	1	0
	Built-in **high pass odd tap** filter (pass band = 3 $f_S/8$ to $f_S/2$)	010	001	101	1	1	0
Decimate by 2	Custom filter (user programmablecoefficients)	001	000	000	0 and 1	1	1
Decimate by 4	Custom filter (user programmablecoefficients)	010	001	000	0 and 1	1	1
Decimate by 8	Custom filter (user programmablecoefficients)	011	100	000	0 and 1	1	1
Bypass decimation	Custom filter (user programmablecoefficients)				0 and 1	1	1

DECIMATION FILTER EQUATION

In the default setting, the decimation filter is implemented as a 24-tap FIR filter with symmetrical coefficients (each coefficient is 12-bit signed). By setting the register bit **<ODD TAPn>** = 1, a 23-tap FIR is implemented

Predefined Coefficients

The built-in filters (low-pass, high-pass and band-pass) use predefined coefficients. The frequency responses of the built-in decimation filters with different decimation factors are shown in Figure 62 and Figure 63.

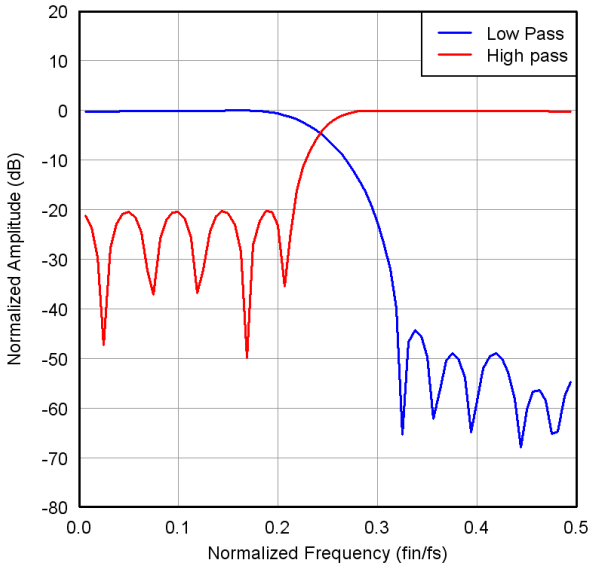


Figure 62. Filter Response, Decimate by 2

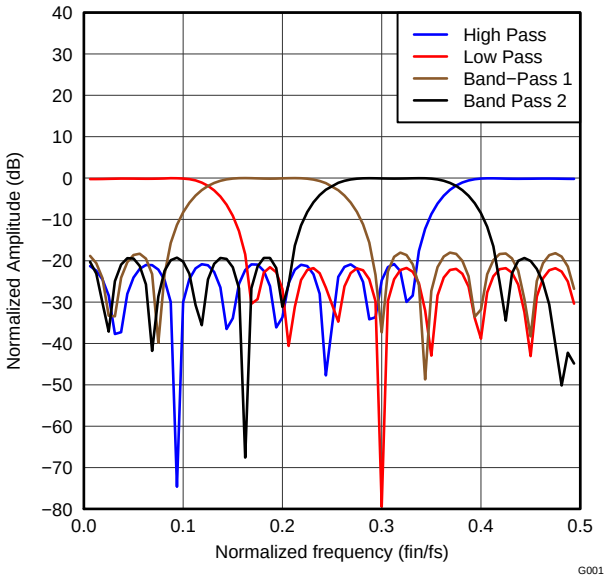


Figure 63. Filter Response, Decimate by 4

Custom Filter Coefficients

The filter coefficients can also be programmed by the user (customized). For custom coefficients, set the register bit **<FILTER COEFF SELECT>** and load the coefficients (h_0 to h_{11}) in registers 0x5A to 0xB9, using the serial interface as:

Register content = real coefficient value x 211, i.e., 12 bit signed representation of real coefficient.

Board Design Considerations

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See *ADS5292EVM Evaluation Module* (SLAU355) for placement of components, routing and grounding.

Supply Decoupling

Because the ADS5292 already includes internal decoupling, minimal external decoupling can be used without loss in performance. For example, the ADS5292EVM uses a single 0.1 µF decoupling capacitor for each supply, placed close to the device supply pins.

Packaging

Exposed Pad

The exposed pad at the bottom of the package is the main path for heat dissipation. Therefore, the pad must be soldered to a ground plane on the PCB for best thermal performance. The pad must be connected to the ground plane through the optimum number of vias.

Also, visit TI's thermal website at www.ti.com/thermal.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 - 0.5/100) \times FS_{ideal}$ to $(1 + 0.5/100) \times FS_{ideal}$.

Offset Error – The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} – T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (7)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (8)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB) – ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \tag{9}$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$\text{THD} = 10\text{Log}^{10}\ \frac{P_S}{P_N} \tag{10}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR) – DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

AC Power-Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$\text{PSRR} = 20\text{Log}^{10}\ \frac{\Delta V_{OUT}}{\Delta V_{SUP}}\ \text{(Expressed in dBc)} \tag{11}$$

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

$$\text{CMRR} = 20\text{Log}^{10}\ \frac{\Delta V_{OUT}}{\Delta V_{CM}}\ \text{(Expressed in dBc)} \tag{12}$$

Crosstalk (only for multi-channel ADCs) – This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

REVISION HISTORY

Changes from Original (November 2011) to Revision A **Page**

- Changed the document From: Product Preview To: Production 1

Changes from Original (November 2011) to Revision B **Page**

- Changed the description of the SYNC pin 4
- Changed the location of OUT A and OUT B in Figure 5 and Figure 6 14
- Added EN_HIGH_ADDRS to Table 3 29
- Moved EN_EXT_REF From: 0x0F To: 0xF0 in Table 3 34
- Added the section BIT-BYTE-WORD WISE OUTPUT. Added Figure 47 and Figure 48. 37
- Added section DIGITAL PROCESSING BLOCKS 38
- Replaced Table 5 and Table 6 with new Table 5 - Digital Filters 43
- Changed the SYNCHRONIZATION PULSE section 46
- Added the External Reference Mode of Operation section 47
- Added Figure 58 53
- Replaced Table 9 (Decimation Filter Modes) with new Table 9 - Digital Filters 56
- Deleted section: Synchronization Pulse 57

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5292IPFP	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5292	Samples
ADS5292IPFPR	ACTIVE	HTQFP	PFP	80	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5292	Samples
ADS5292IPFPT	ACTIVE	HTQFP	PFP	80	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5292	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

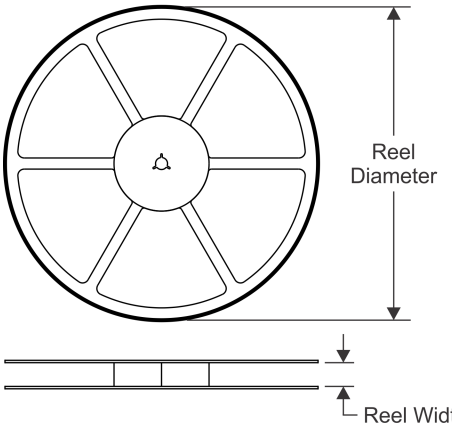
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

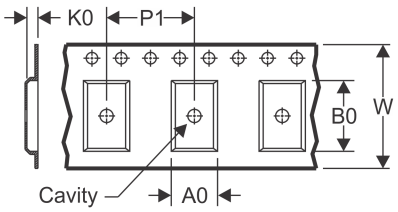
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

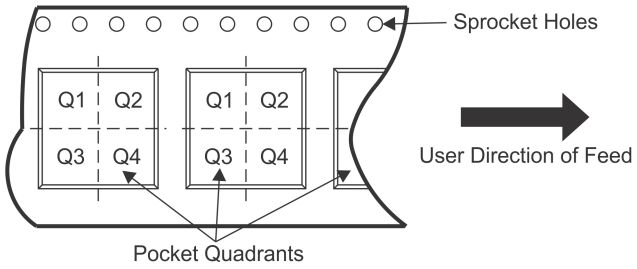


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

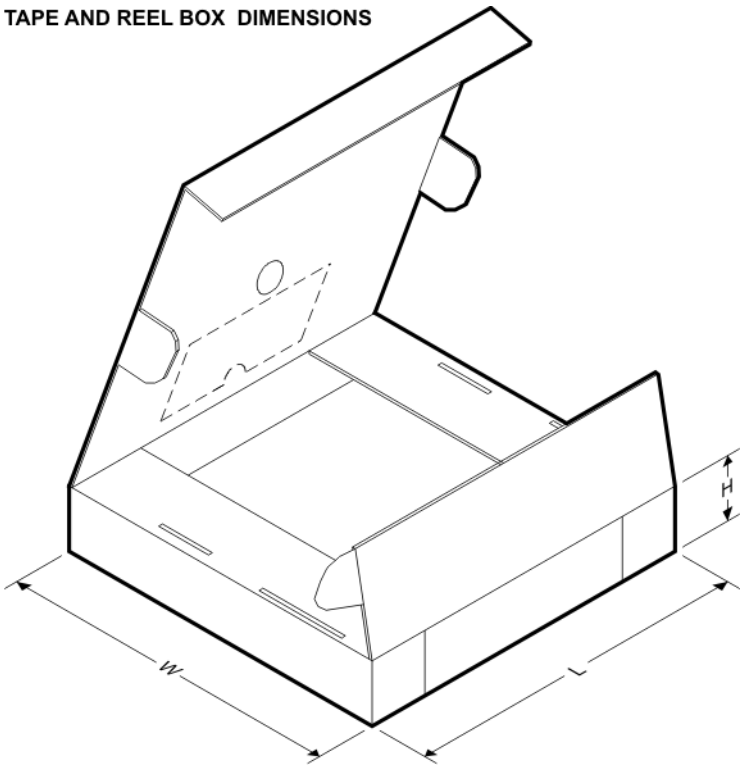
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5292IPFPR	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
ADS5292IPFPT	HTQFP	PFP	80	250	180.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2

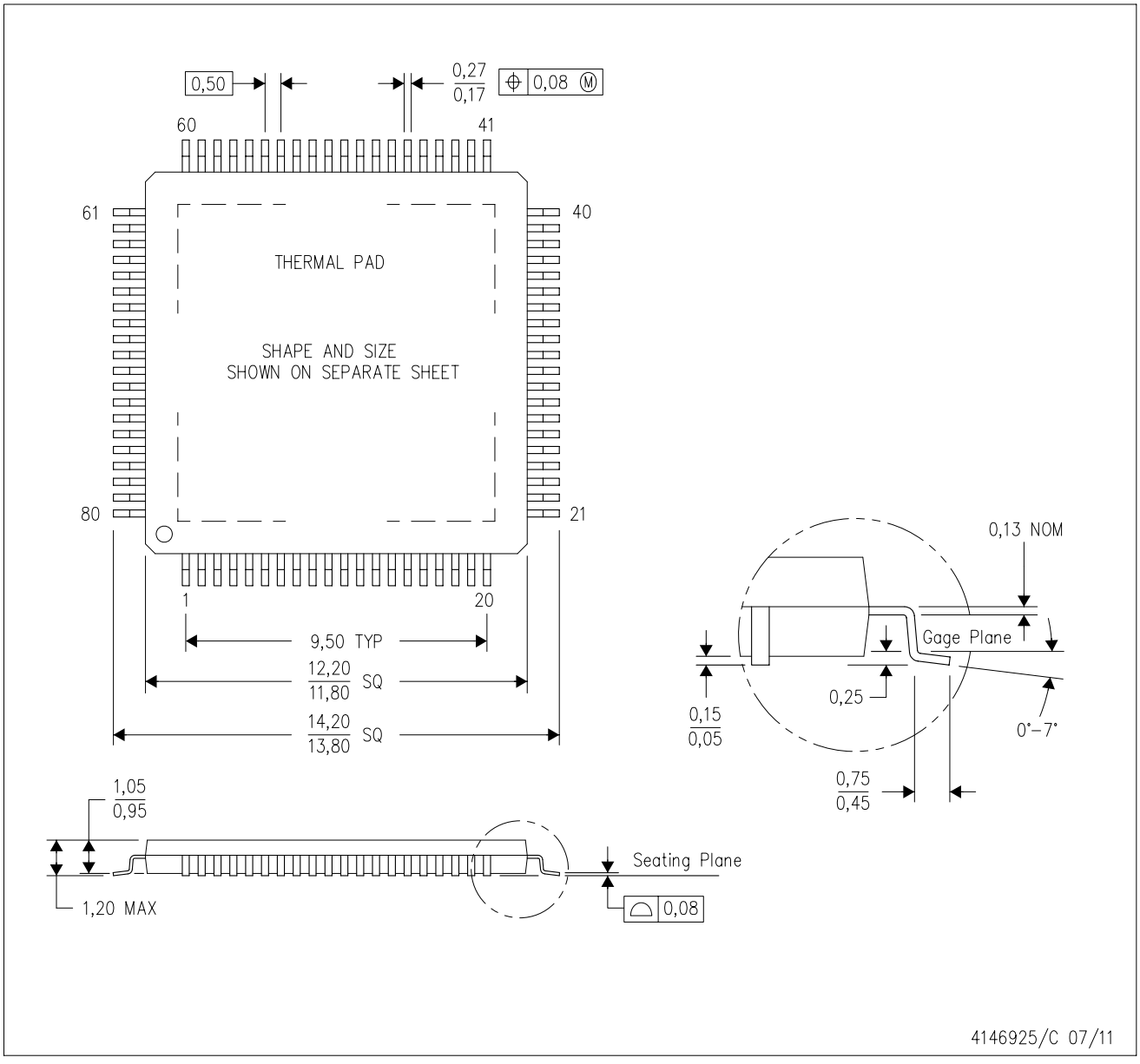
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5292IPFPR	HTQFP	PFP	80	1000	350.0	350.0	43.0
ADS5292IPFPT	HTQFP	PFP	80	250	213.0	191.0	55.0

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

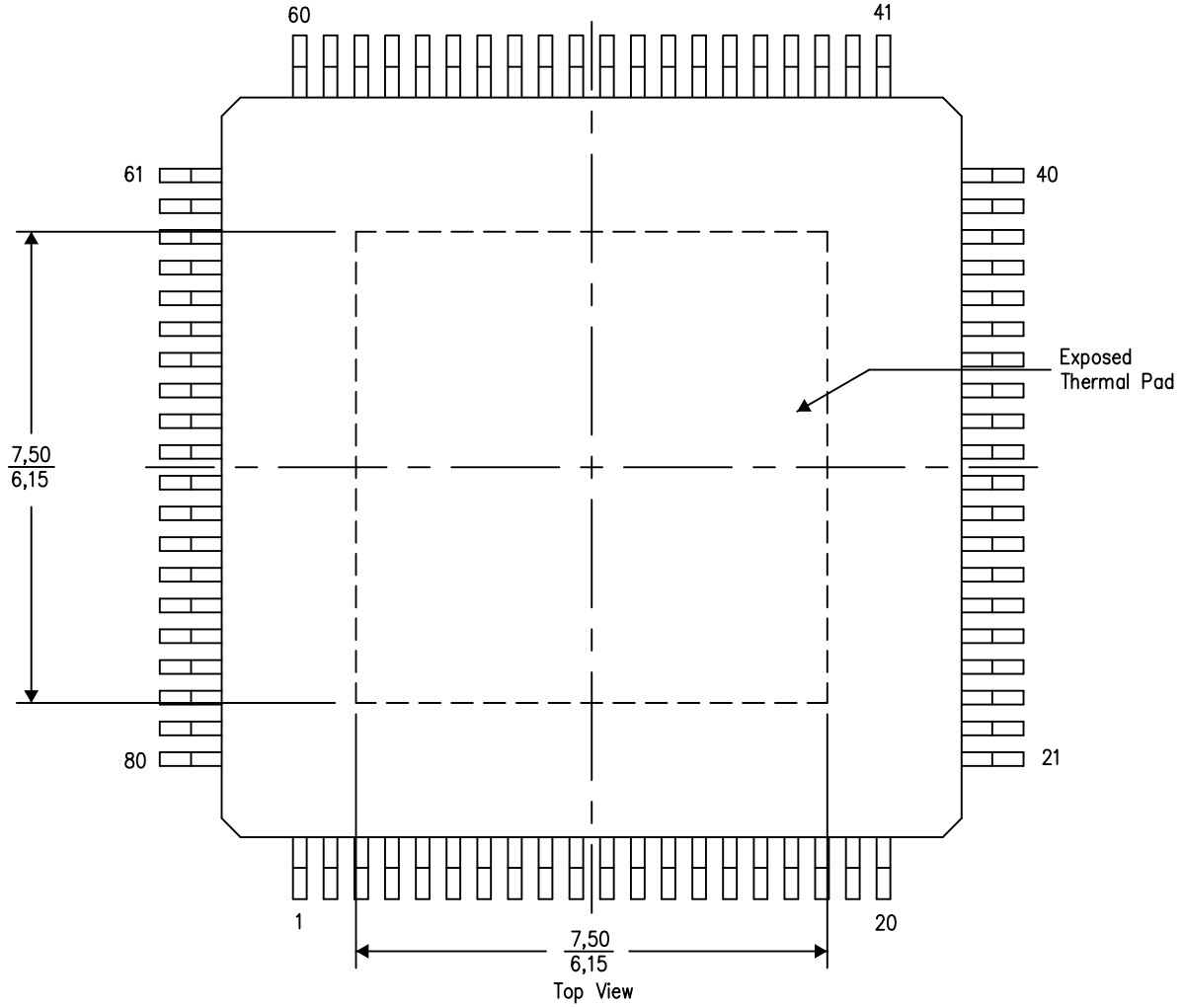
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



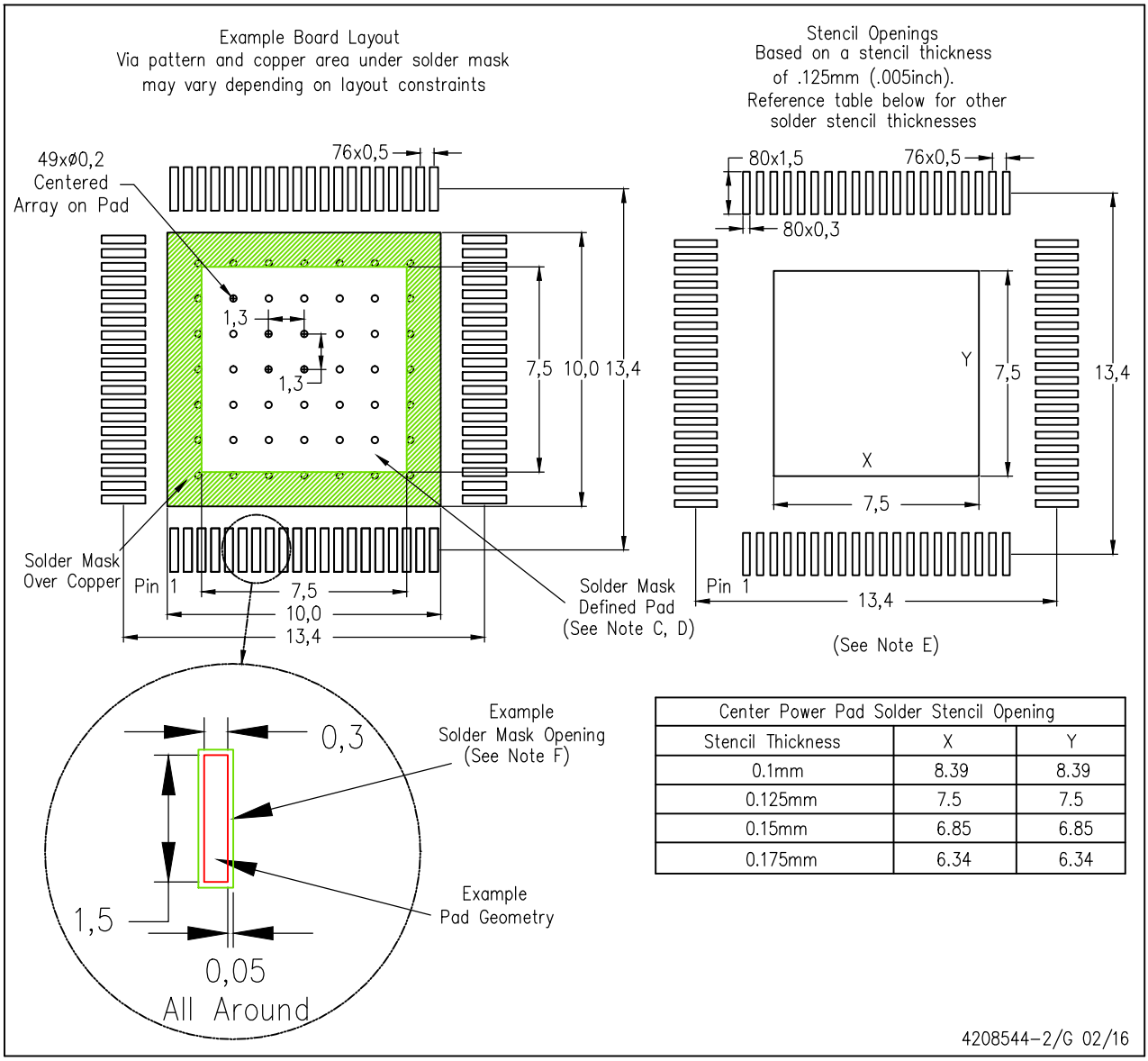
Exposed Thermal Pad Dimensions

4206327–2/P 05/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	8.39	8.39
0.125mm	7.5	7.5
0.15mm	6.85	6.85
0.175mm	6.34	6.34

PowerPAD is a trademark of Texas Instruments.

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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