Octal Ultrasound Analog Front End

Data Sheet **AD9674**

FEATURES

- 8 channels of LNA, VGA, AAF, ADC, and digital RF decimator
  - Low power: 150 mW per channel, TGC mode, 40 MSPS; 62.5 mW per channel, CW mode; <30 mW in power-down
  - Time gain compensation (TGC) channel input referred noise: 0.82 nV/√Hz, maximum gain
  - Flexible power-down modes
  - Fast recovery from low power standby mode: <2 μs
- Low noise preamplifier (LNA)
  - Input referred noise voltage: 0.78 nV/√Hz, gain = 21.6 dB
  - Programmable gain: 15.6 dB/17.9 dB/21.6 dB
  - 0.1 dB compression: 1.00 V p-p/ 0.75 V p-p/0.45 V p-p
  - Flexible active input impedance matching
- Variable gain amplifier (VGA)
  - Attenuator range: 45 dB, linear in dB gain control
  - Postamplifier gain (PGA): 21 dB/24 dB/27 dB/30 dB
- Antialiasing filter (AAF)
  - Programmable second-order low-pass filter (LPF) from 8 MHz to 18 MHz or 13.5 MHz to 30 MHz and high-pass filter (HPF)
- Analog-to-digital converter (ADC)
  - Signal-to-noise ratio (SNR): 75 dB, 14 bits up to 125 MSPS
- Configurable serial low voltage differential signaling (LVDS)
- Continuous wave (CW) Doppler mode harmonic rejection I/Q demodulator
  - Individual programmable phase rotation
  - Dynamic range per channel: >160 dBFS/√Hz
  - Close in SNR: 156 dBc/√Hz, 1 kHz offset, −3 dBFS input
- Radio frequency (RF) digital HPF and decimation by 2
- 10 mm × 10 mm, 144-ball CSP_BGA

APPLICATIONS

- Medical imaging/ultrasound
- Nondestructive Testing (NDT)

GENERAL DESCRIPTION

The AD9674 is designed for low cost, low power, small size, and ease of use for medical ultrasound. It contains eight channels of a VGA with an LNA, a CW harmonic rejection I/Q demodulator with programmable phase rotation, an AAF, an ADC, a digital HPF, and RF decimation by 2.

Each channel features a maximum gain of up to 52 dB, a fully differential signal path, and an active input preamplifier termination. The channel is optimized for high dynamic performance and low power in applications where a small package size is critical.

The LNA has a single-ended to differential gain that is selectable through the serial port interface (SPI). Assuming a 15 MHz noise bandwidth (NBW) and a 21.6 dB LNA gain, the LNA input SNR is 94 dB. In CW Doppler mode, each LNA output drives an I/Q demodulator that has independently programmable phase rotation with 16 phase settings.

Power-down of individual channels is supported to increase battery life for portable applications. Standby mode allows quick power-up for power cycling. In CW Doppler operation, the VGA, AAF, and ADC are powered down. The ADC contains several features designed to maximize flexibility and minimize system cost, such as a programmable clock, data alignment, and programmable digital test pattern generation. The digital test patterns include built in fixed patterns, built in pseudorandom patterns, and custom user defined test patterns entered via the SPI.

Rev. A Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

TABLE OF CONTENTS

REVISION HISTORY

1/16—Revision A: Initial Version

FUNCTIONAL BLOCK DIAGRAM

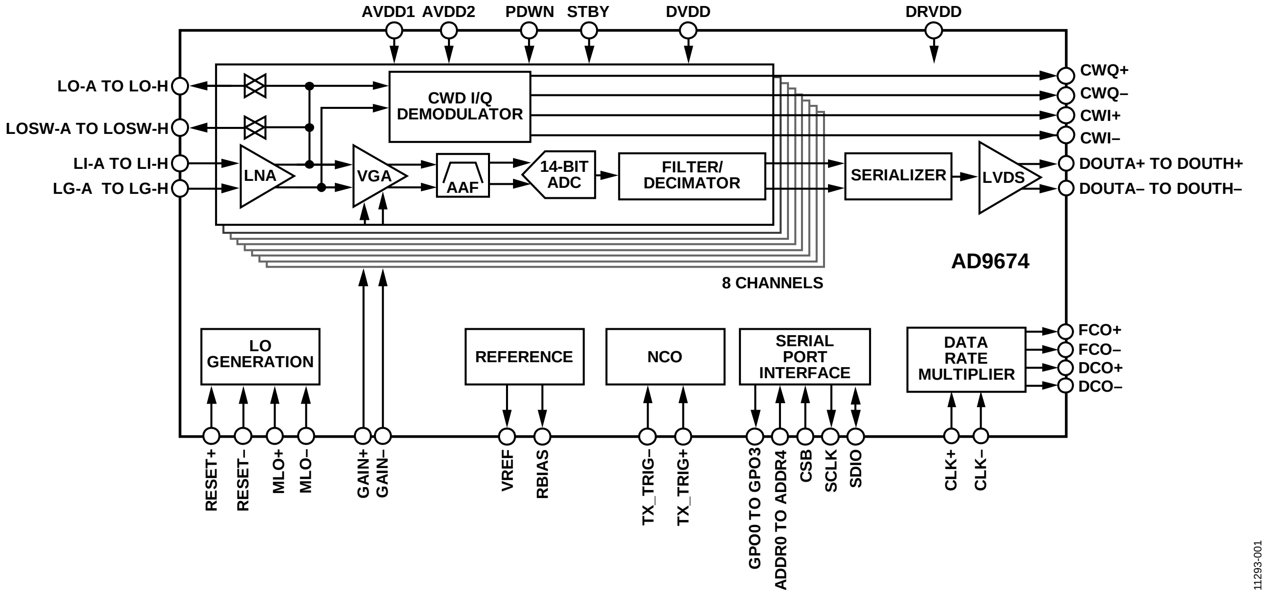

Figure 1.

SPECIFICATIONS

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DVDD = 1.4 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, full temperature range (0°C to 85°C), f_{IN} = 5 MHz, local oscillator (LO) band mode, R_S = 50 Ω, R_{FB} = ∞ (unterminated), LNA gain = 21.6 dB, LNA bias = midhigh, programmable gain amplifier (PGA) gain = 27 dB, analog gain control, V_{GAIN} = (GAIN+) − (GAIN−) = 1.6 V, AAF LPF cutoff = f_{SAMPLE}/3 in Mode I[1]/Mode II,[1] AAF LPF cutoff = f_{SAMPLE}/4.5 in Mode III[1]/Mode IV,[1] HPF cutoff = LPF cutoff/12.00, Mode I[1] = f_{SAMPLE} = 40 MSPS, Mode II[1] = f_{SAMPLE} = 65 MSPS, Mode III[1] = f_{SAMPLE} = 80 MSPS, Mode IV[1] = f_{SAMPLE} = 125 MSPS, RF decimator bypassed, digital filter bypassed, and low power LVDS mode, unless otherwise noted. All gain setting options are listed, which can be configured via SPI registers, and all power supply currents and power dissipations are listed for the four mode settings (Mode I, Mode II, Mode III, and Mode IV).[1]

Table 1.

Parameter[2]	Test Conditions/Comments	Min	Typ	Max	Unit
LNA CHARACTERISTICS					
Gain	Single-ended input to differential output		15.6/17.9/21.6[3]		dB
	Single-ended input to single-ended output		9.6/11.9/15.6[3]		dB
0.1 dB Input Compression Point	LNA gain = 15.6 dB		1.00		V p-p
	LNA gain = 17.9 dB		0.75		V p-p
	LNA gain = 21.6 dB		0.45		V p-p
1 dB Input Compression Point	LNA gain = 15.6 dB		1.20		V p-p
	LNA gain = 17.9 dB		0.90		V p-p
	LNA gain = 21.6 dB		0.60		V p-p
Input Common Mode (LI-x, LG-x)			2.2		V
Output Common Mode (LO-x)	Switch off		High-Z		Ω
	Switch on		1.5		V
Output Common Mode (LOSW-x)	Switch off		High-Z		Ω
	Switch on		1.5		V
Input Resistance (LI-x)	R_{FB} = 300 Ω		50		Ω
	R_{FB} = 1350 Ω		200		Ω
	R_{FB} = ∞ (unterminated)		6		kΩ
Input Capacitance (LI-x)			20		pF
Input Referred Noise Voltage	R_S = 0 Ω				
	LNA gain = 15.6 dB		0.83		nV/√Hz
	LNA gain = 17.9 dB		0.82		nV/√Hz
	LNA gain = 21.6 dB		0.78		nV/√Hz
Input SNR	Noise bandwidth = 15 MHz, LNA gain = 21.6 dB		94		dB
Input Referred Noise Current			2.6		pA/√Hz
FULL CHANNEL (TGC) CHARACTERISTICS					
AAF Low-Pass Cutoff	−3 dB, programmable, low band mode	8		18	MHz
	−3 dB, programmable, high band mode	13.5		30	MHz
In Range AAF Bandwidth Tolerance			±10		%
Group Delay Variation	f = 1 MHz to 18 MHz, V_{GAIN} = −1.6 V to +1.6 V		±350		ps
Input Referred Noise Voltage	LNA gain = 15.6 dB		0.96		nV/√Hz
	LNA gain = 17.9 dB		0.90		nV/√Hz
	LNA gain = 21.6 dB		0.82		nV/√Hz
Noise Figure	R_S = 50 Ω				
Active Termination Matched	LNA gain = 15.6 dB, R_{FB} = 150 Ω		5.6		dB
	LNA gain = 17.9 dB, R_{FB} = 200 Ω		4.8		dB
	LNA gain = 21.6 dB, R_{FB} = 300 Ω		3.8		dB
Unterminated	LNA gain = 15.6 dB		3.2		dB
	LNA gain = 17.9 dB		2.9		dB
	LNA gain = 21.6 dB		2.6		dB
Correlated Noise Ratio	No signal, correlated/uncorrelated		−30		dB

Parameter[2]	Test Conditions/Comments	Min	Typ	Max	Unit
Output Offset		−100		+100	LSB
SNR	f_{IN} = 5 MHz at −12 dBFS, V_{GAIN} = −1.6 V		69		dBFS
	f_{IN} = 5 MHz at −1 dBFS, V_{GAIN} = 1.6 V		59		dBFS
Close-In SNR	f_{IN} = 3.5 MHz at −1 dBFS, V_{GAIN} = 0 V, 1 kHz offset		−130		dBc/√Hz
Second Harmonic	f_{IN} = 5 MHz at −12 dBFS, V_{GAIN} = −1.6 V		−70		dBc
	f_{IN} = 5 MHz at −1 dBFS, V_{GAIN} = 1.6 V		−62		dBc
Third Harmonic	f_{IN} = 5 MHz at −12 dBFS, V_{GAIN} = −1.6 V		−61		dBc
	f_{IN} = 5 MHz at −1 dBFS, V_{GAIN} = 1.6 V		−55		dBc
Two-Tone Intermodulation Distortion (IMD3)	f_{RF1} = 5.015 MHz, f_{RF2} = 5.020 MHz, A_{RF1} = −1 dBFS, A_{RF2} = −21 dBFS, V_{GAIN} = 1.6 V, IMD3 relative to A_{RF2}		−54		dBc
Channel to Channel Crosstalk	f_{IN} = 5 MHz at −1 dBFS		−60		dB
	Overrange condition[4]		−55		dB
GAIN ACCURACY	T_A = 25°C				
Gain Law Conformance Error	−1.6 < V_{GAIN} < −1.28 V		0.4		dB
	−1.28 V < V_{GAIN} < +1.28 V	−1.3		+1.3	dB
	1.28 V < V_{GAIN} < 1.6 V		−0.5		dB
Linear Gain Error	V_{GAIN} = 0 V, normalized for ideal AAF loss	−1.3		+1.3	dB
Channel to Channel Matching	−1.28 V < V_{GAIN} < +1.28 V, 1 σ		0.1		dB
PGA Gain			21/24/27/30[3]		dB
GAIN CONTROL INTERFACE					
Control Range	Differential	−1.6		+1.6	V
Control Common Mode	GAIN+, GAIN−	0.7	0.8	0.9	V
Input Impedance	GAIN+, GAIN−		10		MΩ
Gain Range			45		dB
Scale Factor	Analog		14		dB/V
	Digital step size		3.5		dB
Response Time	Analog 45 dB change		750		ns
CW DOPPLER MODE					
LO Frequency	$f_{LO} = f_{MLO}/M$	1		10	MHz
Phase Resolution	Per channel, 4LO[5] mode		45		Degrees
	Per channel, 8LO[5] mode, 16LO[5] mode		22.5		Degrees
Output DC Bias (Single-Ended)	CWI+, CWI−, CWQ+, CWQ−		AVDD2/2		V
Output AC Current Range	Per CWI+, CWI−, CWQ+, and CWQ−, each channel is enabled (2 × f_{LO} and baseband signal)		±2.2	±2.5	mA
Transconductance (Differential)	Demodulated I_{OUT}/V_{IN}, per CWI+, CWI−, CWQ+, and CWQ−				
	LNA gain = 15.6 dB		3.3		mA/V
	LNA gain = 17.9 dB		4.3		mA/V
	LNA gain = 21.6 dB		6.6		mA/V
Input Referred Noise Voltage	R_S = 0 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		1.6		nV/√Hz
	LNA gain = 17.9 dB		1.3		nV/√Hz
	LNA gain = 21.6 dB		1.0		nV/√Hz
Noise Figure	R_S = 50 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		5.7		dB
	LNA gain = 17.9 dB		4.5		dB
	LNA gain = 21.6 dB		3.4		dB
Dynamic Range	R_S = 0 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		164		dBFS/√Hz
	LNA gain = 17.9 dB		162		dBFS/√Hz
	LNA gain = 21.6 dB		160		dBFS/√Hz

Parameter[2]	Test Conditions/Comments	Min	Typ	Max	Unit
Close In SNR	−3 dBFS input, f_{RF} = 2.5 MHz, f_{LO} = 40 MHz, 1 kHz offset, 16LO[5] mode, one channel enabled		156		dBc/√Hz
	−3 dBFS input, f_{RF} = 2.5 MHz, f_{LO} = 40 MHz, 1 kHz offset, 16LO[5] mode, eight channels enabled		161		dBc/√Hz
Two-Tone Intermodulation Distortion (IMD3)	f_{RF1} = 5.015 MHz, f_{RF2} = 5.020 MHz, f_{LO} = 80 MHz, A_{RF1} = −1 dBFS, A_{RF2} = −21 dBFS, IMD3 relative to A_{RF2}		−58		dBc
LO Harmonic Rejection				−20	dBc
Quadrature Phase Error	I to Q, all phases, 1 σ		0.15		Degrees
I/Q Amplitude Imbalance	I to Q, all phases, 1 σ		0.015		dB
Channel to Channel Matching	Phase I to I, Q to Q, 1 σ		0.5		Degrees
	Amplitude I to I, Q to Q, 1 σ		0.25		dB
POWER SUPPLY	Mode I/Mode II/Mode III/Mode IV[1, 3]				
AVDD1		1.7	1.8	1.9	V
AVDD2		2.85	3.0	3.6	V
DVDD		1.3	1.4	1.9	V
DRVDD		1.7	1.8	1.9	V
I_{AVDD1}	TGC mode, LO band mode		144/188/224/294[3]		mA
	CW Doppler mode		4		mA
I_{AVDD2}	TGC mode, no signal, low band mode		230		mA
	TGC mode, no signal, high band mode		239		mA
	CW Doppler mode, eight channels enabled		140		mA
I_{DVDD}	RF decimator enabled in Mode III[1] and Mode IV,[1] digital HPF enabled		47/75/57/91[3]		mA
	RF decimator enabled in Mode III[1] and Mode IV,[1] digital HPF disabled		30/48/42/65[3]		mA
I_{DRVDD}	ANSI-644 mode		125/170/128/169[3]		mA
	Low power (IEEE 1596.3 similar) mode		109/155/114/154[3]		mA
Total Power Dissipation (Including Output Drivers)	TGC mode, no signal, RF decimator enabled in Mode III and Mode IV, digital HPF disabled		1190/1385/ 1365/1600[3]	1325/1535/ 1515/1765[3]	mW
	TGC mode, no signal, RF decimator enabled in Mode III[1] and Mode IV,[1] digital HPF enabled		1215/1425/ 1385/1640[3]	1350/1575/ 1535/1800[3]	mW
	CW Doppler mode, eight channels enabled		500		mW
Power-Down Dissipation				30	mW
Standby Power Dissipation			630		mW
ADC					
Resolution			14		Bits
SNR	f_{IN} = 5 MHz		75		dB
ADC REFERENCE					
Output Voltage Error	VREF = 1 V			±50	mV
Load Regulation at 1.0 mA	VREF = 1 V		2		mV
Input Resistance			7.5		kΩ

[1] The ADC speed modes depending on the encoding clock rate.
[2] For a complete set of definitions and information about how these tests were completed, see the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*.
[3] The slashes mean that the four different power and current values are listed for the four different modes (Mode I, Mode II, Mode III, Mode IV).
[4] The overrange condition is specified as 6 dB more than the full-scale input range.
[5] The internal LO frequency, f_{LO}, is generated from the supplied multiplier local oscillator frequency, f_{MLO}, by dividing it up by a configurable divider value (M) that can be 4, 8, or 16; the MLO signal is named 4LO, 8LO, or 16LO, accordingly.

DIGITAL SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DVDD = 1.4 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, full temperature range (0°C to 85°C), unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
INPUTS (CLK+, CLK−, TX_TRIG+, TX_TRIG−)					
Logic Compliance	Full		CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	0.2		3.6	V p-p
Input Voltage Range	Full	GND − 0.2		AVDD1 + 0.2	V
Input Common-Mode Voltage	Full		0.9		V
Input Resistance (Differential)	25°C		15		kΩ
Input Capacitance	25°C		4		pF
INPUTS (MLO±, RESET±)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage[2]	Full	0.250		2 × AVDD2	V p-p
Input Voltage Range	Full	GND − 0.2		AVDD2 + 0.2	V
Input Common-Mode Voltage	Full		AVDD2/2		V
Input Resistance (Single-Ended)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
LOGIC INPUTS (PDWN, STBY, SCLK, SDIO, ADDRx)					
Logic 1 Voltage	Full	1.2		DRVDD + 0.3	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		30 (26 for SDIO)		kΩ
Input Capacitance	25°C		2 (5 for SDIO)		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		DRVDD + 0.3	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 μA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 μA)	Full			0.05	V
DIGITAL OUTPUTS (DOUTx+, DOUTx−), ANSI-644					
Logic Compliance	Full		LVDS		
Differential Output Voltage (V_{OD})	Full	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	V
Output Coding (Default)	Full		Offset binary		
DIGITAL OUTPUTS (DOUTx+, DOUTx−), LOW POWER, REDUCED SIGNAL OPTION					
Logic Compliance	Full		LVDS		
Differential Output Voltage (V_{OD})	Full	150		250	mV
Output Offset Voltage (V_{OS})	Full	1.10		1.30	V
Output Coding (Default)	Full		Offset binary		
LOGIC OUTPUT (GPO0/GPO1/GPO2/GPO3)	Full				
Logic 0 Voltage (I_{OL} = 50 μA)	Full			0.05	V

[1] For a complete set of definitions and information about how these tests were completed, see the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*.
[2] Specified for LVDS and LVPECL only.
[3] Specified for 13 SDIO pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DVDD = 1.4 V, DRVDD = 1.8 V, full temperature range (0°C to 85°C), RF decimator bypassed, and digital HPF bypassed, unless otherwise noted.

Table 3.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK[2]					
Clock Rate					
40 MSPS (Mode I)	Full	20.5		40	MHz
65 MSPS (Mode II)	Full	20.5		65	MHz
80 MSPS (Mode III)[3]	Full	20.5		80	MHz
125 MSPS (Mode IV)[4]	Full	20.5		125	MHz
Clock Pulse Width High (t_{EH})	Full		3.75		ns
Clock Pulse Width Low (t_{EL})	Full		3.75		ns
OUTPUT PARAMETERS[2, 5]					
Propagation Delay (t_{PD})	Full	$10.8 - 1.5 \times t_{DCO}$	10.8	$10.8 + 1.5 \times t_{DCO}$	ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
DCO± Period (t_{DCO})[6]	Full		$t_{SAMPLE}/7$		ns
FCO± Propagation Delay (t_{FCO})	Full	$10.8 - 1.5 \times t_{DCO}$	10.8	$10.8 + 1.5 \times t_{DCO}$	ns
DCO± Propagation Delay (t_{CPD})[7]	Full		$t_{FCO} + (t_{SAMPLE}/28)$		ns
DCO± to Data Delay (t_{DATA})[7]	Full	$(t_{SAMPLE}/28) - 300$	$t_{SAMPLE}/28$	$(t_{SAMPLE}/28) + 300$	ps
DCO± to FCO± Delay (t_{FRAME})[7]	Full	$(t_{SAMPLE}/28) - 300$	$t_{SAMPLE}/28$	$(t_{SAMPLE}/28) + 300$	ps
Data to Data Skew ($t_{DATA-MAX} - t_{DATA-MIN}$)	Full		±225	±400	ps
TX_TRIG± to CLK± Setup Time (t_{SETUP})	25°C	1			ns
TX_TRIG± to CLK± Hold Time (t_{HOLD})	25°C	1			ns
Wake-Up Time (Standby)	25°C		2		µs
Wake-Up Time (Power-Down)	25°C		375		µs
ADC Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Uncertainty (Jitter), t_A	25°C		<1		ps rms
LO GENERATION					
MLO± Frequency					
4LO Mode	Full	4		40	MHz
8LO Mode	Full	8		80	MHz
16LO Mode	Full	16		160	MHz
RESET± to MLO± Setup Time (t_{SETUP})	Full	1	$t_{MLO}/2$		ns
RESET± to MLO± Hold Time (t_{HOLD})	Full	1	$t_{MLO}/2$		ns

[1] For a complete set of definitions and information about how these tests were completed, see the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*.
[2] The clock can be adjusted via the SPI.
[3] Mode III must have the RF decimator enabled, unless DVDD runs at 1.8 V and 12-bit mode is configured.
[4] Mode IV must have the RF decimator enabled.
[5] Measurements were made using the device soldered to FR-4 material.
[6] $t_{SAMPLE}/7$ is based on the number of bits (14) divided by 2 because the interface uses DDR sampling.
[7] $t_{SAMPLE}/28$ is based on the number of bits (14) multiplied by 2 because the delays are based on half duty cycles.

ADC Timing Diagram

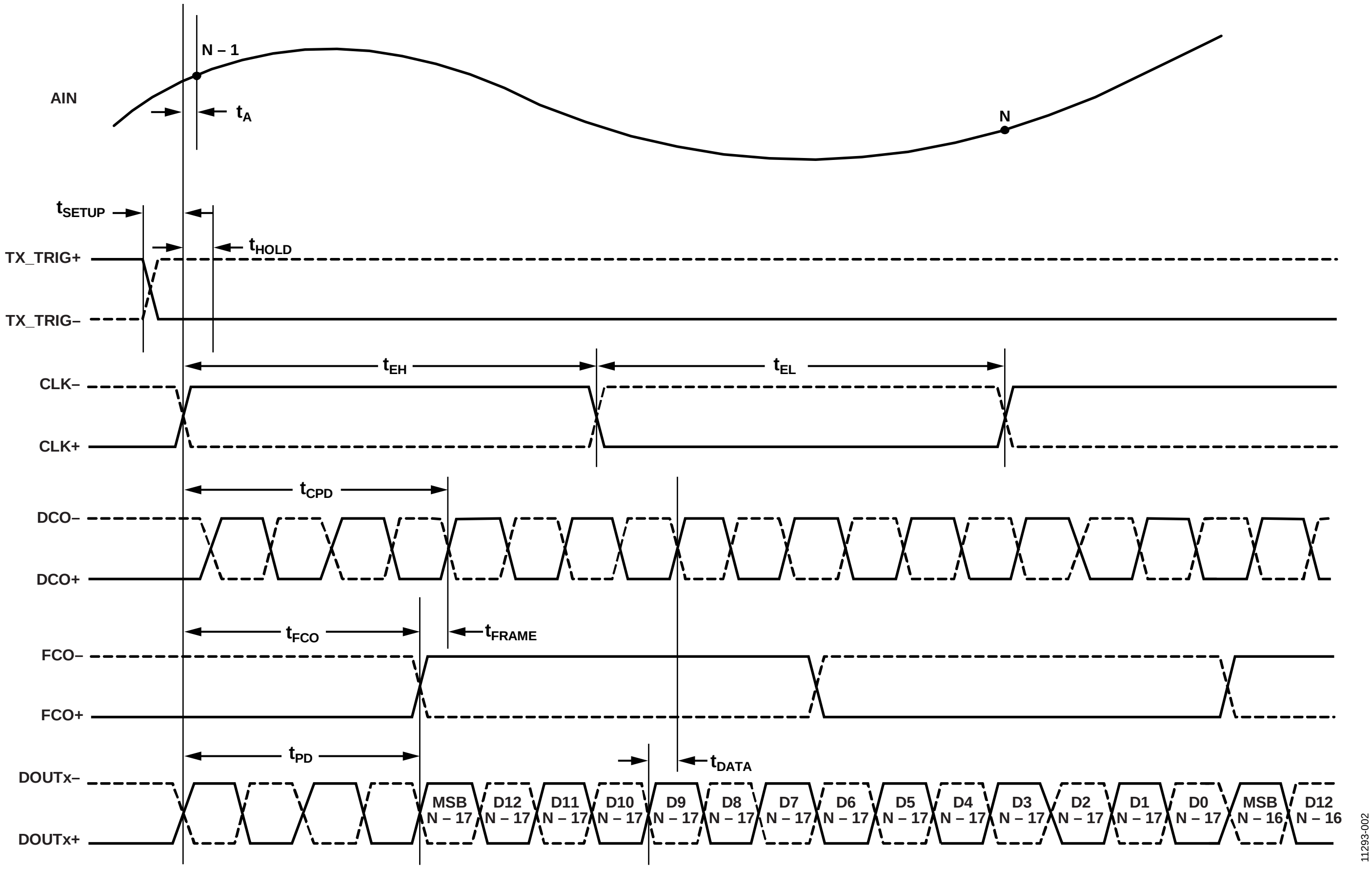

Figure 2. 14-Bit Data Serial Stream (Default, RF Decimator Bypassed, Digital HPF Bypassed), One Channel per Lane Mode, FCO Mode = Word

CW Doppler Timing Diagram

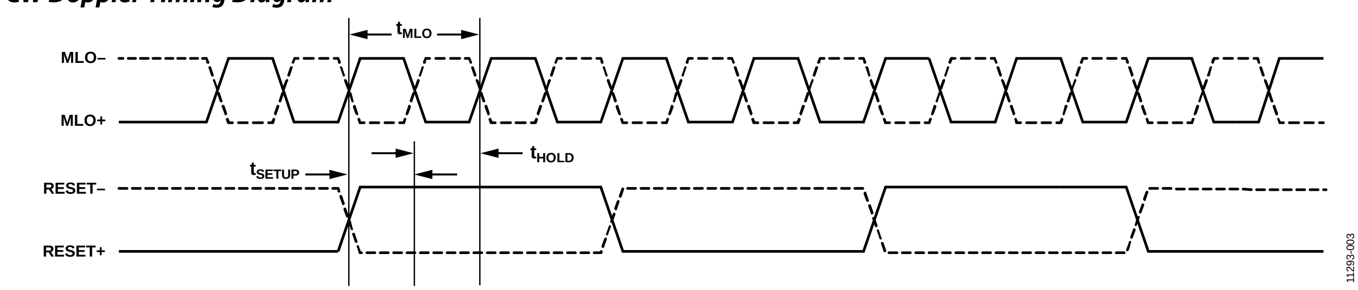

Figure 3. CW Doppler Mode Input MLO±, Continuous Synchronous RESET± Timing, Sampled on the Falling MLO± Edge, 4LO Mode

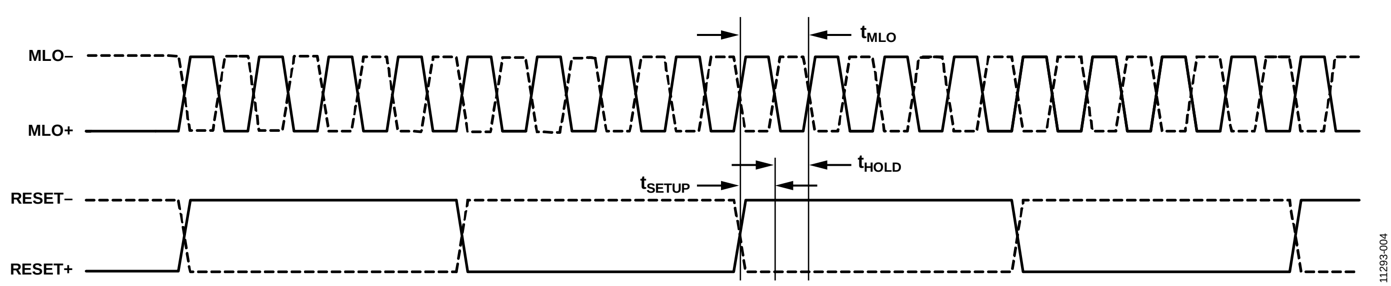

Figure 4. CW Doppler Mode Input MLO±, Continuous Synchronous RESET± Timing, Sampled on the Falling MLO± Edge, 8LO Mode

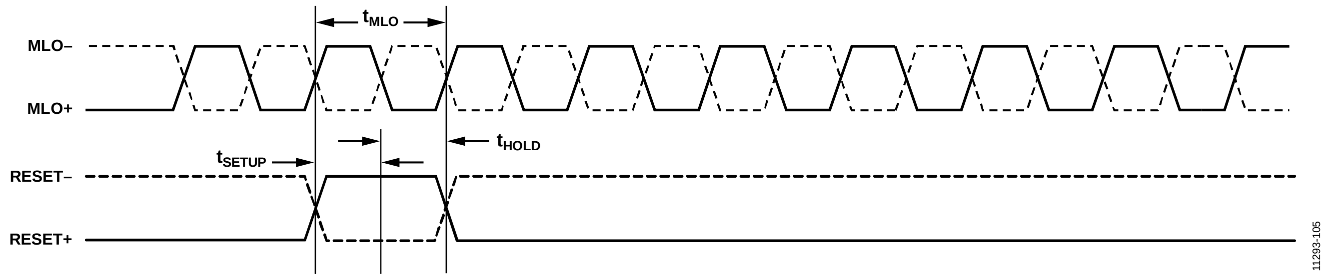

Figure 5. CW Doppler Mode Input MLO±, Pulse Synchronous RESET± Timing, 4LO/8LO/16LO Mode

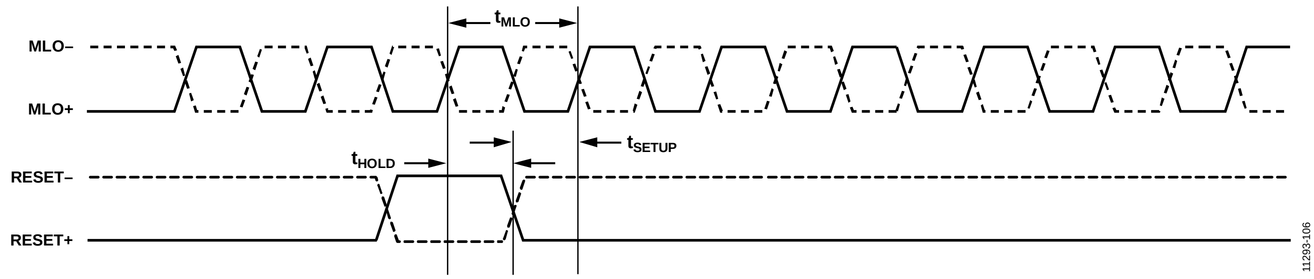

Figure 6. CW Doppler Mode Input MLO±, Pulse Asynchronous RESET± Timing, 4LO/8LO/16LO Mode

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVDD1 to GND	−0.3 V to +2.0 V
AVDD2 to GND	−0.3 V to +3.9 V
DVDD to GND	−0.3 V to +2.0 V
DRVDD to GND	−0.3 V to +2.0 V
GND to GND	−0.3 V to +0.3 V
AVDD2 to AVDD1	−2.0 V to +3.9 V
AVDD1 to DRVDD	−2.0 V to +2.0 V
AVDD2 to DRVDD	−2.0 V to +3.9 V
Digital Outputs (DOUTx+, DOUTx−, DCO+, DCO−, FCO+, FCO−) to GND	−0.3 V to DRVDD + 0.3 V
LI-x, LG-x, LO-x, LOSW-x, CWI−, CWI+, CWQ−, CWQ+, GAIN+, GAIN−, RESET+, RESET−, MLO+, MLO−, GPO0, GPO1, GPO2, GPO3 to GND	−0.3 V to AVDD2 + 0.3 V
CLK+, CLK−, TX_TRIG+, TX_TRIG−, VREF to GND	−0.3 V to AVDD1 + 0.3 V
SDIO, PDWN, STBY, SCLK, CSB, ADDRx	−0.3 V to DRVDD + 0.3 V
Operating Temperature Range (Ambient)	0°C to 85°C
Storage Temperature Range (Ambient)	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL IMPEDANCE

Table 5.

Symbol	Description	Value[1]	Unit
θ_{JA}	Junction to ambient thermal resistance, 0.0 m/sec airflow per JEDEC JESD51-2 (still air)	22.0	°C/W
Ψ_{JB}	Junction to board thermal characterization parameter, 0 m/sec airflow per JEDEC JESD51-8 (still air)	9.2	°C/W
Ψ_{JT}	Junction to top of package characterization parameter, 0 m/sec airflow per JEDEC JESD51-2 (still air)	0.12	°C/W

[1] Results are from simulations. The printed circuit board (PCB) is JEDEC multilayer. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine whether they are similar to those assumed in these calculations.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12
A	LI-E	LI-F	LI-G	LI-H	VREF	RBIAS	GAIN+	GAIN–	LI-A	LI-B	LI-C	LI-D
B	LG-E	LG-F	LG-G	LG-H	GND	GND	CLNA	GND	LG-A	LG-B	LG-C	LG-D
C	LO-E	LO-F	LO-G	LO-H	GND	GND	GND	GND	LO-A	LO-B	LO-C	LO-D
D	LOSW-E	LOSW-F	LOSW-G	LOSW-H	GND	GND	GND	GND	LOSW-A	LOSW-B	LOSW-C	LOSW-D
E	GND	AVDD2	AVDD2	AVDD2	GND	GND	GND	GND	AVDD2	AVDD2	AVDD2	GND
F	AVDD1	GND	AVDD1	GND	AVDD1	GND	GND	AVDD1	GND	AVDD1	GND	AVDD1
G	GND	AVDD1	GND	DVDD	GND	GND	GND	GND	AVDD1	GND	DVDD	GND
H	CLK–	TX_TRIG–	GND	GND	GND	GND	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	CSB
J	CLK+	TX_TRIG+	CWQ+	GND	CWI+	AVDD2	MLO+	RESET–	GPO3	GPO1	PDWN	SDIO
K	GND	GND	CWQ–	GND	CWI–	AVDD2	MLO–	RESET+	GPO2	GPO0	STBY	SCLK
L	DRVDD	DOUTH+	DOUTG+	DOUTF+	DOUTE+	DCO+	FCO+	DOUTD+	DOUTC+	DOUTB+	DOUTA+	DRVDD
M	GND	DOUTH–	DOUTG–	DOUTF–	DOUTE–	DCO–	FCO–	DOUTD–	DOUTC–	DOUTB–	DOUTA–	GND

11293-005

Figure 7. Pin Configuration

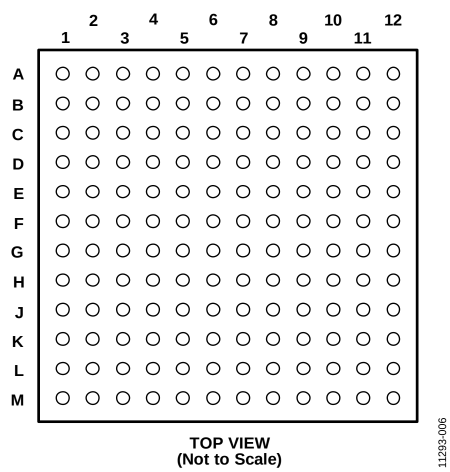

Figure 8. CSP_BGA Pin Location

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
B5, B6, B8, C5 to C8, D5 to D8, E1, E5 to E8, E12, F2, F4, F6, F7, F9, F11, G1, G3, G5 to G8, G10, G12, H3 to H6, J4, K1, K2, K4, M1, M12	GND	Ground. Tie to a quiet analog ground.
F1, F3, F5, F8, F10, F12, G2, G9	AVDD1	1.8 V Analog Supply.
G4, G11	DVDD	1.4 V/1.8 V Digital Supply.
E2 to E4, E9 to E11, J6, K6	AVDD2	3.0 V Analog Supply.
B7	CLNA	LNA External Capacitor.
L1, L12	DRVDD	1.8 V Digital Output Driver Supply.
C1	LO-E	LNA Analog Inverted Output for Channel E.
D1	LOSW-E	LNA Analog Switched Output for Channel E.
A1	LI-E	LNA Analog Input for Channel E.
B1	LG-E	LNA Ground for Channel E.
C2	LO-F	LNA Analog Inverted Output for Channel F.
D2	LOSW-F	LNA Analog Switched Output for Channel F.
A2	LI-F	LNA Analog Input for Channel F.
B2	LG-F	LNA Ground for Channel F.
C3	LO-G	LNA Analog Inverted Output for Channel G.
D3	LOSW-G	LNA Analog Switched Output for Channel G.
A3	LI-G	LNA Analog Input for Channel G.
B3	LG-G	LNA Ground for Channel G.
C4	LO-H	LNA Analog Inverted Output for Channel H.
D4	LOSW-H	LNA Analog Switched Output for Channel H.
A4	LI-H	LNA Analog Input for Channel H.
B4	LG-H	LNA Ground for Channel H.
H1	CLK–	Clock Input Complement.
J1	CLK+	Clock Input True.
H2	TX_TRIG–	Transmit Trigger Complement.
J2	TX_TRIG+	Transmit Trigger True.
H11	ADDR0	Chip Address Bit 0.
H10	ADDR1	Chip Address Bit 1.
H9	ADDR2	Chip Address Bit 2.
H8	ADDR3	Chip Address Bit 3.
H7	ADDR4	Chip Address Bit 4.
M2	DOUTH–	ADC Channel H Digital Output Complement.
L2	DOUTH+	ADC Channel H Digital Output True.
M3	DOUTG–	ADC Channel G Digital Output Complement.
L3	DOUTG+	ADC Channel G Digital Output True.
M4	DOUTF–	ADC Channel F Digital Output Complement.
L4	DOUTF+	ADC Channel F Digital Output True.
M5	DOUTE–	ADC Channel E Digital Output Complement.
L5	DOUTE+	ADC Channel E Digital Output True.
M6	DCO–	Digital Clock Output Complement.
L6	DCO+	Digital Clock Output True.
M7	FCO–	Frame Clock Digital Output Complement.
L7	FCO+	Frame Clock Digital Output True.
M8	DOUTD–	ADC Channel D Digital Output Complement.
L8	DOUTD+	ADC Channel D Digital Output True.
M9	DOUTC–	ADC Channel C Digital Output Complement.
L9	DOUTC+	ADC Channel C Digital Output True.
M10	DOUTB–	ADC Channel B Digital Output Complement.
L10	DOUTB+	ADC Channel B Digital Output True.
M11	DOUTA–	ADC Channel A Digital Output Complement.

Pin No.	Mnemonic	Description
L11	DOUTA+	ADC Channel A Digital Output True.
K11	STBY	Standby Power-Down.
J11	PDWN	Full Power-Down.
K12	SCLK	Serial Clock.
J12	SDIO	Serial Data Input/Output.
H12	CSB	Chip Select Bar.
B9	LG-A	LNA Ground for Channel A.
A9	LI-A	LNA Analog Input for Channel A.
D9	LOSW-A	LNA Analog Switched Output for Channel A.
C9	LO-A	LNA Analog Inverted Output for Channel A.
B10	LG-B	LNA Ground for Channel B.
A10	LI-B	LNA Analog Input for Channel B.
D10	LOSW-B	LNA Analog Switched Output for Channel B.
C10	LO-B	LNA Analog Inverted Output for Channel B.
B11	LG-C	LNA Ground for Channel C.
A11	LI-C	LNA Analog Input for Channel C.
D11	LOSW-C	LNA Analog Switched Output for Channel C.
C11	LO-C	LNA Analog Inverted Output for Channel C.
B12	LG-D	LNA Ground for Channel D.
A12	LI-D	LNA Analog Input for Channel D.
D12	LOSW-D	LNA Analog Switched Output for Channel D.
C12	LO-D	LNA Analog Inverted Output for Channel D.
K10	GPO0	General-Purpose Open-Drain Output 0.
J10	GPO1	General-Purpose Open-Drain Output 1.
K9	GPO2	General-Purpose Open-Drain Output 2.
J9	GPO3	General-Purpose Open-Drain Output 3.
J8	RESET−	Synchronizing Input for LO Divide-by-M Counter Complement.
K8	RESET+	Synchronizing Input for LO Divide-by-M Counter True.
K7	MLO−	CW Doppler Multiple Local Oscillator Input Complement.
J7	MLO+	CW Doppler Multiple Local Oscillator Input True.
A8	GAIN−	Gain Control Voltage Input Complement.
A7	GAIN+	Gain Control Voltage Input True.
A6	RBIAS	External Resistor to Set the Internal ADC Core Bias Current.
A5	VREF	Voltage Reference Input/Output.
K5	CWI−	CW Doppler I Output Complement.
J5	CWI+	CW Doppler I Output True.
K3	CWQ−	CW Doppler Q Output Complement.
J3	CWQ+	CW Doppler Q Output True.

TYPICAL PERFORMANCE CHARACTERISTICS

TGC MODE

Mode I = f_{SAMPLE} = 40 MSPS, f_{IN} = 5 MHz, LO band mode, R_S = 50 Ω, R_{FB} = ∞ (unterminated), LNA gain = 21.6 dB, LNA bias = midhigh, PGA gain = 27 dB, V_{GAIN} = (GAIN+) − (GAIN−) = 1.6 V, AAF LPF cutoff = f_{SAMPLE}/3, HPF cutoff = LPF cutoff/12 (default), RF decimator bypassed, and digital HPF bypassed, unless otherwise noted.

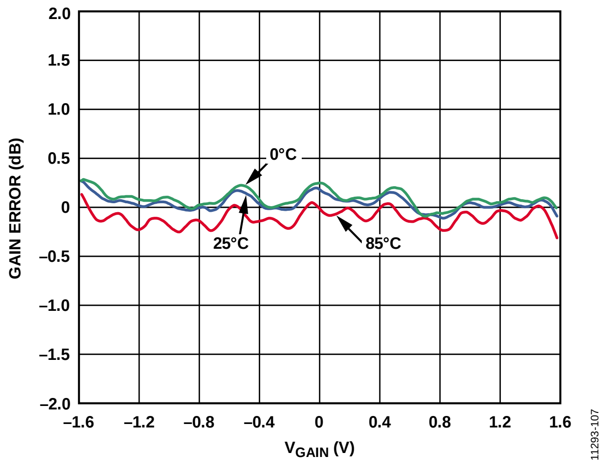

Figure 9. Gain Error vs. V_{GAIN}

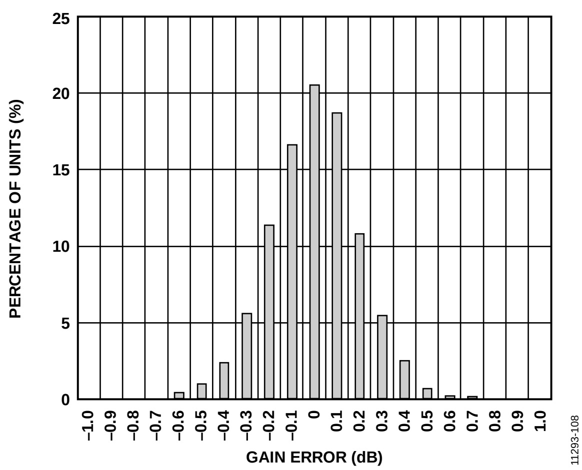

Figure 10. Gain Error Histogram, V_{GAIN} = −1.28 V

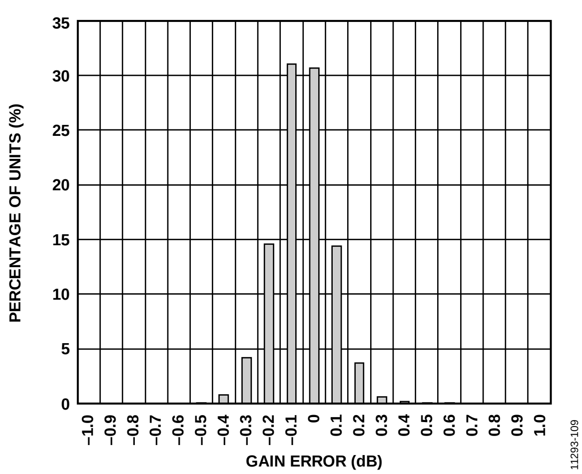

Figure 11. Gain Error Histogram, V_{GAIN} = 0 V

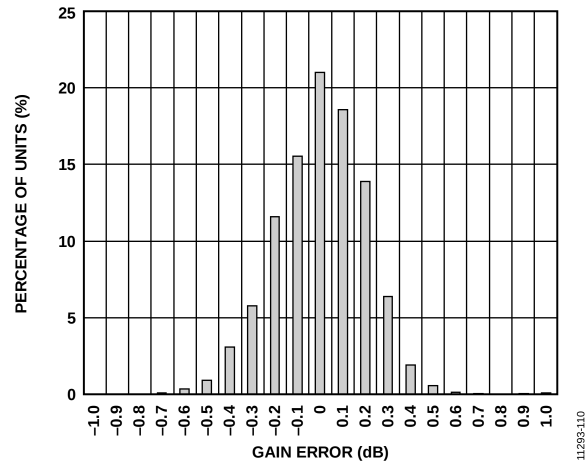

Figure 12. Gain Error Histogram, V_{GAIN} = 1.28 V

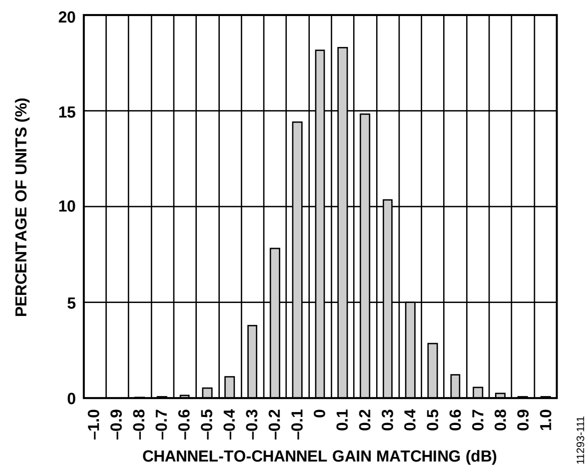

Figure 13. Gain Matching Histogram, V_{GAIN} = −1.2 V

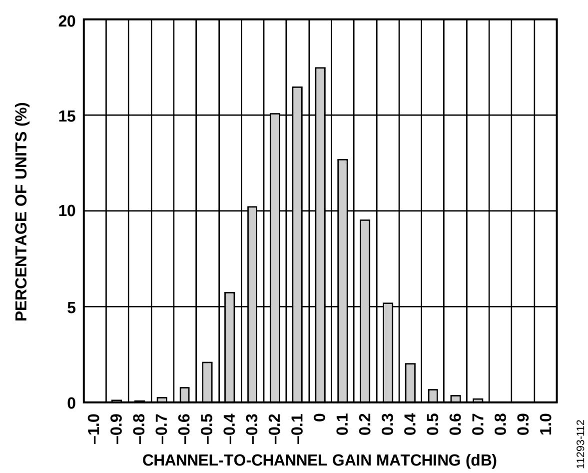

Figure 14. Gain Matching Histogram, V_{GAIN} = 1.2 V

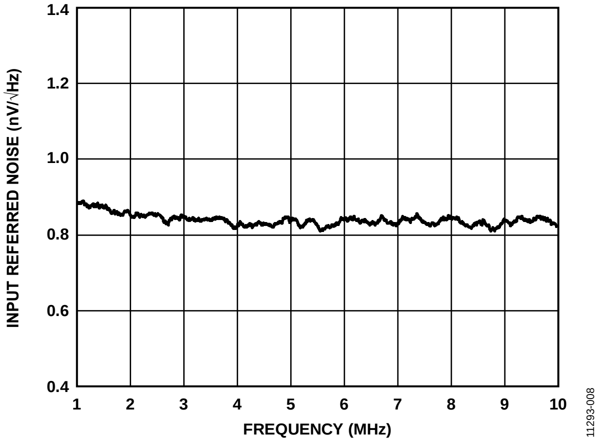

Figure 15. Short-Circuit, Input Referred Noise vs. Frequency

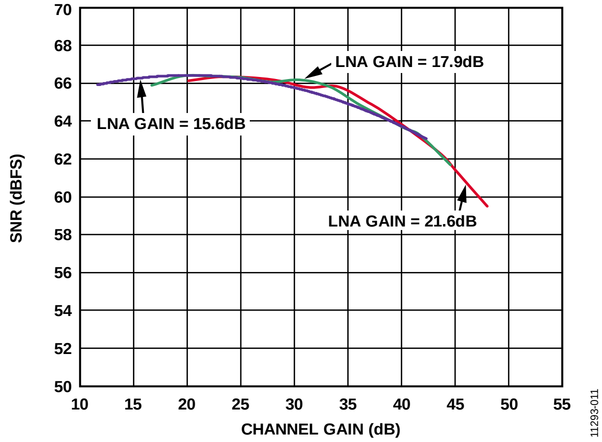

Figure 18. SNR vs. Channel Gain and LNA Gain, Output Amplitude (A_{OUT}) = −1.0 dBFS

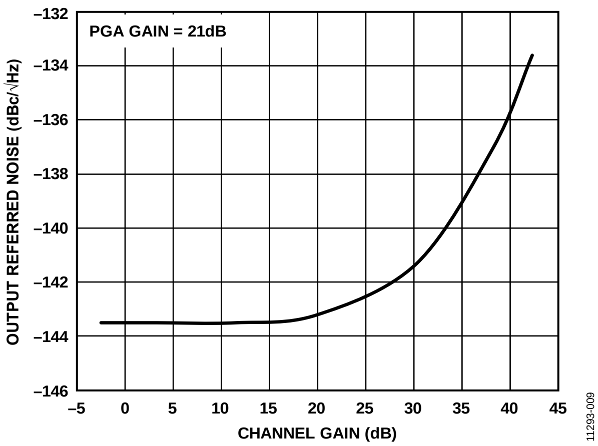

Figure 16. Short-Circuit, Output Referred Noise vs. Channel Gain, PGA Gain = 21 dB, V_{GAIN} = 1.6 V

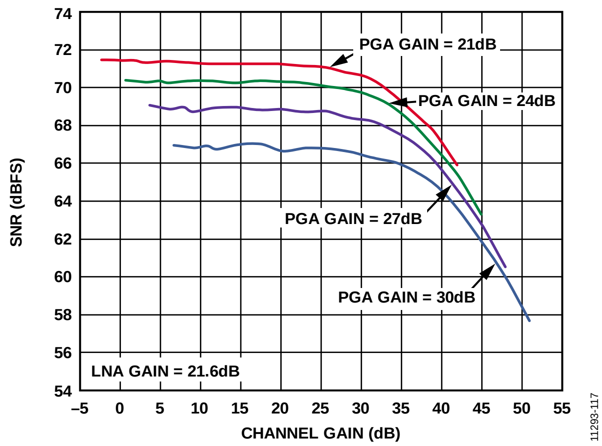

Figure 19. SNR vs. Channel Gain and PGA Gain, Input Amplitude (A_{IN}) = −45 dBm

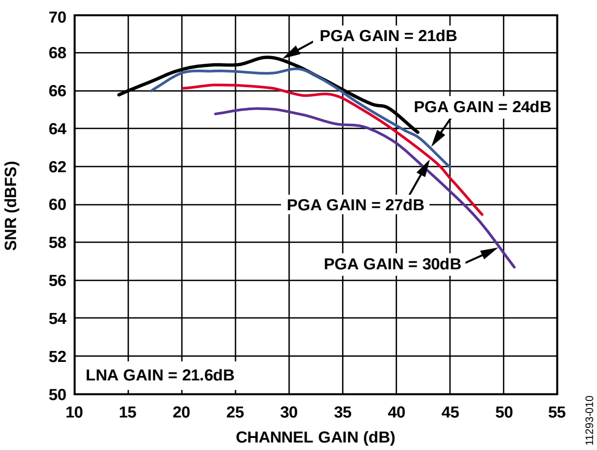

Figure 17. SNR vs. Channel Gain and PGA Gain, A_{OUT} = −1.0 dBFS

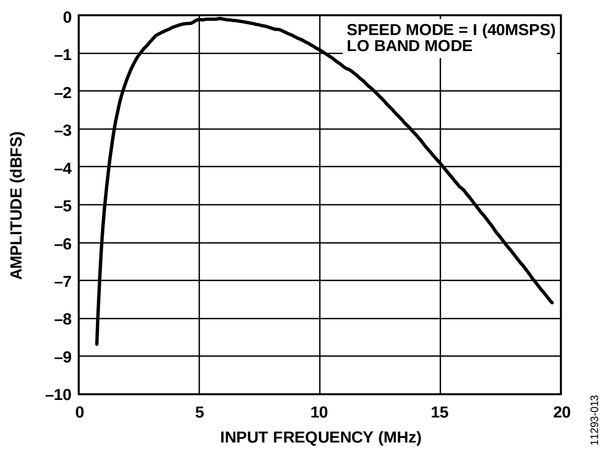

Figure 20. AAF Pass-Band Response, LPF Cutoff = 1 × (1/3) × f_{SAMPLE}, HPF = LPF Cutoff/12

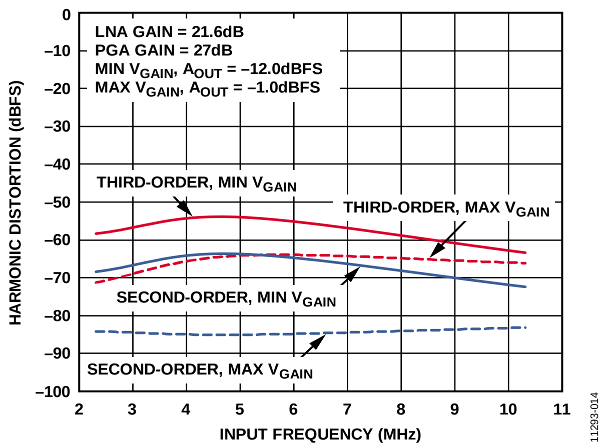

Figure 21. Second-Order and Third-Order Harmonic Distortion vs. Input Frequency, A_{OUT} = −1.0 dBFS

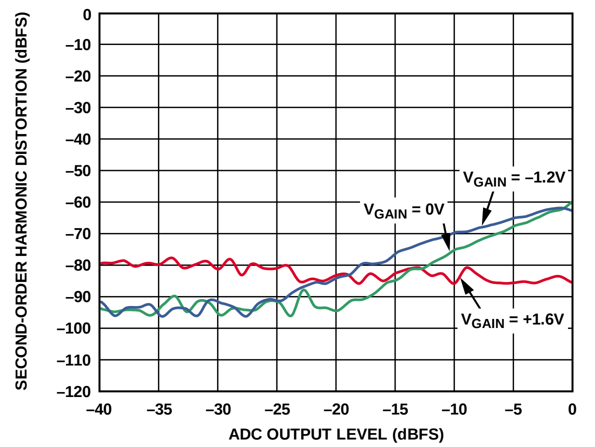

Figure 24. Second-Order Harmonic Distortion vs. ADC Output Level (A_{OUT})

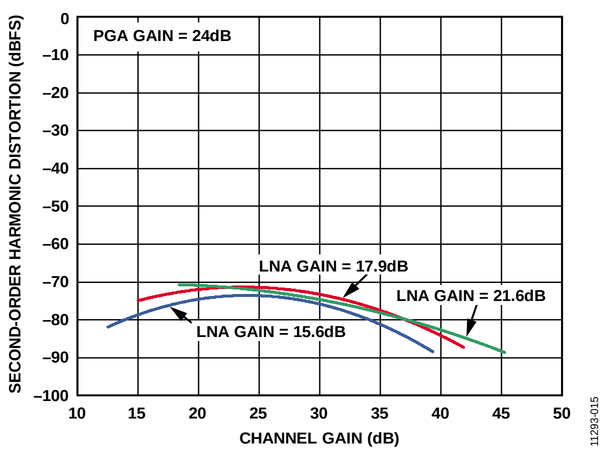

Figure 22. Second-Order Harmonic Distortion vs. Channel Gain, A_{OUT} = −1.0 dBFS

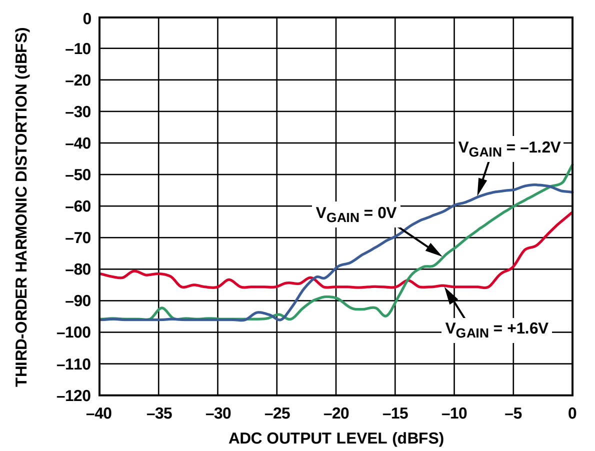

Figure 25. Third-Order Harmonic Distortion vs. ADC Output Level (A_{OUT})

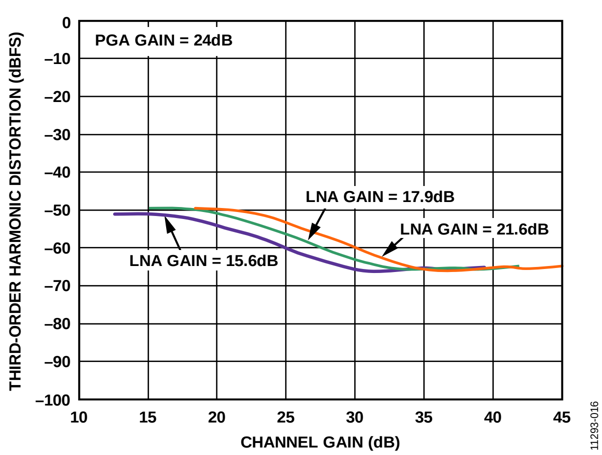

Figure 23. Third-Order Harmonic Distortion vs. Channel Gain, A_{OUT} = −1.0 dBFS

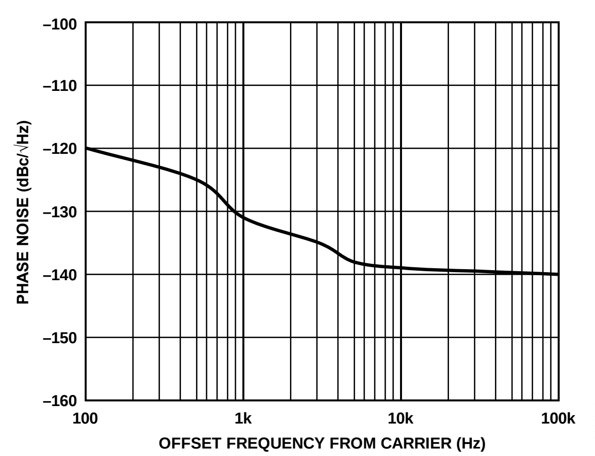

Figure 26. TGC Path Phase Noise, LNA Gain = 21.6 dB, PGA Gain = 27 dB, V_{GAIN} = 0 V

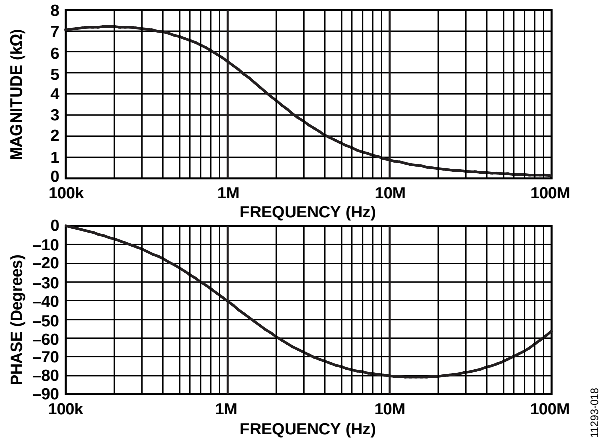

Figure 27. LNA Input Impedance Magnitude and Phase, Unterminated

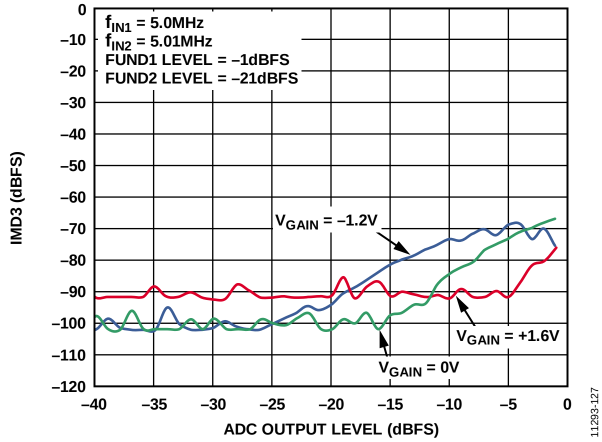

Figure 29. IMD3 vs. ADC Output Level (A_{OUT})

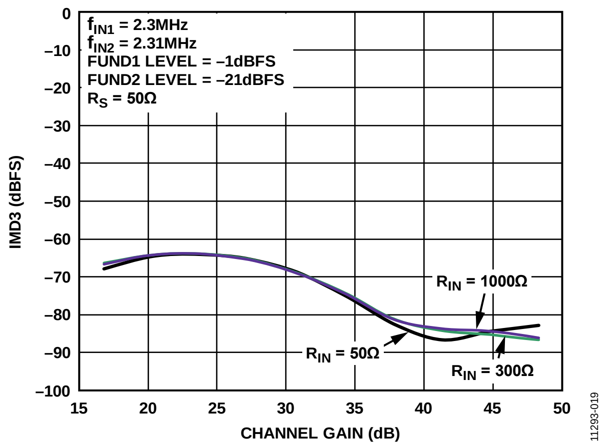

Figure 28. IMD3 vs. Channel Gain

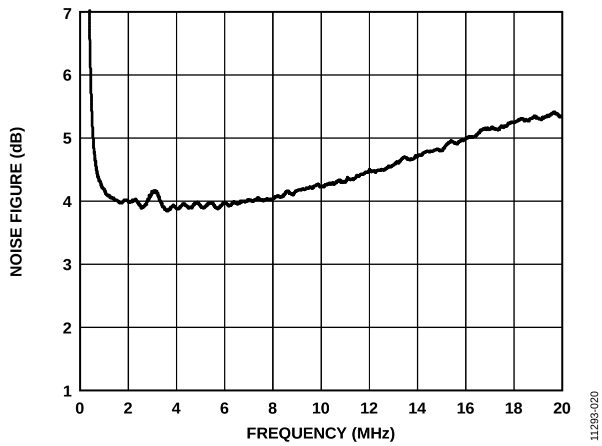

Figure 30. Noise Figure vs. Frequency, $R_S = R_{IN} = 100\ \Omega$, LNA Gain = 17.9 dB, PGA Gain = 30 dB, $V_{GAIN} = 1.6$ V

CW DOPPLER MODE

f_{IN} = 5 MHz, f_{LO} = 20 MHz, 4LO mode, R_S = 50 Ω, LNA gain = 21.6 dB, LNA bias = midhigh, all CW channels enabled, phase rotation = 0°.

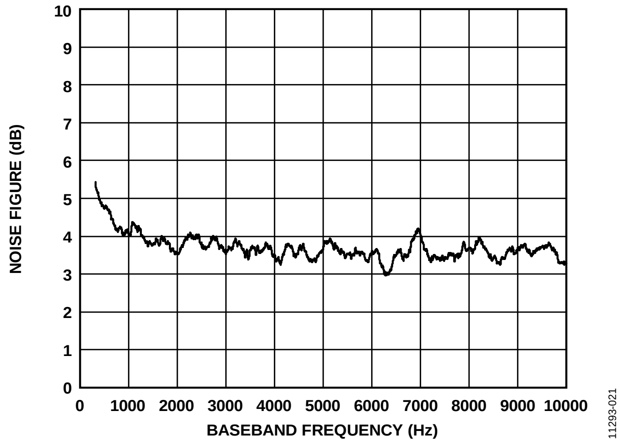

Figure 31. Noise Figure vs. Baseband Frequency

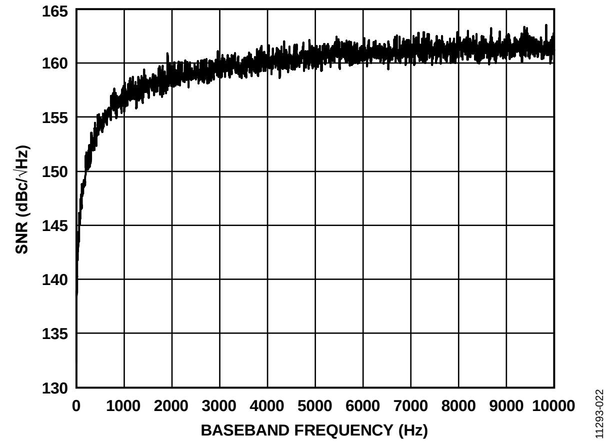

Figure 32. SNR vs. Baseband Frequency, −3 dBFS LNA Input

THEORY OF OPERATION

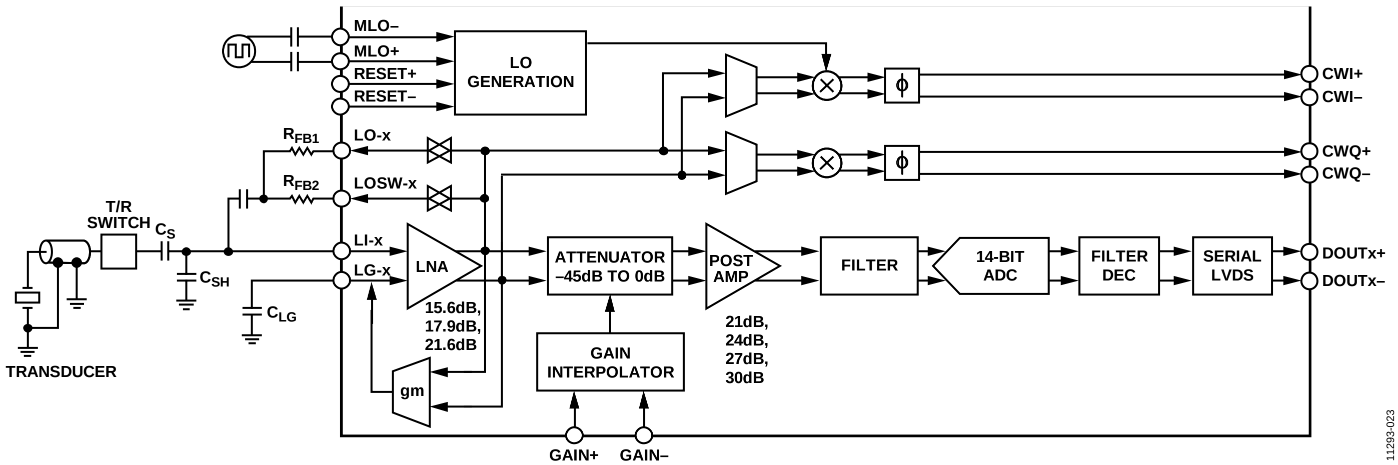

Figure 33. Simplified Block Diagram of a Single Channel

Each channel of the AD9674 contains both a TGC signal path and a CW Doppler signal path. Common to both signal paths, the LNA provides four user adjustable input impedance termination options for matching different probe impedances. The CW Doppler path includes an I/Q demodulator with the programmable phase rotation needed for analog beamforming. The TGC path includes a differential X-AMP® VGA, an antialiasing filter, an ADC, and a digital HPF and RF decimator. Figure 33 shows a simplified block diagram with the external components.

TGC OPERATION

The system gain is distributed as listed in Table 7.

Table 7. Channel Analog Gain Distribution

Section	Nominal Gain (dB)
LNA	15.6/17.9/21.6 (LNA_{GAIN})[1]
Attenuator	−45 to 0 (VGA_{ATT})
VGA Amplifier	21/24/27/30 (PGA_{GAIN})[1]
Filter	0
ADC	0

[1] The slashes represent the LNA and PGA gain settings that can change using SPI registers.

Each LNA output is dc-coupled to a VGA input. The VGA consists of an attenuator with a −45 dB to 0 dB range followed by an amplifier with 21 dB, 24 dB, 27 dB, or 30 dB of gain. The X-AMP gain interpolation technique results in low gain error and uniform bandwidth; differential signal paths minimize distortion.

The linear in dB gain (law conformance) range of the TGC path is 45 dB. The slope of the gain control interface is 14 dB/V, and the gain control range is −1.6 V to +1.6 V. Equation 1 is the expression for the differential voltage, V_{GAIN}, at the gain control interface. Equation 2 is the expression for the VGA attenuation, VGA_{ATT}, as a function of V_{GAIN}.

$$V_{GAIN}\ (\text{V}) = (GAIN+) - (GAIN-) \quad (1)$$

$$VGA_{ATT}\ (\text{dB}) = -14\ (\text{dB/V}) \times (1.6 - V_{GAIN}) \quad (2)$$

The total channel gain can then be calculated as shown in Equation 3.

$$Channel\ Gain\ (\text{dB}) = LNA_{GAIN} + VGA_{ATT} + PGA_{GAIN} \quad (3)$$

In its default condition, the LNA has a gain of 21.6 dB (12×), and the VGA postamplifier gain is 24 dB. If the voltage on the GAIN+ pin is 0 V and the voltage on the GAIN− pin is 1.6 V (45.1 dB attenuation), the total gain of the channel is 0.5 dB if the LNA input is unmatched. The channel gain is −5.5 dB if the LNA is matched to 50 Ω (R_{FB} = 300 Ω). However, if the voltage on the GAIN+ pin is 1.6 V and the voltage on the GAIN− pin is 0 V (0 dB attenuation), VGA_{ATT} is 0 dB. This results in a total gain of 45.3 dB through the TGC path if the LNA input is unmatched, or in a total gain of 39.3 dB, if the LNA input is matched. Similarly, if the LNA input is unmatched and has a gain of 21.6 dB (12×), and the VGA postamplifier gain is 30 dB, the channel gain is approximately 52 dB with 0 dB VGA_{ATT}.

In addition to the analog VGA attenuation described in Equation 2, the attenuation level can be digitally controlled in 3.5 dB increments. Equation 3 is still valid, and the value of VGA_{ATT} is equal to the attenuation level set in Address 0x011, Bits[7:4].

Low Noise Amplifier (LNA)

Good system sensitivity relies on a proprietary ultralow noise LNA at the beginning of the signal chain, which minimizes the noise contribution in the following VGA. Active impedance control optimizes noise performance for applications that benefit from input impedance matching.

The LNA input, LI-x, is capacitively coupled to the source. An on-chip bias generator establishes dc input bias voltages of approximately 2.2 V and centers the output common-mode levels at 1.5 V (AVDD2 divided by 2). A capacitor, C_{LG}, of the same value as the input coupling capacitor, C_S, is connected from LG-x to ground.

The LNA supports three gain settings, 21.6 dB, 17.9 dB, or 15.6 dB, set through the SPI. Overload protection ensures quick recovery time from large input voltages.

Low value feedback resistors and the current driving capability of the output stage allow the LNA to achieve a low input referred noise voltage of 0.78 nV/√Hz (at a gain of 21.6 dB). On-chip resistor matching results in precise single-ended gains, which are critical for accurate impedance control. The use of a fully differential topology and negative feedback minimizes distortion. Low second-order harmonic distortion is particularly important in harmonic ultrasound imaging applications.

Active Impedance Matching

The LNA consists of a single-ended voltage gain amplifier with differential outputs; the negative output is externally available on two output pins (LO-x and LOSW-x) that are controlled via internal switches. This configuration allows active input impedance synthesis of three different impedance values (and an unterminated value) by connecting up to two external resistances in parallel and controlling the internal switch states via the SPI. For example, with a fixed gain of 8× (17.9 dB), an active input termination is synthesized by connecting a feedback resistor between the negative output pin, LO-x, and the positive input pin, LI-x. This well-known technique is used for interfacing multiple probe impedances to a single system. The input resistance calculation is shown in Equation 4.

$$R_{IN} = \frac{(R_{FB1} + 20\ \Omega) \,||\, (R_{FB2} + 20\ \Omega) + 30\ \Omega}{\left(1 + \frac{A}{2}\right)} \tag{4}$$

where A/2 is the single-ended gain or the gain from the LI-x inputs to the LO-x outputs, R_{FB1} and R_{FB2} are the external feedback resistors, the 20 Ω is the internal switch on resistance, and the 30 Ω is an internal series resistance common to the two internal switches. R_{FB} can equal to R_{FB1}, R_{FB2}, or $(R_{FB1} + 20\ \Omega)||(R_{FB2} + 20\ \Omega)$ depending on the connection status of the internal switches.

Because the amplifier has a gain of 8× from its input to its differential output, it is important to note that the gain, A/2, is the gain from the LI-x pin to the LO-x pin, and that it is 6 dB less than the gain of the amplifier, or 12.1 dB (4×). The input resistance is reduced by an internal bias resistor of 6 kΩ in parallel with the source resistance connected to the LI-x pin and with the LG-x pin ac grounded. Equation 5 can be used to calculate the required R_{FB} for a desired R_{IN}, even for higher values of R_{IN}.

$$R_{IN} = \frac{(R_{FB1} + 20\ \Omega) \,||\, (R_{FB2} + 20\ \Omega) + 30\ \Omega}{\left(1 + \frac{A}{2}\right)} \,||\, 6\ \text{k}\Omega \tag{5}$$

For example, to set R_{IN} to 200 Ω with a single-ended LNA gain of 12.1 dB (4×), the value of R_{FB} from Equation 4 must be 950 Ω while the switch for R_{FB2} is open. If the more accurate equation (Equation 5) is used to calculate R_{IN}, the value is then 194 Ω instead of 200 Ω, resulting in a gain error of less than 0.27 dB. Some factors, such as the presence of a dynamic source resistance, may influence the absolute gain accuracy more significantly.

At higher frequencies, the input capacitance of the LNA must be considered. The user must determine the level of matching accuracy and adjust R_{FB} accordingly.

R_{FB} is the resulting impedance of the R_{FB1} and R_{FB2} combination (see Figure 33). Using Address 0x02C in the SPI memory, the AD9674 can be programmed for four impedance matching options: three active terminations and one unterminated option. Table 8 shows an example of how to select R_{FB1} and R_{FB2} for R_{IN} = 66 Ω, 100 Ω, and 200 Ω input impedances for an LNA gain = 21.6 dB (12×).

Table 8. Active Termination Example for LNA Gain = 21.6 dB, R_{FB1} = 650 Ω, and R_{FB2} = 1350 Ω

Reg. 0x02C, Bits[1:0]	R_S (Ω)	LO-x Switch	LOSW-x Switch	R_{FB} (Ω)	R_{IN} (Ω) (Eq. 4)
00 (default)	100	On	Off	R_{FB1}	100
01	50	On	On	$R_{FB1}\|\|R_{FB2}$	66
10	200	Off	On	R_{FB2}	200
11	N/A[1]	Off	Off	∞	∞

[1] N/A means not applicable.

The bandwidth (BW) of the LNA is greater than 80 MHz. Ultimately, the BW of the LNA limits the accuracy of the synthesized R_{IN}. R_{IN} = R_S up to approximately 200 Ω. The best match is between 100 kHz and 10 MHz where the lower frequency limit is determined by the size of the ac coupling capacitors and the upper limit is determined by the LNA BW. Furthermore, the input capacitance and R_S limit the BW at higher frequencies. Figure 34 shows input resistance (R_{IN}) vs. frequency for various R_{FB} values.

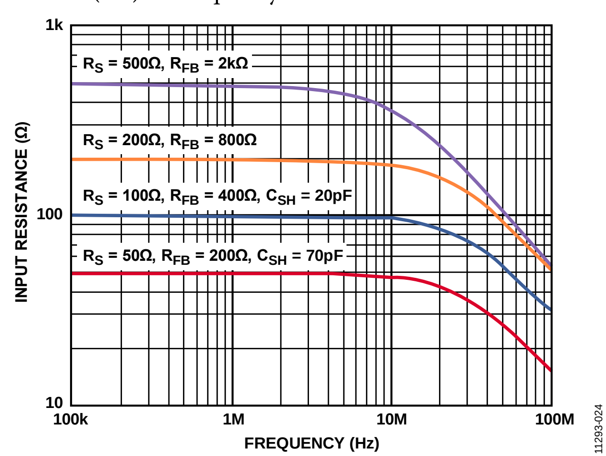

Figure 34. Input Resistance (R_{IN}) vs. Frequency for Various R_{FB} Values (Effects of R_S and C_{SH} Are Also Shown)

For larger R_{IN} values, parasitic capacitance starts rolling off the signal BW before the LNA can produce peaking. C_{SH} further degrades the match; therefore, do not use C_{SH} for values of R_{IN} that are greater than 100 Ω (see Figure 34).

Table 9 lists the recommended values for R_{FB} and C_{SH} in terms of R_{IN}. C_{FB} is needed in series with R_{FB} because the dc levels at the LO-x pin and the LI-x pin are unequal.

Table 9. Active Termination External Component Values

LNA Gain (dB)	R_{IN} (Ω)	R_{FB} (Ω)	Minimum C_{SH} (pF)
15.6	50	150	90
17.9	50	200	70
21.6	50	300	50
15.6	100	350	30
17.9	100	450	20
21.6	100	650	10
15.6	200	750	Not applicable
17.9	200	950	Not applicable
21.6	200	1350	Not applicable

LNA Noise

The short-circuit noise voltage (input referred noise) is an important limit on system performance. The short-circuit noise voltage for the LNA is 0.78 nV/√Hz at a gain of 21.6 dB, including the VGA noise at a VGA postamplifier gain of 27 dB. These measurements, which were taken without a feedback resistor, provide the basis for calculating the input noise and noise figure (NF) performance.

Figure 35 and Figure 36 are simulations of noise figure vs. R_S results with different input configurations and an input referred noise voltage of 2.5 nV/√Hz for the VGA. The unterminated ($R_{FB} = \infty$) operation exhibits the lowest equivalent input noise and noise figure. Figure 36 shows the noise figure vs. the source resistance rising at low R_S, where the LNA voltage noise is large compared with the source noise, and at high R_S due to the noise contribution from R_{FB}. The lowest NF is achieved when R_S matches R_{IN}.

Figure 35 shows the relative noise figure performance. With an LNA gain of 21.6 dB, the input impedance is swept with R_S to preserve the match at each point. The noise figures for a source impedance of 50 Ω are 7 dB, 4 dB, and 2.5 dB for the shunt termination, active termination, and unterminated configurations, respectively. The noise figures for 200 Ω are 4.5 dB, 1.7 dB, and 1 dB, respectively.

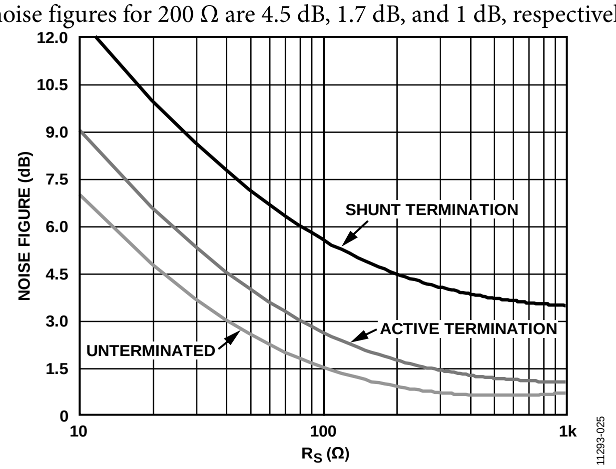

Figure 35. Noise Figure vs. R_S for Shunt Termination, Active Termination Matched and Unterminated Inputs, V_{GAIN} = 1.6 V

Figure 36 shows the noise figure as it relates to R_S for various values of R_{IN}, which is helpful for design purposes.

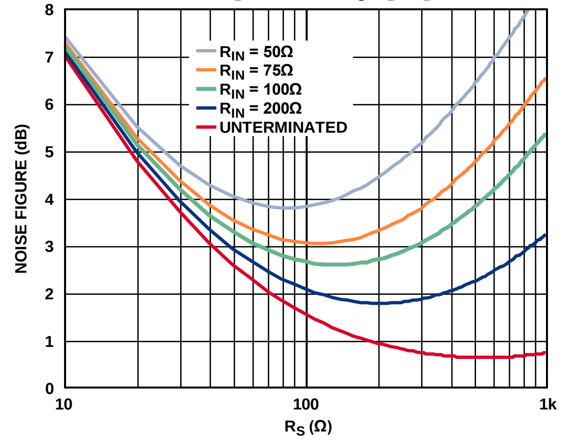

Figure 36. Noise Figure vs. R_S for Various Fixed Values of R_{IN}, Active Termination Matched Inputs, V_{GAIN} = 1.6 V

CLNA Connection

CLNA (Ball B7) must have a 1 nF capacitor attached to AVDD2.

DC Offset Correction/High-Pass Filter

The AD9674 LNA architecture is designed to correct for dc offset voltages that can develop on the external C_S capacitor due to leakage of the transmit/receive switch during ultrasound transmit cycles. The dc offset correction, as shown in Figure 37, provides a feedback mechanism to the LG-x input of the LNA to correct for this dc voltage.

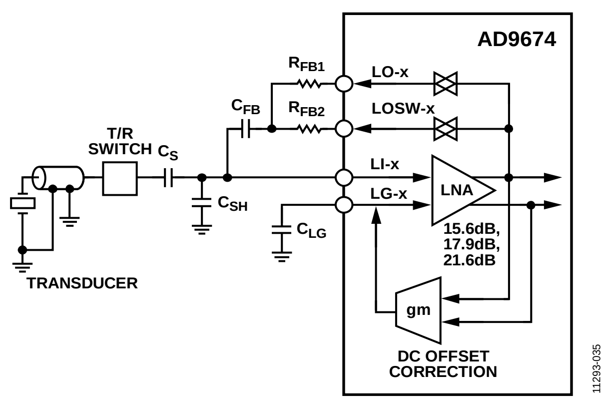

Figure 37. Simplified LNA Input Configuration

The feedback acts as a high-pass filter providing dynamic correction of the dc offset. The cutoff frequency of the high-pass filter response is dependent on the value of the C_{LG} capacitor, the gain of the LNA (LNA_{GAIN}), and the g_m of the feedback transconductance amplifier. The g_m value is programmed in Address 0x120, Bits[4:3]. It is required that C_S be equal to C_{LG} for proper operation.

Table 10. High-Pass Filter Cutoff Frequency, f_{HP}, for C_{LG} = 10 nF

Addr. 0x120[4:3]	g_m (mS)	LNA_{GAIN} = 15.6 dB	LNA_{GAIN} = 17.9 dB	LNA_{GAIN} = 21.6 dB
00 (default)	0.5 mS	41 kHz	55 kHz	83 kHz
01	1.0 mS	83 kHz	110 kHz	167 kHz
10	1.5 mS	133 kHz	178 kHz	267 kHz
11	2.0 mS	167 kHz	220 kHz	330 kHz

For other values of C_{LG}, the high-pass filter cutoff frequency can be determined by scaling the values from Table 10 or by calculating the value based on C_{LG}, LNA_{GAIN}, and g_m, as shown in Equation 6.

$$f_{HP}(C_{LG}) = \frac{1}{2\times\pi}\times LNA_{GAIN}\times\frac{g_m}{C_{LG}} = f_{HP}(Table\ 10)\times\frac{10\text{ nF}}{C_{LG}} \quad (6)$$

Variable Gain Amplifier (VGA)

The differential X-AMP VGA provides precise input attenuation and interpolation. It has a low input referred noise of 2.5 nV/√Hz and excellent gain linearity. The VGA is driven by a fully differential input signal from the LNA. The X-AMP architecture produces a linear in dB gain law conformance and low distortion levels, deviating only ±0.5 dB or less from the ideal. The gain slope is monotonic with respect to the control voltage and is stable with variations in process, temperature, and supply. The resulting total gain range is 45 dB, allowing range loss at the endpoints.

The X-AMP inputs are part of a programmable gain amplifier (PGA) that completes the VGA. The PGA in the VGA can be programmed to a gain of 21 dB, 24 dB, 27 dB, or 30 dB, allowing optimization of the channel gain for different imaging modes in the ultrasound system. The VGA bandwidth is greater than 100 MHz. The input stage is designed to ensure excellent frequency response uniformity across the gain setting. For TGC mode, the design of the input stage minimizes time delay variation across the gain range.

Gain Control

The analog gain control interface, GAIN±, is a differential input. V_{GAIN} varies the gain of all VGAs through the interpolator by selecting the appropriate input stages connected to the input attenuator. The nominal V_{GAIN} range is 14 dB/V from −1.6 V to +1.6 V, with the best gain linearity from approximately −1.44 V to +1.44 V, where the error is typically less than ±0.5 dB. For V_{GAIN} voltages greater than +1.44 V and less than −1.44 V, the error increases. The value of GAIN± can exceed the supply voltage by 1 V without gain foldover.

The gain control response time is less than 750 ns to settle within 10% of the final value for a change from minimum to maximum gain.

The differential input pins, GAIN+ and GAIN−, can interface to an amplifier, as shown in Figure 38. Decouple and drive the GAIN+ and GAIN− pins to accommodate a 3.2 V full-scale input.

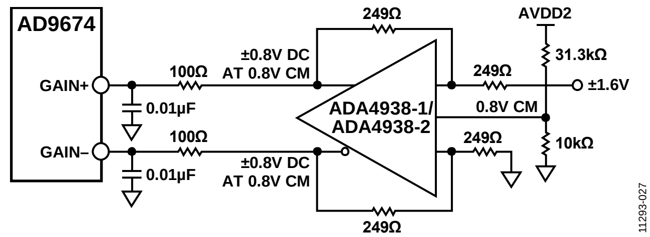

Figure 38. Differential GAIN± Pin Configuration

The analog gain control can be disabled and the attenuator can be controlled digitally using Address 0x011, Bits[7:4]. The control range is 45 dB, and the step size is 3.5 dB.

VGA Noise

In a typical application, a VGA compresses a wide dynamic range input signal to within the input span of an ADC. The input referred noise of the LNA limits the minimum resolvable input signal, whereas the output referred noise, which depends primarily on the VGA, limits the maximum instantaneous dynamic range that can be processed at any one particular gain control voltage. This latter limit is set in accordance with the total noise floor of the ADC.

The output referred noise is a flat 40 nV/√Hz (postamplifier gain = 24 dB) over most of the gain range because it is dominated by the fixed output referred noise of the VGA. At the high end of the gain control range, the noise of the LNA and the source prevail. The input referred noise reaches its minimum value near the maximum gain control voltage, where the input referred contribution of the VGA is miniscule.

At lower gains, the input referred noise and, therefore, the noise figure increase as the gain decreases. The instantaneous dynamic range of the system is not lost, however, because the input capacity increases as the input referred noise increases. The contribution of the ADC noise floor has the same dependence. The important relationship is the magnitude of the VGA output noise floor relative to that of the ADC.

Gain control noise is a concern in very low noise applications. Thermal noise in the gain control interface can modulate the channel gain. The resulting noise is proportional to the output signal level and is usually evident only when a large signal is present. Take care to minimize noise impinging at the GAIN± inputs. An external RC filter can be used to remove V_{GAIN} source noise. The filter bandwidth must be sufficient to accommodate the desired control bandwidth and attenuate unwanted switching noise from the external digital-to-analog converters used to drive the gain control.

The AD9674 can bypass the GAIN± inputs and control the gain of the attenuator digitally (see the Gain Control section). This mode removes any external noise contributions when active gain control is not needed.

Antialiasing Filter (AAF)

The filter that the signal reaches prior to the ADC is used to reject dc signals and to band limit the signal for antialiasing. The antialiasing filter is a combination of a single-pole high-pass filter and a second-order low-pass filter. The high-pass filter can be configured as a ratio of the low-pass filter cutoff frequency. This is selectable using Address 0x02B, Bits[1:0].

The filter uses on-chip tuning to trim the capacitors and set the desired low-pass cutoff frequency and reduce variations. The default −3 dB low-pass filter cutoff is 1/3, 1/4.5, or 1/6 of the ADC sample clock rate. The cutoff can be scaled to 0.75, 0.8, 0.9, 1.0, 1.13, 1.25, or 1.45 times this frequency using Address 0x00F. The cutoff tolerance (±10%) is maintained from 8 MHz to 18 MHz for low band mode or 13.5 MHz to 30 MHz for high band mode.

Table 11 and Table 12 calculate the valid SPI-selectable low-pass filter settings and the expected cutoff frequencies for low band mode and high band mode at the minimum and the maximum sample frequency in each speed mode.

Table 11. SPI-Selectable Low-Pass Filter Cutoff Options for Low Band Mode at Example Sampling Frequencies

Address 0x00F[7:3]	LPF Cutoff Frequency (MHz)	Sampling Frequency (MHz)				
		20.5	40	65	80	125
0 0000	$1.45 \times (1/3) \times f_{SAMPLE}$	9.91	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range
0 0001	$1.25 \times (1/3) \times f_{SAMPLE}$	8.54	16.67	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range
0 0010	$1.13 \times (1/3) \times f_{SAMPLE}$	Out of tunable filter range	15.00	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range
0 0011	$1.0 \times (1/3) \times f_{SAMPLE}$	Out of tunable filter range	13.33	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range
0 0100	$0.9 \times (1/3) \times f_{SAMPLE}$	Out of tunable filter range	12.00	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range
0 0101	$0.8 \times (1/3) \times f_{SAMPLE}$	Out of tunable filter range	10.67	17.33	Out of tunable filter range	Out of tunable filter range
0 0110	$0.75 \times (1/3) \times f_{SAMPLE}$	Out of tunable filter range	10.00	16.25	16.82	Out of tunable filter range
0 1000	$1.45 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	12.89	20.94	Out of tunable filter range	Out of tunable filter range
0 1001	$1.25 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	11.11	18.06	Out of tunable filter range	Out of tunable filter range
0 1010	$1.13 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	10.00	16.25	Out of tunable filter range	Out of tunable filter range
0 1011	$1.0 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	8.89	14.44	17.78	Out of tunable filter range
0 1100	$0.9 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	8.00	13.00	16.00	Out of tunable filter range
0 1101	$0.8 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	11.56	14.22	Out of tunable filter range
0 1110	$0.75 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	10.83	13.33	17.50
1 0000	$1.45 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	9.67	15.71	Out of tunable filter range	Out of tunable filter range
1 0001	$1.25 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	8.33	13.54	16.67	Out of tunable filter range
1 0010	$1.13 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	12.19	15.00	Out of tunable filter range
1 0011	$1.0 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	10.83	13.33	Out of tunable filter range
1 0100	$0.9 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	9.75	12.00	Out of tunable filter range
1 0101	$0.8 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	8.67	10.67	16.67
1 0110	$0.75 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	8.13	10.00	15.63

Table 12. SPI-Selectable Low-Pass Filter Cutoff Options for High Band Mode at Example Sampling Frequencies

Address 0x00F[7:3]	LPF Cutoff Frequency (MHz)	Sampling Frequency (MHz)				
		20.5	40	65	80	125
0 0000	$1.45 \times (1/3) \times f_{SAMPLE}$	Out of tunable filter range	19.33	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range
0 0001	$1.25 \times (1/3) \times f_{SAMPLE}$	Out of tunable filter range	16.67	27.08	Out of tunable filter range	Out of tunable filter range
0 0010	$1.13 \times (1/3) \times f_{SAMPLE}$	Out of tunable filter range	15.00	24.38	30.00	Out of tunable filter range
0 0011	$1.0 \times (1/3) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	21.67	26.67	Out of tunable filter range
0 0100	$0.9 \times (1/3) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	19.50	24.00	Out of tunable filter range
0 0101	$0.8 \times (1/3) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	17.33	21.33	Out of tunable filter range
0 0110	$0.75 \times (1/3) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	16.25	20.00	Out of tunable filter range
0 1000	$1.45 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	20.94	25.78	Out of tunable filter range
0 1001	$1.25 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	18.06	22.22	Out of tunable filter range
0 1010	$1.13 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	16.25	20.00	Out of tunable filter range
0 1011	$1.0 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	14.44	17.78	27.78
0 1100	$0.9 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	16.00	25.00
0 1101	$0.8 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	14.22	22.22
0 1110	$0.75 \times (1/4.5) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	20.83
1 0000	$1.45 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	15.71	19.33	Out of tunable filter range
1 0001	$1.25 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	13.54	16.67	26.04
1 0010	$1.13 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	15.00	23.44
1 0011	$1.0 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	20.83
1 0100	$0.9 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	18.75
1 0101	$0.8 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	16.67
1 0110	$0.75 \times (1/6) \times f_{SAMPLE}$	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	Out of tunable filter range	15.63

Tuning is normally off to avoid changing the capacitor settings during critical times. The tuning circuit is enabled through the SPI. It is disabled automatically after 512 cycles of the ADC sample clock. Initializing the tuning of the filter must be performed after initial power-up and after reprogramming of the filter cutoff scaling or the ADC sample rate. The tuning is initiated using Address 0x02B, Bit 6.

Four SPI-programmable settings allow users to vary the high-pass filter cutoff frequency as a function of the low-pass cutoff frequency. Two examples are shown in Table 13: an 8 MHz low-pass cutoff frequency and an 18 MHz low-pass cutoff frequency. In both cases, as the ratio decreases, the amount of rejection on the low end frequencies increases. Therefore, making the entire AAF frequency pass band narrow can reduce low frequency noise or maximize the dynamic range for harmonic processing.

Table 13. High-Pass Filter Cutoff Options

Addr. 0x02B[1:0] High-Pass Filter Cutoff	Ratio[1]	High-Pass Cutoff Frequency	
		Low-Pass Cutoff = 8 MHz	Low-Pass Cutoff = 18 MHz
00 (default)	12	670 kHz	1.5 MHz
01	9	890 kHz	2.0 MHz
10	6	1.33 MHz	3.0 MHz
11	3	2.67 MHz	6.0 MHz

[1] Ratio means low-pass filter cutoff frequency/high-pass filter cutoff frequency.

AAF/VGA Test Mode

For debugging and testing, there is a bypass switch to view the AAF output on the GPO2 and GPO3 pins. This mode can be enabled via Address 0x109, Bit 4. The differential AAF output allows only one channel to be accessed at a time. The dc output voltage is 1.5 V (or AVDD2/2), and the maximum ac output voltage is 2 V p-p.

ADC

The AD9674 uses a pipelined ADC architecture. The quantized output from each stage is combined into a 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and output clocks.

Clock Input Considerations

For optimum performance, clock the AD9674 sample clock inputs (CLK+ and CLK−) with a differential signal. This signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 39 shows the preferred method for clocking the AD9674. A low jitter clock source, such as the Valpey Fisher oscillator, VFAC3-BHL-50 MHz, is converted from a single-ended configuration to a differential configuration using an RF transformer.

The back to back Schottky diodes across the secondary transformer limit clock excursions into the AD9674 to approximately 0.8 V p-p differential. These diodes help prevent large voltage swings of the clock from feeding through to other portions of the AD9674, and they preserve the fast rise and fall times of the signal, which is critical to low jitter performance.

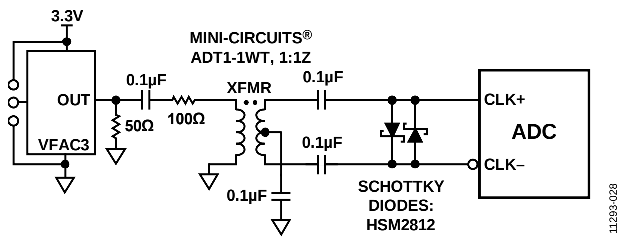

Figure 39. Transformer-Coupled Differential Clock

If a low jitter clock is available, another option is to ac couple a differential positive emitter coupled logic (PECL) signal to the sample clock input pins, as shown in Figure 40. Analog Devices,Inc., offers a family of clock drivers with excellent jitter performance,including the AD9516-0, AD9516-1, AD9516-2, AD9516-3, and AD9516-5 (these five devices are represented by AD9516-x in Figure 40, Figure 41, and Figure 42), as well as the AD9524.

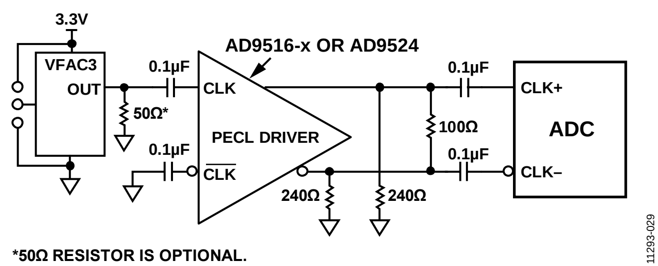

Figure 40. Differential PECL Sample Clock

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 41.

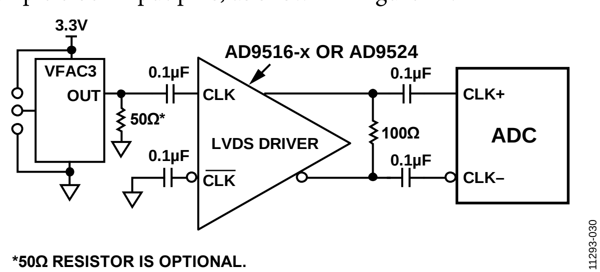

Figure 41. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, drive CLK+ directly from a CMOS gate, and bypass the CLK− pin to ground with a 0.1 µF capacitor (see Figure 42).

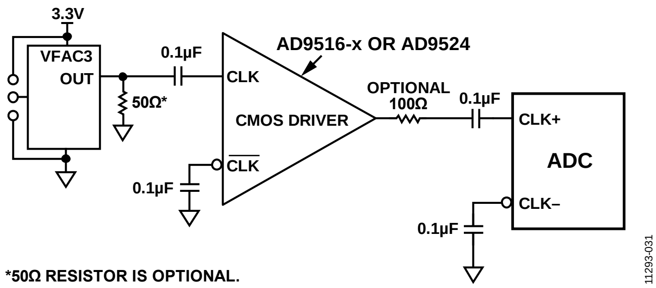

Figure 42. Single-Ended 1.8 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs can be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9674 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This feature allows a wide range of clock input duty cycles without affecting the performance of the AD9674. When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. When the DCS function is off, the dynamic range performance can be affected.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately eight clock cycles to allow the DLL to acquire and lock to the new rate.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated as follows:

$$SNR\ Degradation = 20 \times \log 10(1/2 \times \pi \times f_A \times t_J) \tag{7}$$

In Equation 7, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter (see Figure 43).

Treat the clock input as an analog signal when aperture jitter may affect the dynamic range of the AD9674. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators, such as the Valpey Fisher VFAC3 series, make the best clock sources. When the clock is generated from another type of source (by gating, dividing, or other methods), retime it by the original clock during the last step.

For more information on how jitter performance relates to ADCs, refer to the AN-501 Application Note and AN-756 Application Note.

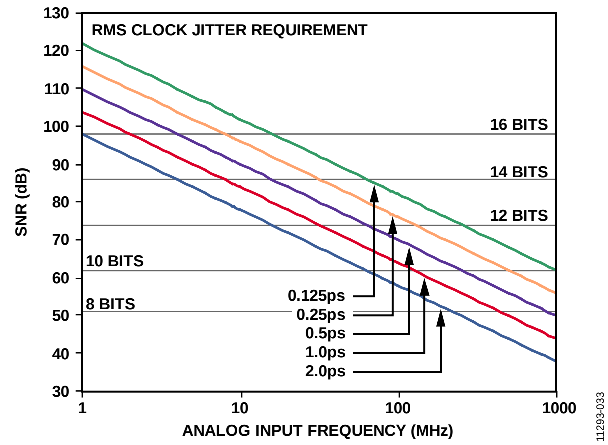

Figure 43. Ideal SNR vs. Analog Input Frequency and Jitter

Power Dissipation and Power-Down Mode

The power dissipated by the AD9674 is proportional to its sample rate. The digital power dissipation does not vary significantly because it is determined primarily by the DRVDD supply and the bias current of the LVDS output drivers. The AD9674 features scalable LNA bias currents (see Table 25, Address 0x012). The default LNA bias current settings are midhigh.

By asserting the PDWN pin high, the AD9674 is placed into power-down mode. In this state, the device dissipates at a maximum of 30 mW. During power-down, the LVDS output drivers are placed into a high impedance state. The AD9674 returns to normal operating mode when the PDWN pin is pulled low. This pin is only 1.8 V tolerant. To drive the PDWN pin from a 3.3 V logic level, insert a 1 kΩ resistor in series with this pin to limit the current.

By asserting the STBY pin high, the AD9674 is placed in standby mode. In this state, the device typically dissipates 630 mW. During standby, the entire device, except the internal references, powers down. The LVDS output drivers are placed into a high impedance state. This mode is well suited for applications that require power savings because it allows the device to be powered down when not in use and then to be quickly powered up. In addition, the time to power up the device is greatly reduced. The AD9674 returns to normal operating mode when the STBY pin is pulled low. This pin is only 1.8 V tolerant. To drive the STBY pin from a 3.3 V logic level, insert a 1 kΩ resistor in series with this pin to limit the current.

In power-down mode, low power dissipation is achieved by shutting down the reference, reference buffer, phase-locked loop (PLL), and biasing networks. The decoupling capacitors on VREF are discharged when entering power-down mode and must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in power-down mode: shorter cycles result in proportionally shorter wake-up times. To restore the device to full operation, approximately 375 μs is required when using the recommended 1 μF and 0.1 μF decoupling capacitors on the VREF pin and the 0.01 μF decoupling capacitors on the GAIN± pins. Most of this time is dependent on gain decoupling; higher value decoupling capacitors on the GAIN± pins result in longer wake-up times.

Other power-down options are available when using the SPI port interface. The user can individually power down each channel or place the entire device into standby mode. When fast wake-up times are required, standby mode allows the user to keep the internal PLL powered up. The wake-up time is slightly dependent on gain. To achieve a 2 μs wake-up time when the device is in standby mode, apply 0.8 V to the GAIN± pins.

Power and Ground Connection Recommendations

When connecting power to the AD9674, use two separate 1.8 V supplies: one for analog (AVDD1) and one for digital (DRVDD). When only one 1.8 V supply is available, route it to the AVDD1 pin first, tap it off, and isolate it with a ferrite bead or a filter choke preceded by decoupling capacitors for the DRVDD pin.

The DVDD pin can be tied to the 1.8 V DRVDD supply. When this is done, route the DVDD supply first, tap it off, and isolate it with a ferrite bead or filter choke preceded by decoupling capacitors for the DRVDD pin. It is not recommended to use the same supply for AVDD1, DVDD, and DRVDD to avoid noise issues. For compatibility with the AD9674 or for lower power operation, the DVDD pin can be tied to 1.4 V.

To cover both high and low frequencies, use several decoupling capacitors on all supplies. Locate these capacitors close to the point of entry at the PCB level and close to the device, with minimal trace lengths.

When using the AD9674, a single PCB ground plane is sufficient. With proper decoupling and smart partitioning of the analog, digital, and clock sections of the PCB, optimum performance is easily achievable.

Advanced Power Control

For an ultrasound system, not all channels are needed during all scanning periods. The POWER_START and POWER_STOP values in the vector profile can be used to delay the channel startup and turn the channel off after a certain number of samples. These counters are relative to TX_TRIG±. The analog circuitry must power up before the digital circuitry. The analog circuitry must power up (POWER_SETUP) before POWER_START is set up in Register 0x112 (see Table 25).

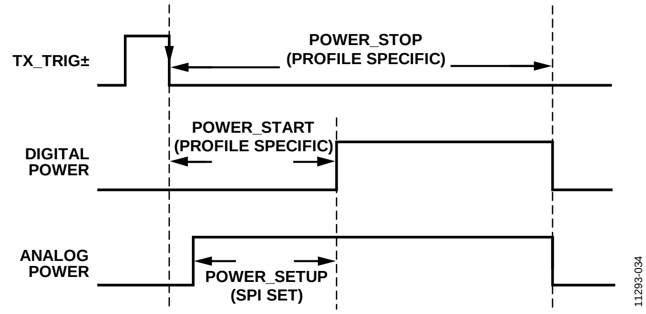

Figure 44. Power Sequencing

Digital Outputs and Timing

The AD9674 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This setting can be changed to a low power, reduced signal option similar to the IEEE 1596.3 standard via the SPI using Address 0x015, Bit 7. This LVDS standard can further reduce the overall power dissipation of the device by approximately 36 mW.

The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver.

The AD9674 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point to point network topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. No far-end receiver termination and poor differential trace routing may result in timing errors. The trace length must be no longer than 24 inches; keep the differential output traces close together and at equal lengths.

Figure 45 and Figure 46 show an example of the LVDS output using the ANSI-644 standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths of less than 24 inches on standard FR-4 material. Figure 47 and Figure 48 show an example of the trace lengths exceeding 24 inches on standard FR-4 material. Notice that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position. Therefore, the user must determine whether the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches.

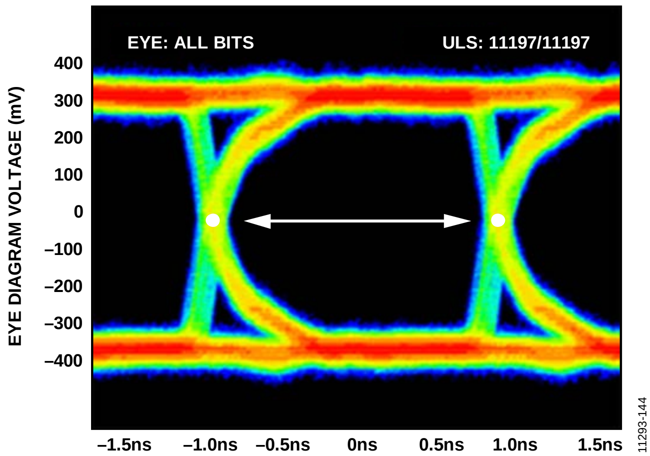

Figure 45. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Less Than 24 Inches on Standard FR-4

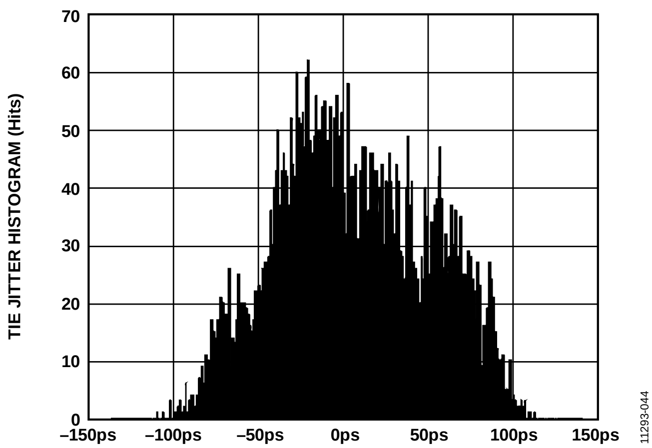

Figure 46. TIE Jitter Histogram for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Less Than 24 Inches on Standard FR-4

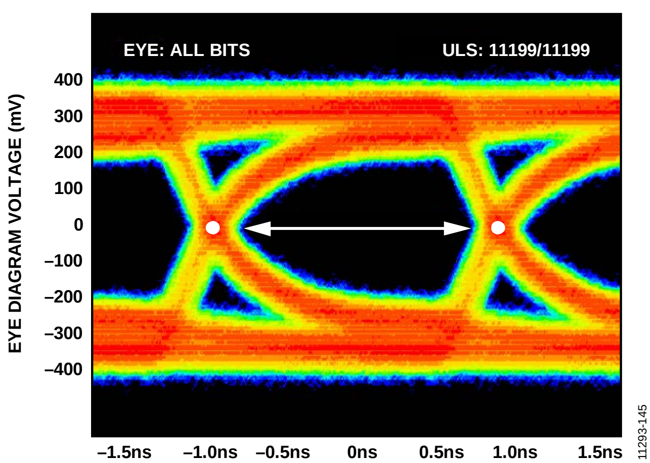

Figure 47. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Greater Than 24 Inches on Standard FR-4

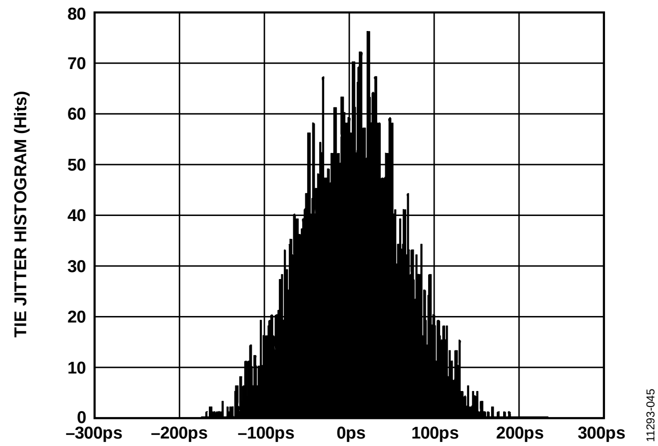

Figure 48. TIE Jitter Histogram for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Greater Than 24 Inches on Standard FR-4

Additional SPI options let the user further increase the internal current of all eight outputs to drive longer trace lengths. Even though this produces sharper rise and fall times on the data edges, increasing the internal current is less prone to bit errors and improves frequency distribution. The power dissipation of the DRVDD supply increases when this option is used.

In applications that require increased drive current, Address 0x015 allows the user to adjust the drivers from 2 mA to 3.72 mA. Note that this feature requires Bit 3 of Address 0x015 to be set to 1. The drive current can be adjusted for both ANSI-644 and IEEE 1596.3 (low power) mode. See Table 25 for more details.

The format of the output data is twos complement by default. Table 14 provides an example of the output coding format. To change the output data format to twos complement, see the Memory Map section.

Table 14. Digital Output Coding with RF Decimator Bypassed, Digital HPF Bypassed

Code	(VIN+) − (VIN−), Input Span = 2 V p-p (V)	Digital Output Mode: Twos Complement (D13 to D0)
16384	+1.00	01 1111 1111 1111
8192	0.00	00 0000 0000 0000
8191	−0.000488	11 1111 1111 1111
0	−1.00	10 0000 0000 0000

Digital data from each channel is serialized based on the number of lanes that are enabled (see Table 25). The maximum data rate for each serial output lane is 1 Gbps. For one channel per lane with a 14-bit data stream and ADC sample clock of 70 MHz, the output data rate is 980 Mbps (14 bits × 70 MHz = 980 Mbps) with the RF decimator bypassed, and digital HPF bypassed. For higher sample rates, enabling the RF decimator is required.

Two output clocks are provided to assist in capturing data from the AD9674. The digital clock outputs (DCO±) are used to clock the output data and are equal to seven times the sampling clock rate in 14-bit mode with the RF decimator bypassed and digital HPF bypassed.

Data is clocked out of the AD9674 and must be captured on the rising and falling edges of DCO±, which support double data rate (DDR) capturing. The frame clock outputs (FCO±) signal the start of a new output byte and are equal to the sampling clock rate.

A 12-, 14-, or 16-bit serial stream can also be initiated from Address 0x021, Bits[1:0]. The user can implement different serial streams and test device compatibility with lower and higher resolution systems using these modes.

When using the SPI, all the data outputs can also invert from their nominal state by setting Bit 2 in the output mode register (Address 0x014). This feature is not to be confused with inverting the serial stream to an LSB first mode. In default mode, as shown in Figure 2, the MSB is represented first in the data output serial stream. However, using Address 0x000, Bit 6, this order can be inverted so that the LSB is represented first in the data output serial stream.

Digital Output Test Patterns

Nine digital output test pattern options can be initiated through the SPI using Address 0x0D. These options are useful when validating receiver capture and timing. See Table 16 for the output test mode bit sequencing options. Some test patterns have two serial sequential words and can be alternated in various ways depending on the test pattern chosen. Note that some patterns may not adhere to the data format select option. In addition, custom user defined test patterns can be assigned in the user pattern registers (Address 0x019 through Address 0x020). All test mode options except the pseudonoise (PN) sequence short and PN sequence long can support 8- to 14-bit word lengths to verify data capture to the receiver.

The PN sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ bits, or 511 bits. A description of the PN sequence short pattern and how it is generated can be found in Section 5.1 of the ITU-T O.150 (05/96) standard. However, the PN sequence long pattern differs from the ITU-T O.150 (05/96) standard because it begins with a specific value instead of 1s (see Table 15 for the initial values).

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ bits, or 8,388,607 bits. A description of the PN sequence long pattern and how it is generated can be found in Section 5.6 of the ITU-T O.150 (05/96) standard. The PN sequence long pattern differs from the standard, however, because the starting value of the pattern is a specific value rather than a value of only 1s and the AD9674 inverts the bit stream (see Table 15 for the initial values). The output sample size depends on the selected bit length.

Table 15. PN Sequence Initial Values

Sequence	Initial Value	First Three Output Samples (MSB First, 16-Bit)
PN Sequence Short	0x092	0x496F, 0xC9A9, 0x980C
PN Sequence Long	0x003	0xFF5C, 0x0029, 0xB80A

See the Memory Map section for information on how to change these additional digital output timing features through the SPI.

SDIO Pin

The SDIO pin is required to operate the SPI. The pin has an internal 30 kΩ pull-down resistor that pulls this pin low and is only 1.8 V tolerant. If applications require that this pin be driven from a 3.3 V logic level, insert a 1 kΩ resistor in series with this pin to limit the current.

SCLK Pin

The SCLK pin is required to operate the SPI. The pin has an internal 30 kΩ pull-down resistor that pulls this pin low and is only 1.8 V tolerant. To drive the SCLK pin from a 3.3 V logic level, insert a 1 kΩ resistor in series with this pin to limit the current.

CSB Pin

The CSB pin is required to operate the SPI. The pin has an internal 70 kΩ pull-up resistor that pulls this pin high and is only 1.8 V tolerant. To drive the CSB pin from a 3.3 V logic level, insert a 1 kΩ resistor in series with this pin to limit the current.

RBIAS Pin

To set the internal core bias current of the ADC, place a resistor nominally equal to 10.0 kΩ to ground at the RBIAS pin. Using a resistor other than the recommended 10.0 kΩ resistor for RBIAS degrades the performance of the device. Therefore, it is imperative that at least a 1% tolerance on this resistor be used to achieve consistent performance.

VREF Pin

A stable and accurate 0.5 V voltage reference is built into the AD9674. This voltage reference is gained up internally by a factor of 2, setting VREF to 1.0 V, which results in a full-scale differential input span of 2.0 V p-p for the ADC. VREF is set internally by default, but the VREF pin can be driven externally with a 1.0 V reference to achieve more accuracy. However, the AD9674 does not support ADC full-scale ranges less than 2.0 V p-p.

When applying the decoupling capacitors to the VREF pin, use ceramic, low equivalent series resistance (ESR) capacitors. Ensure that these capacitors are close to the reference pin and on the same layer of the PCB as the AD9674. The VREF pin must have both a 0.1 µF capacitor and a 1 µF capacitor that are connected in parallel to the analog ground. These capacitor values are recommended for the ADC to properly settle and acquire the next valid sample.

Table 16. Flexible Output Test Modes

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Resolution Select
0000	Off (default)	Not applicable	Not applicable	Not applicable
0001	Midscale short	10 0000 0000 0000	Same	Yes
0010	Positive full-scale short	11 1111 1111 1111	Same	Yes
0011	Negative full-scale short	00 0000 0000 0000	Same	Yes
0100	Checkerboard	10 1010 1010 1010	01 0101 0101 0101	No
0101	PN sequence long	Not applicable	Not applicable	Yes
0110	PN sequence short	Not applicable	Not applicable	Yes
0111	One-word/zero-word toggle	11 1111 1111 1111	00 0000 0000 0000	No
1000	User input	Address 0x019 and Address 0x01A	Address 0x01B and Address 0x01C	No
1111	Ramp output	00 0000 0000 0000	00 0000 0000 0001	Yes

General-Purpose Output Pins

The general-purpose output pins, GPO0, GPO1, GPO2 and GPO3, can be used in a system to provide programmable inputs to other chips in the system. The value of each pin is set via Address 0x00E to either Logic 0 or Logic 1 (see Table 25).

Chip Address Pins

The chip address pins can be used to address individual AD9674 chips among multiple chips in a system. The chip address mode is enabled using Address 0x115, Bit 5 (see Table 25). If the value written to Bits[4:0] matches the value on the chip address bit pins (ADDR4 to ADDR0]), the device is selected and any subsequent SPI writes or reads to addresses indicated as chip registers are written only to that device. If chip address mode is disabled, all addresses can be written to regardless of the value on the address pins.

ANALOG TEST SIGNAL GENERATION

The AD9674 can generate analog test signals that can be switched to the input of the LNA of each channel to be used for channel gain calibration. The test signal amplitude at the LNA output is dependent on LNA gain, as shown in Table 17.

Table 17. Test Signal Fundamental Amplitude at LNA Output

Address 0x116, Bits[3:2], Analog Test Tones	LNA Gain 15.6 dB	LNA Gain 17.9 dB	LNA Gain 21.6 dB
00 (default)	80 mV p-p	98 mV p-p	119 mV p-p
01	160 mV p-p	196 mV p-p	238 mV p-p
10	320 mV p-p	391 mV p-p	476 mV p-p

The test signal amplitude at the input to the ADC can be calculated given the LNA gain, attenuator control voltage, and the PGA gain.

Table 18 and Table 19 give example calculations.

Table 18. Test Signal Fundamental Amplitude at ADC Input, VGAIN = 0 V, PGA Gain = 21 dB

Address 0x116, Bits[3:2], Analog Test Tones	LNA Gain 15.6 dB	LNA Gain 17.9 dB	LNA Gain 21.6 dB
00 (default)	−29 dBFS	−28 dBFS	−26 dBFS
01	−23 dBFS	−22 dBFS	−20 dBFS
10	−17 dBFS	−16 dBFS	−14 dBFS

Table 19. Test Signal Fundamental Amplitude at ADC Input, V_{GAIN} = 0 V, PGA Gain = 30 dB

Address 0x116, Bits [3:2], Analog Test Tones	LNA Gain 15.6 dB	LNA Gain 17.9 dB	LNA Gain 21.6 dB
00 (default)	−20 dBFS	−19 dBFS	−17 dBFS
01	−14 dBFS	−13 dBFS	−11 dBFS
10	−8 dBFS	−7 dBFS	−5 dBFS

CW DOPPLER OPERATION

Each channel of the AD9674 includes an I/Q demodulator. Each demodulator has an individual programmable phase shifter. The I/Q demodulator is ideal for phased array beamforming applications in medical ultrasound. Each channel can be programmed for 16 phase settings/360° (or 22.5°/step), selectable via the SPI port. The device has a RESET± input that is used to synchronize the LO dividers of each channel. If multiple AD9674 devices are used, a common reset across the array ensures a synchronized phase for all channels. Internal to the AD9674, the individual Channel I and Channel Q outputs are current summed. If multiple AD9674 devices are used, the I and Q outputs from each AD9674 can be current summed and converted to a voltage using an external transimpedance amplifier.

Quadrature Generation

The internal 0° and 90° LO phases are digitally generated by a divide by M logic circuit, where M is 4, 8, or 16. The internal divider is selected via Address 0x02E, Bits[2:1] (see Table 25). The divider is dc-coupled and inherently broadband; the maximum LO frequency is limited only by its switching speed. The duty cycle of the quadrature LO signals must be as close to 50% as possible for the 4LO and 8LO modes. The 16LO mode does not require a 50% duty cycle. Furthermore, the divider is implemented so the multiple LO signal reclocks the final flip flops that generate the internal LO signals and, therefore, minimizes noise introduced by the divide circuitry.

For optimum performance, the MLO± input is driven differentially, as on the AD9670 evaluation board. The common-mode voltage on each pin is approximately 1.2 V with the nominal 3 V supply. It is important to ensure that the MLO± source has very low phase noise (jitter), a fast slew rate, and an adequate input level to obtain optimum performance of the CW signal chain.

Beamforming applications require a precise channel-to-channel phase relationship for coherence among multiple channels. The RESET± input is provided to synchronize the LO divider circuits in different AD9674 devices when they are used in arrays. The RESET± input is a synchronous edge triggered input that resets the dividers to a known state after power is applied to multiple AD9674 devices.

The RESET± signal can be either a continuous signal or a single pulse, and can be either synchronized with the MLO± clock edge (recommended) or it can be asynchronous. If a continuous signal is used for the RESET±, it must be at the LO rate. For a synchronous RESET±, the device can be configured to sample the RESET± signal with either the falling or rising edge of the MLO± clock, which makes it easier to align the RESET± signal with the opposite MLO± clock edge. Register 0x02E is used to configure the RESET± signal behavior. Synchronize the RESET± input to the MLO± input. Accurate channel to channel phase matching can be achieved via a common clock on the RESET± input when using more than one AD9674 device.

I/Q Demodulator and Phase Shifter

The I/Q demodulators consist of double balanced, harmonic rejection, passive mixers. The RF input signals are converted into currents by transconductance stages that have a maximum differential input signal capability matching the full-scale LNA output. These currents are then presented to the mixers, which convert them to baseband (RF − LO) and 2× RF (RF + LO). The signals are phase shifted according to the codes that are programmed into the SPI latch (see Table 20). The phase shift function is an integral part of the overall circuit. The phase shift listed in Table 20 is defined as being between the baseband I or Q channel outputs. As an example, for a common signal applied to a pair of RF inputs to an AD9674, the baseband outputs are in phase for matching phase codes. However, if the phase code for Channel 1 is 0000 and the phase code for Channel 2 is 0001, Channel 2 leads Channel 1 by 22.5°.

Table 20. Phase Select Code for Channel to Channel Phase Shift

Φ Shift	I/Q Demodulator Phase (Address 0x02D, Bits[3:0])
0°	0000
22.5°	0001 (not valid in 4LO mode)
45°	0010
67.5°	0011 (not valid in 4LO mode)
90°	0100
112.5°	0101 (not valid in 4LO mode)
135°	0110
157.5°	0111 (not valid in 4LO mode)
180°	1000
202.5°	1001 (not valid in 4LO mode)
225°	1010
247.5°	1011 (not valid in 4LO mode)
270°	1100
292.5°	1101 (not valid in 4LO mode)
315°	1110
337.5°	1111 (not valid in 4LO mode)

DIGITAL RF DECIMATOR

The AD9674 contains digital processing capability. Each channel has two stages of processing available: RF decimator and HPF. For test purposes, the input to the decimator can be a test waveform. Normally, the input to the decimator is the output of the ADC. The output of the decimator and filter is sent to the serializer for output formatting.

The maximum data rate of the serializer is 1000 MSPS. Therefore, if the sample rate of the ADC is greater than 65 MSPS, the RF decimator (fixed rate of 2) must be enabled. The ADC resolution is 14 bits. Saturation of the ADC is determined after the dc offset calibration to ensure maximum dynamic range.

VECTOR PROFILE

To minimize the time needed to reconfigure device settings while operating, the device supports configuration profiles. Up to 32 profiles can be stored in the device. A profile is selected by a 5-bit index. A profile consists of a 64-bit vector, as described in Table 21. Each parameter is concatenated to form the 64-bit profile vector. The profile memory starts at Address 0xF00 and ends at Address 0xFFF. The memory can be written in either stream mode or address selected data mode. However, the memory must be read using stream mode.

When writing or reading in stream mode while the SPI configuration is set to MSB first mode (default setting for Register 0x000), the write/read address must refer to the last register address, not the first one. For example, when writing or reading the first profile that spans the address space between 0xF00 and 0xF07, and the SPI port is configured as MSB first, the referenced address must be 0xF07 to allow reading from or writing to the 64-bit profile in MSB mode. For more information about stream mode, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI.*

A buffer in the device stores the current profile data. When the profile index is written in Register 0x10C, the selected profile is read from memory and stored in the current profile buffer. The profile memory is read/written in the SPI clock domain. After the SPI writes the profile index value, it takes four SPI clock cycles to read the profile from RAM and store it in the current profile buffer. If the SPI is in LSB mode, these additional SPI clock cycles are provided when the profile index register is written. If the SPI is in MSB mode, an additional byte needs to be read or written to update the profile buffer.

Updating the profile memory does not affect the data in the profile buffer. The profile index register must be written to cause a refresh of the current profile data, even if the profile index register is written with the same value.

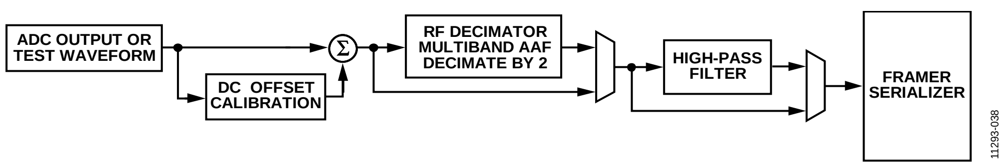

Figure 49. Simplified Block Diagram of a Single Channel of RF Decimator

Table 21. Profile Definition

Field	Bits	Description
Reserved	32	Reserved
HPF bypass	1	Digital HPF bypass 0 = disable (filter enabled) 1 = enable (filter bypassed)
POWER_START	15	ADC clock cycles counted from TX_TRIG± when the active channels are powered up 0x0000 = 0 clock cycles 0x0001 = 1 clock cycle … 0x7FFF = 32,767 clock cycles
Reserved	1	Reserved
POWER_STOP	15	ADC clock cycles counted from TX_TRIG± when the active channels are powered down 0x0000 = 0 clock cycles 0x0001 = 1 clock cycle … 0x7FFF = Continuous run mode

RF DECIMATOR

The input to the RF decimator is either the ADC output data or a test waveform, as described in the Digital Test Waveforms section. The test waveforms are enabled per channel using Address 0x11A (see Table 25).

DC Offset Calibration

DC offset can be reduced through a manual system calibration process. The dc offset of every channel in the system is measured, followed by setting a calibration value in Address 0x110 and Address 0x111. Note that these registers are both chip and local addresses, meaning the registers are accessed using the chip address and device index. The dc offset calibration can be bypassed using Address 0x10F, Bits[2:0].

Multiband AAF and Decimate by 2

The multiband filter is a finite impulse response (FIR) filter. It is programmable with low or high band filtering. The filter requires 11 input samples to populate the filter. The decimation rate is fixed at 2×. Therefore, the decimation frequency is $f_{DEC} = f_{SAMPLE}/2$. Figure 50 and Figure 51 show the frequency response of the filter, depending on this mode. Figure 50 shows the attenuation amplitude over the Nyquist frequency range. Figure 51 shows the pass band response as nearly flat.

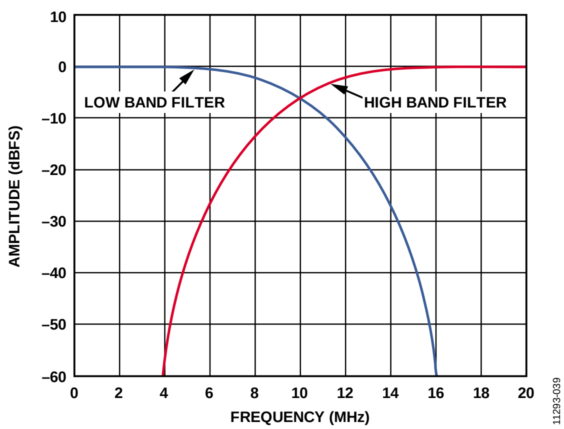

Figure 50. AAF Frequency Response (Frequency Scale Assumes $f_{ADC} = 2 \times f_{DEC} = 40$ MHz)

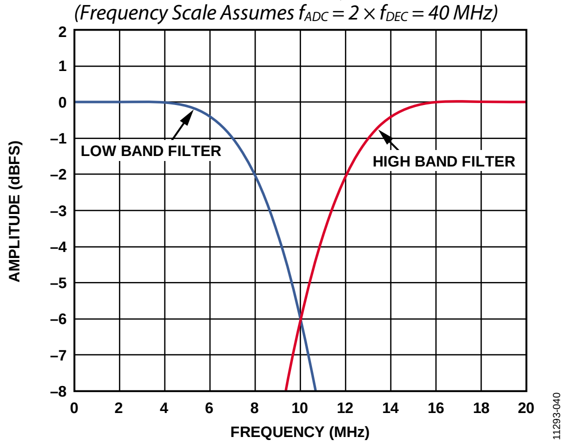

Figure 51. AAF Frequency Response Zoomed In (Frequency Scale Assumes $f_{ADC} = 2 \times f_{DEC} = 40$ MHz)

High-Pass Filter

A second-order Butterworth, high-pass, infinite impulse response (IIR) filter can be applied after the RF decimator. The IIR filter has a settling time of 2.5 µs and a cutoff frequency of 700 kHz for an encode clock of 50 MHz. Therefore, if the ADC clock is 50 MHz, the first 125 samples (2.5 µs/0.02 µs) must be ignored. The filter can be bypassed or enabled in the vector profile if the filter is enabled using Address 0x113, Bit 5. If the filter is bypassed by setting Address 0x113, Bit 5, to 1, the filter cannot be enabled from the vector profile.

DIGITAL TEST WAVEFORMS

Digital test waveforms can be used in the digital processing block instead of the ADC output. To enable digital test waveforms, use Address 0x11B. Each channel can be individually enabled in Address 0x11A.

Waveform Generator

For testing and debugging, a programmable waveform generator can be used in place of ADC data. The waveform generator can vary offset, amplitude, and frequency. The generator uses the ADC sample frequency, f_{SAMPLE}, and ADC full-scale amplitude, $A_{FULL\text{-}SCALE}$, as references. The values are set in Address 0x117, Address 0x118, and Address 0x119 (see Table 25).

$$x = C + A \times \sin(2 \times \pi \times N) \tag{8}$$

$$N = \frac{f_{SAMPLE} \times n}{64}\text{, see Address 0x117} \tag{9}$$

$$A = \frac{A_{FULL-SCALE}}{2^x}\text{, see Address 0x118} \tag{10}$$

$$C = A_{FULL\text{-}SCALE} \times a \times 2^{-(13-b)}\text{, see Address 0x119} \tag{11}$$

Channel ID and Ramp Generator

In Channel ID test mode, the output is a concatenated value. Bits[6:0] are a ramp. Bit 7 is reserved as 0. Bits[10:8] are the channel ID such that Channel A is coded as 000 and Channel B is 001. Bits[15:11] compose the chip address.

DIGITAL BLOCK POWER SAVING SCHEME

To reduce power consumption in the digital block after the ADC, the RF decimator and filter start in an idle state after running the chip (Register 0x008, Bits[2:0] = 000). The digital block only switches to a running state when the negative edge of the TX_TRIG signal pulse is detected, or with a software TX_TRIG signal write (Register 0x10C, Bit 5 = 1).

To put the digital block back into the idle state (while the rest of the chip is still running) and save power, raise the TX_TRIG signal high or write to the profile index (Register 0x10C, Bits[0:4]). The digital block will also switch to the idle state if the power stop expires when using the advanced power control feature. Figure 52 illustrates the digital block power saving scheme.

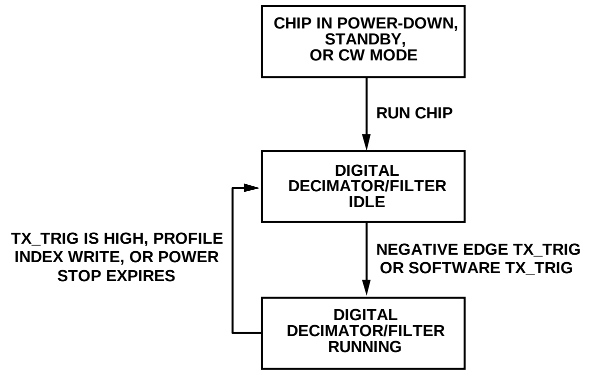

Figure 52. Digital Block Power Saving Scheme

SERIAL PORT INTERFACE (SPI)

The AD9674 SPI allows the user to configure the signal chain for specific functions or operations through the structured register space provided inside the chip. The SPI offers the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, as documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

The SCLK, SDIO, and CSB pins define the SPI (see Table 22). The SCLK (serial clock) pin synchronizes the read and write data presented to the device. The SDIO pin is a dual-purpose pin that allows data to be sent to and read from the internal memory map registers of the device. The CSB pin is an active low control that enables or disables the read and write cycles.

Table 22. Serial Port Pins

Pin	Function
SCLK	Serial clock. Serial shift clock input. SCLK is used to synchronize serial interface reads and writes.
SDIO	Serial data input/output. Dual-purpose pin that typically serves as an input or an output, depending on the instruction sent and the relative position in the timing frame.
CSB	Chip select bar (active low). This control gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing sequence. During the instruction phase, a 16-bit instruction is transmitted, followed by one or more data bytes, which is determined by the W0 and W1 bit fields. An example of the serial timing and definitions are shown in Figure 54 and Table 23.

During normal operation, CSB signals to the AD9674 that SPI commands must be received and processed. When CSB is brought low, the device processes SCLK and SDIO to execute instructions. Normally, CSB remains low until the communication cycle is complete. However, if connected to a slow device, CSB can be brought high between bytes, allowing older microcontrollers enough time to transfer data into shift registers. CSB can be stalled when transferring one, two, or three bytes of data. When W0 and W1 are set to 11, the device enters streaming mode and continues to process data, either reading or writing, until CSB is taken high to end the communication cycle. This mode allows complete memory transfers without the need for additional instructions. Regardless of the mode, if CSB is taken high in the middle of a byte transfer, the SPI state machine is reset, and the device waits for a new instruction.

The SPI port can be configured to operate in different manners. CSB can also be tied low to enable 2-wire mode. When CSB is tied low, SCLK and SDIO are the only pins required for communication.

Although the device is synchronized during power-up, caution must be exercised when using 2-wire mode to ensure that the serial port remains synchronized with the CSB line. When operating in 2-wire mode, it is recommended that a 1-, 2-, or 3-byte transfer be used exclusively. Without an active CSB line, streaming mode can be entered but not exited.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or LSB first mode. MSB first mode is the default at power-up and can be changed by adjusting the configuration register (Address 0x00). For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 22 constitute the physical interface between the programming device and the serial port of the AD9674. The SCLK and CSB pins function as inputs when using the SPI. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

If multiple SDIO pins share a common connection, ensure that proper V_{OH} levels are met. Figure 53 shows the number of SDIO pins that can be connected together and the resulting V_{OH} levels, assuming the same load for each AD9674.

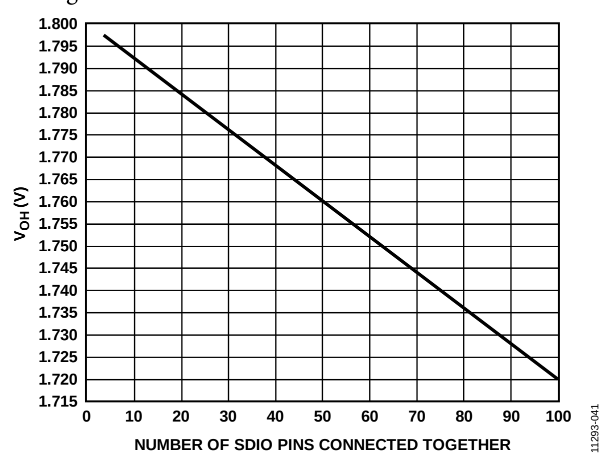

Figure 53. SDIO Pin Loading

This interface is flexible enough to be controlled either by serial programmable read-only memories (PROMs) or by PIC microcontrollers, which provide the user with an alternative to a full SPI controller for programming the device (see the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI®) Boot Circuit*).

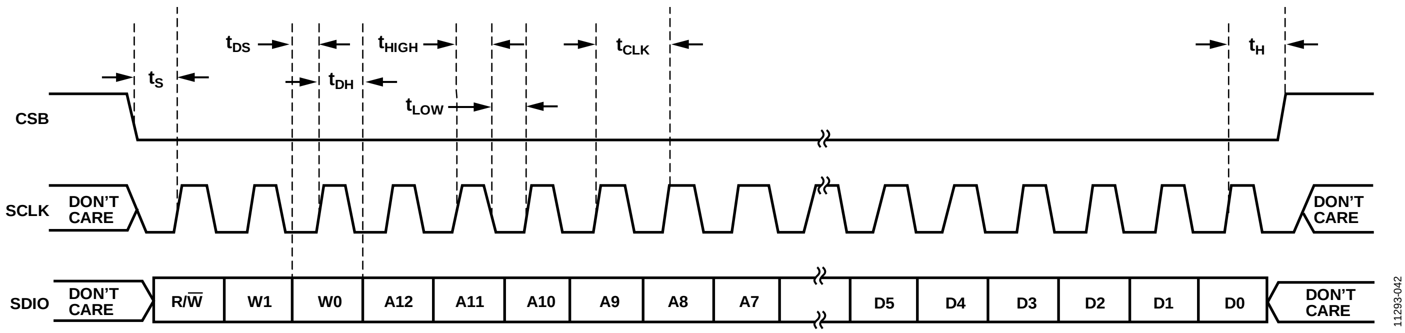

Figure 54. Serial Timing Details

Table 23. Serial Timing Definitions

Parameter	Timing (ns min)	Description
t_{DS}	12.5	Setup time between the data and the rising edge of SCLK
t_{DH}	5	Hold time between the data and the rising edge of SCLK
t_{CLK}	40	Period of the clock
t_{S}	5	Setup time between CSB and SCLK
t_{H}	2	Hold time between CSB and SCLK
t_{HIGH}	16	Minimum period that SCLK must be in a logic high state
t_{LOW}	16	Minimum period that SCLK must be in a logic low state
t_{EN_SDIO}	15	Minimum time for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 54)
t_{DIS_SDIO}	15	Minimum time for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 54)

MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into two sections: the chip configuration register map (Address 0x000 to Address 0x1A1) and the profile register map (Address 0xF00 to Address 0xFFF). Registers that are designated as local registers use the device index in Address 0x004 and Address 0x005 to determine to which channels of a device the command is applied. Registers that are designated as chip registers use the chip address mode in Address 0x115 to determine whether the device is to be updated by writing to the chip register.

The address hex column of Table 25 indicates the register address. The default value is shown in the default value column. The Bit 7 (MSB) column is the start of the default hexadecimal value given. For example, Address 0x009, the global clock register, has a default value of 0x01, meaning that Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 1, or 0000 0001 in binary. This setting is the default for the duty cycle stabilizer in the on condition.

For more information about the SPI memory map and other functions, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

RESERVED LOCATIONS

Do not write to undefined memory locations except when writing the default values suggested in this data sheet. Addresses that have values marked as 0 must be considered reserved and have a 0 written into their registers during power-up.

DEFAULT VALUES

After a reset, critical registers are automatically loaded with default values. These values are indicated in Table 25, where an X refers to an undefined feature.

LOGIC LEVELS

“Bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.” Similarly, “bit is cleared” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”

RECOMMENDED START-UP SEQUENCE

To save system power during programming, the AD9674 powers up in power-down mode. To start the device up and initialize the data interface, the SPI commands listed in Table 24 are recommended. At a minimum, the profile memory for an index of 0 must be written (Address 0xF00 to Address 0xF03). If additional profiles and coefficient memory are required, these can be written after Profile Memory 0.

Table 24. SPI Write Start-Up Sequence Example

Address	Value	Description
0x000	0x3C	Initiates SPI reset
0x002	0x0X (default)	Sets speed mode to 40 MHz
0x0FF	0x01	Enables speed mode change (required after Register 0x002 writes)
0x004	0x0F	Sets local registers to all channels
0x005	0x3F	Sets local registers to all channels
0x113	0x00	Bypasses RF decimator; enable digital HPF
0x011	0x06 (default)	Sets LNA gain = 21.6 dB, VGA gain = external, and PGA gain = 24 dB
0xF00	0xFF	Continuous run mode enabled; do not power down channels (POWER_STOP LSB)
0xF01	0x7F	Continuous run mode enabled; do not power down channels (POWER_STOP MSB)
0xF02	0x00	Powers up all channels 0 clock cycles after TX_TRIG± (POWER_STOP LSB)
0xF03	0x80	Digital high-pass bypassed (POWER_STOP MSB)
0x10C[1]	0x00 (default)	Sets the profile index (required after profile memory writes)
0x014	0x00	Sets output data format
0x008	0x00	TGC run mode[2]
0x021	0x05	14 bits, 8 lanes, frame clock output (FCO) covers entire frame
0x199	0x80	Enables automatic clocks per sample calculation
0x19B	0x50	Serial format
0x188	0x01	Enables start code
0x18B	0x27	Sets start code MSB
0x18C	0x72	Sets start code LSB
0x182	0x82	Autoconfigures PLL
0x10C[3]	0x20	Sets SPI TX_TRIG and profile index
0x00F	0x18 (default)	Sets low-pass filter cutoff frequency and bandwidth mode
0x02B	0x40	Sets analog LPF and HPF to defaults, tune filters[4]

[1] Setting the profile index requires an additional SPI write in SPI MSB mode before the chip runs to complete the current profile buffer update.
[2] Running the chip from full power-down mode requires 375 µs wake-up time, as listed in Table 3.
[3] Software TX_TRIG switches the demodulator/decimator digital block to a running state. The software TX_TRIG signal may not be needed if a hardware TX_TRIG signal is used to run the digital block.
[4] Tuning the filters requires 512 ADC clock cycles.

Table 25. Memory Map Registers

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Comments
Chip Configuration Registers											
0x000	CHIP_PORT_ CONFIG	0	LSB first: 0 = off (default), 1 = on	SPI reset: 0 = off (default), 1 = on	1	1	SPI reset: 0 = off (default), 1 = on	LSB first: 0 = off (default), 1 = on	0	0x18	Mirror nibbles so LSB first or MSB Mode I is set correctly regardless of shift mode. SPI reset reverts all registers (including LVDS registers), except Register 0x000, to their default values, and Register 0x000, Bit 2 and Bit 5 bits automatically clear.
f0x001	CHIP_ID	Chip ID, Bits[7:0] (AD9674 = 0xA8), default								0xA8	Default is unique chip ID, different for each device; read only register.
0x002	CHIP_GRADE	X	X	Speed mode, Bits[5:4] (identify device variants of chip ID): 00 = Mode I (40 MSPS) (default), 01 = Mode II (65 MSPS), 10 = Mode III (80 MSPS), 11 = Mode III (125 MSPS)		X	X	X	X	0x0X	Speed mode used to differentiate ADC speed power modes (must update Register 0x0FF after for the speed mode changes to take effect).
0x0FF	DEVICE_UPDATE	X	X	X	X	X	X	X	X	0x00	A write to Register 0x0FF (value does not matter) resets all default register values (analog and ADC registers only; not JESD204B ones and not Register 0x00 or Register 0x02, Bits[5:4]) if Register 0x02 has been previously written since the last reset/load of defaults.
0x004	DEVICE_INDEX_2	X	X	X	X	Data Channel H: 0 = off, 1 = on (default)	Data Channel G: 0 = off, 1 = on (default)	Data Channel F: 0 = off, 1 = on (default)	Data Channel E: 0 = off, 1 = on (default)	0x0F	Bits are set to determine which on-chip channel receives the next write command.
0x005	DEVICE_INDEX_1	X	X	Clock Channel DCO±: 0 = off, 1 = on (default)	Clock Channel FCO±: 0 = off, 1 = on (default)	Data Channel D: 0 = off, 1 = on (default)	Data Channel C: 0 = off, 1 = on (default)	Data Channel B: 0 = off, 1 = on (default)	Data Channel A: 0 = off, 1 = on (default)	0x3F	Bits are set to determine which on-chip channel receives the next write command.
0x008	GLOBAL_MODES	X	LNA input impedance: 0 = 6 kΩ (default), 1 = 3 kΩ	X	0	0	Internal power-down mode: 000 = chip run (TGC mode), 001 = full power-down (default), 010 = standby, 011 = reset all LVDS registers, 100 = CW Doppler mode (TGC is powered down)			0x01	Determines generic modes of chip operation (global).
0x009	GLOBAL_CLOCK	X	X	X	X	X	X	X	DCS: 0 = off, 1 = on (default)	0x01	Turns the internal DCS on and off (global).
0x00A	PLL_STATUS	PLL lock status: 0 = not locked (default), 1 = locked	X	X	X	X	X	X	X	0x00	Monitor PLL lock status (read only, global).

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Comments
0x00D	TEST_IO	User test mode: 0 = continuous, repeat user patterns (1, 2, 3, 4, 1, 2, 3, 4, …) (default), 1 = single clock cycle user patterns, then zeros (1, 2, 3, 4, 0, 0, …)	X	Reset PN long gen 0 = on, PN long running (default), 1 = off, PN long held in reset	Reset PN short gen: 0 = on, PN short running (default), 1 = off, PN short held in reset	Output test mode: 0000 = off (default), 0001 = midscale short, 0010 = positive full-scale short, 0011 = negative full-scale short, 0100 = checkerboard output, 0101 = PN sequence long, 0110 = PN sequence short, 0111 = one-word/zero-word toggle, 1000 = user input, 1001:1110 = reserved, 1111 = ramp output (see Table 16)				0x00	When register is set, the test data is placed on the output pins in place of normal data (local).
0x00E	GPO	X	X	X	X	GPO3 output: 0 = low (default); 1 = high	GPO2 output: 0 = low (default); 1 = high	GPO1 output: 0 = low (default): 1 = high	GPO0 output: 0 = low (default); 1 = high	0x00	Values placed on GPOx pins (global).
0x00F	FLEX_CHANNEL_INPUT	Filter cutoff frequency control: 00000 = 1.45 × (1/3) × f_{SAMPLE}, 00001 = 1.25 × (1/3) × f_{SAMPLE}, 00010 = 1.13 × (1/3) × f_{SAMPLE}, 00011 = 1.0 × (1/3) × f_{SAMPLE} (default), 00100 = 0.9 × (1/3) × f_{SAMPLE}, 00101 = 0.8 × (1/3) × f_{SAMPLE}, 00110 = 0.75 × (1/3) × f_{SAMPLE}, 00111 = reserved, 01000 = 1.45 × (1/4.5) × f_{SAMPLE}, 01001 = 1.25 × (1/4.5) × f_{SAMPLE}, 01010 = 1.13 × (1/4.5) × f_{SAMPLE}, 01011 = 1.0 × (1/4.5) × f_{SAMPLE}, 01100 = 0.9 × (1/4.5) × f_{SAMPLE}, 01101 = 0.8 × (1/4.5) × f_{SAMPLE}, 01110 = 0.75 × (1/4.5) × f_{SAMPLE}, 01111 = reserved, 10000 = 1.45 × (1/6) × f_{SAMPLE}, 10001 = 1.25 × (1/6) × f_{SAMPLE}, 10010 = 1.13 × (1/6) × f_{SAMPLE}, 10011 = 1.0 × (1/6) × f_{SAMPLE}, 10100 = 0.9 × (1/6) × f_{SAMPLE}, 10101 = 0.8 × (1/6) × f_{SAMPLE}, 10110 = 0.75 × (1/6) × f_{SAMPLE}, 1 0111 = reserved					Band mode: 0 = low (default, 8 MHz to 18 MHz), 1 = high (13.5 MHz to 30 MHz)	X	X	0x18	Antialiasing filter cutoff (global).
0x010	FLEX_OFFSET	X	X	1	0	0	0	0	0	0x20	Reserved.
0x011	FLEX_GAIN	Digital VGA gain control: 0000 = GAIN± pins enabled (default), 0001 = 0.0 dB (maximum gain, GAIN± pins disabled), 0010 = −3.5 dB, 0011 = −7.0 dB, …., 1110 = 45 dB 1111 = 45 dB				PGA gain: 00 = 21 dB, 01 = 24 dB (default), 10 = 27 dB, 11 = 30 dB		LNA gain: 00 = 15.6 dB, 01 = 17.9 dB, 10 = 21.6 dB (default)		0x06	LNA and PGA gain adjustment (global).
0x012	BIAS_CURRENT	X	X	X	X	1	PGA bias: 0 = 100% (default), 1 = 60%	LNA bias: 00 = high, 01 = midhigh (default), 10 = midlow, 11 = low		0x09	LNA bias current adjustment (global).
0x013	RESERVED_13	0	0	0	0	0	0	0	0	0x00	Reserved.
0x014	OUTPUT_MODE	X	X	X	Output data enable: 0 = enable (default), 1 = disable	X	Output data invert: 0 = disable (default), 1 = enable	Output data format: 00 = offset binary, 01 = twos complement (default), 10 = gray code, 11 = reserved		0x01	Data output modes (local).
0x015	OUTPUT_ADJUST	LVDS output standard: 0 = ANSI-644 (default), 1 = IEEE 1596.3 (low power)	1	1	0	LVDS drive strength enable: 0 = disable (default), 1 = enable	LVDS drive current: 000 = 3.72 mA, 001 = 3.5 mA (default), 010 = 3.30 mA, 011 = 2.96 mA, 100 = 2.82 mA, 101 = 2.57 mA, 110 = 2.27 mA, 111 = 2.0 mA (reduced range)			0x61	Data output levels (global).

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Comments
0x016	FLEX_OUTPUT_ PHASE	X	X	0	DCO signal invert: 0 = disable (default), 1 = enable	X	X	DCO signal phase adjust with respect to DOUT: 00 = +90° (default), 01 = 0°, 10 = 0°, 11 = −90°		0x00	DCO signal inversion and coarse phase adjustment (global).
0x017	FLEX_OUTPUT_ DELAY	DCO signal delay enable: 0 = disable (default), 1 = enable	X	X	DCO signal clock delay: 00000: 100 ps (default), 00001 = 200 ps, 00010 = 300 ps, …, 11101 = 3.0 ns, 11110 = 3.1 ns, 11111 = 3.2 ns					0x00	DCO signal delay (global).
0x018	RESERVED_018	X	X	X	X	X	1	0	0	0x04	Reserved (global).
0x019	USER_ PATT1_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-Defined Pattern 1, LSB (global).
0x01A	USER_ PATT1_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-Defined Pattern 1, MSB (global).
0x01B	USER_ PATT2_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-Defined Pattern 2, LSB (global).
0x01C	USER_ PATT2_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-Defined Pattern 2, MSB (global).
0x01D	USER_ PATT3_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-Defined Pattern 3, LSB (global).
0x01E	USER_ PATT3_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-Defined Pattern 3, MSB (global).
0x01F	USER_ PATT4_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-Defined Pattern 4, LSB (global).
0x020	USER_ PATT4_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-Defined Pattern 4, MSB (global).
0x021	FLEX_ SERIAL_CTRL	0	FCO signal invert: 0 = not inverted (default), 1 = inverted	Lane mode: 00 = 1-channel/lane (8 lanes) (default), 01 = 2-channel/lane (4 lanes), 10 = 4-channel/lane (2 lanes), 11 = 8-channel/lane (1 lane)		Lane low rate: 0 = normal (default), 1 = low sample frequency (<32 MHz)	X	Output word length: 00 = 12 bits (default), 01 = 14 bits, 10 = 16 bits, 11 = reserved		0x00	LVDS control (global).
0x022	SERIAL_ CH_STAT	X	X	X	X	X	X	X	Channel power-down: 1 = on, 0 = off (default)	0x00	Used to power down individual channels (local).
0x02B	FLEX_FILTER	X	Enables automatic low-pass tuning: 1 = on (self clearing)	X	X	Bypass analog HPF: 0 = off (default), 1 = on	X	Analog high-pass filter cutoff: 00 = f_{LP}/12 (default), 01 = f_{LP}/9, 10 = f_{LP}/6, 11 = f_{LP}/3		0x00	Filter cutoff (global); (f_{LP} = low-pass filter cutoff frequency in MSPS).
0x02C	LNA_TERM	X	X	X	X	X	X	LO-x, LOSW-x connection: 00 = R_{FB1} (default), 01 = (R_{FB1}||R_{FB2}), 10 = R_{FB2}, 11 = ∞		0x00	LNA active termination/ input impedance (global).

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Comments
0x02D	CW_ENABLE_ PHASE	X	X	X	CW Doppler channel enable: 0 = off (default), 1 = on	I/Q demodulator phase: 0000 = 0° (default), 0001 = 22.5° (not valid for 4LO mode), 0010 = 45°, 0011 = 67.5° (not valid for 4LO mode), 0100 = 90°, 0101 = 112.5° (not valid for 4LO mode), 0110 = 135°, 0111 = 157.5° (not valid for 4LO mode), 1000 = 180°, 1001 = 202.5° (not valid for 4LO mode), 1010 = 225°, 1011 = 247.5° (not valid for 4LO mode), 1100 = 270°, 1101 = 292.5° (not valid for 4LO mode), 1110 = 315°, 1111 = 337.5° (not valid for 4LO mode)				0x00	Phase of demodulators (local, chip).
0x02E	CW_LO_MODE	Partially enable LVDS during CW 0: LVDS link disabled during CW (default), 1: LVDS link partially enabled during CW, PLL, FCO, and DCO are enabled, while LVDS data drivers are disabled (switching activity can degrade CW performance)	RESET± with MLO± clock edge: 0 = synchronous (default), 1 = asynchronous	Synchronous RESET± sampling MLO± clock edge: 0 = falling (default), 1 = rising	RESET± signal polarity: 0 = active high (default), 1 = active low	MLO± and RESET± buffer enable (in all modes except CW mode): 0 = power down (default), 1 = enable	LO mode 00X = 4LO, third to fifth odd harmonic rejection (default) 010 = 8LO, third to fifth odd harmonic rejection 011 = 8LO, third to 13th odd harmonic rejection 100 = 16LO, third to fifth odd harmonic rejection 101 = 16LO, third to 13th odd harmonic rejection 11X = reserved			0x00	CW mode functions (global).
0x02F	CW_OUTPUT	CW output dc bias voltage: 0 = bypass, 1 = enable (default)	0	0	0	0	0	0	0	0x80	CW dc voltage output control (global).
0x102	RESERVED_102	0	0	0	0	0	0	0	0	0x00	Reserved.
0x103	RESERVED_103	0	0	0	0	0	0	0	0	0x00	Reserved.
0x104	RESERVED_104	0	0	1	1	1	1	1	1	0x3F	Reserved.
0x105	RESERVED_105	0	0	0	0	0	0	0	0	0x00	Reserved.
0x106	RESERVED_106	0	0	0	0	0	0	0	9	0x00	Reserved.
0x107	RESERVED_107	0	0	0	0	0	0	X	X	Read only	Reserved.
0x108	RESERVED_108	0	0	0	0	0	0	0	0	0x00	Reserved.
0x109	VGA_TEST	X	X	X	VGA/AAF test mode enable: 0 = off (default), 1 = on	X	VGA/AAF output test mode: 000 = Channel A (default), 001 = Channel B, 010 = Channel C, 011 = Channel D, 100 = Channel E, 101 = Channel F, 110 = Channel G, 111 = Channel H			0x00	VGA/AAF test mode, enables AAF output to GPO2 and GPO3 pins (global).
0x10C	PROFILE_INDEX	X	X	Manual TX_TRIG: 0 = off, use pin (default), 1 = on, auto generate TX_TRIG (self clears)	Profile index, Bits[4:0]					0x00	Index for profile memory; selects active profile (global).
0x10D	RESERVED_10D	1	1	1	1	1	1	1	1	0xFF	Reserved.
0x10E	RESERVED_10E	1	1	1	1	1	1	1	1	0xFF	Reserved.
0x10F	DIG_OFFSET_CAL	0	0	0	0	Digital offset calibration status: 0 = not complete (default), 1 = complete	Digital offset calibration: 000 = disable correction, reset correction value (default), 001 = average 2^{10} samples, 010 = average 2^{11} samples, …, 111 = average 2^{16} samples			0x00	Controls digital offset calibration enable and number of samples used (global).

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Comments
0x110	DIG_OFFSET_ CORR1	D7	D6	D5	D4	D3	D2	D1	D0	0x00	Offset correction LSB (local, chip).
0x111	DIG_OFFSET_ CORR2	D15	D14	D13	D12	D11	D10	D9	D8	0x00	Offset correction MSB (local, chip).
		Digital offset calibration (read back if auto calibration enabled with Register 0x10F. Otherwise, force correction value.) Offset correction = [D15:D0] × $A_{FULL\text{-}SCALE}/2^{16}$, 0111 1111 1111 1111 ($2^{15} - 1$) = +1/2 × $A_{FULL\text{-}SCALE}$ − $1/2^{16}$ × $A_{FULL\text{-}SCALE}$, 0111 1111 1111 1110 ($2^{15} - 2$) = +1/2 × $A_{FULL\text{-}SCALE}$ − $2/2^{16}$ × $A_{FULL\text{-}SCALE}$, …, 0000 0000 0000 0001 (+1) = $1/2^{16}$ × $A_{FULL\text{-}SCALE}$, 0000 0000 0000 0000 = no correction (default), 1111 1111 1111 1111 (−1) = $-1/2^{16}$ × $A_{FULL\text{-}SCALE}$, …, 1000 0000 0000 0000 (-2^{15}) = −1/2 $A_{FULL\text{-}SCALE}$									
0x112	POWER_ MASK_CONFIG	X	X	X	Power-up setup time (POWER_SETUP): 0 0000 = 0, 0 0001 = 1 × $40/f_{SAMPLE}$, 0 0010 = 2 × $40/f_{SAMPLE}$ (default), 0 0011 = 3 × $40/f_{SAMPLE}$, …, 1 1111 = 31 × $40/f_{SAMPLE}$					0x02	Power setup time used to set the power-up time (global).
0x113	DIG_CONFIG	X	X	Digital high-pass filter: 0 = enable (default), 1 = bypass	0	Decimator and filter enable: 00 = RF 2× decimator bypassed (default), 01 = RF 2× decimator enabled and low band filter, 1X = RF 2× decimator enabled and high band filter,		X	X	0x00	Enables stages of the digital processing (global).
0x115	CHIP_ADDR_EN	X	X	Chip address mode: 0 = disable (default), 1 = enable	Chip address qualifier: 0 0000 (default), if read, returns state of Pin ADDR4 to Pin ADDR0					0x00	Chip address mode enables the addressing of specific devices if the value of Bits[4:0] qualifier equals the state on the ADDR4 to ADDR0 pins (global).
0x116	ANALOG_ TEST_TONE	X	X	X	X	Analog test signal amplitude (see Table 17 to Table 19)		Analog test signal frequency: 00 = $f_{SAMPLE}/4$ (default), 01 = $f_{SAMPLE}/8$, 10 = $f_{SAMPLE}/16$, 11 = $f_{SAMPLE}/32$		0x00	Analog test tone amplitude and frequency (global).
0x117	DIG_SINE_ TEST_FREQ	X	X	X	Digital test tone frequency: 0 0000 = 1 × $f_{SAMPLE}/64$, 0 0001 = 2 × $f_{SAMPLE}/64$, …, 1 1111 = 32 × $f_{SAMPLE}/64$					0x00	Digital sine test tone frequency (global).
0x118	DIG_SINE_ TEST_AMP	X	X	X	X	Digital test tone amplitude: 0000 = $A_{FULL\text{-}SCALE}$ (default), 0001 = $A_{FULL\text{-}SCALE}/2$, 0010 = $A_{FULL\text{-}SCALE}/2^2$, …, 1111 = $A_{FULL\text{-}SCALE}/2^{15}$				0x00	Digital sine test tone amplitude (global).
0x119	DIG_SINE_ TEST_OFFSET	Offset multiplier (a): 0 1111 = 15, 0 1110 = 14, …, 0 0000 = 0 (default), 1 1111 = −1, …, 1 0000 = −16					Offset exponent (b): 000 = 0 (default), 001 = 1, …, 111 = 7			0x00	Digital sine test tone offset (global).
		Offset = $A_{FULL\text{-}SCALE} \times a \times 2^{-(13-b)}$, offset range is ~0.5 dB, maximum positive offset = $15 \times 2^{-(13-7)} = 0.25 \times A_{FULL\text{-}SCALE}$, maximum negative offset = $-16 \times 2^{-(13-7)} \approx -0.25 \times A_{FULL\text{-}SCALE}$									
0x11A	TEST_MODE_ CH_ENABLE	Channel H enable: 0 = off (default), 1 = on	Channel G enable: 0 = off (default), 1 = on	Channel F enable: 0 = off (default), 1 = on	Channel E enable: 0 = off (default), 1 = on	Channel D enable: 0 = off (default), 1 = on	Channel C enable: 0 = off (default), 1 = on	Channel B enable: 0 = off (default), 1 = on	Channel A enable: 0 = off (default), 1 = on	0x00	Enables channels for test mode (global).

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Comments
0x11B	TEST_MODE_ CONFIG	X	X	X	X	X	Test mode selection: 000 = disable test modes (default), 001 = enable digital sine test mode, 010 = reserved 011 = enable channel ID test mode (16-bit data = digital ramp (7 bits) + reserved bit (0) + Channel ID (3 bits) + chip address (5 bits), 100 = enable analog test tone, 101 = reserved, 110 = reserved, 111 = reserved			0x00	Enables digital test modes (global).
0x11C	RESERVED_11C	0	0	0	0	0	0	0	0	0x00	Reserved.
0x11D	RESERVED_11D	0	0	0	0	0	0	0	0	0x00	Reserved.
0x11E	RESERVED_11E	0	0	0	0	0	0	0	0	0x00	Reserved.
0x11F	RESERVED_11F	0	0	0	0	0	0	0	0	0x00	Reserved.
0x120	CW_TEST_TONE	0	CW I/Q output swap: 0 = disable (default), 1 = enable	LNA offset cancel-lation: 0 = enable (default), 1 = disable	LNA offset cancellation transconductance: 00 = 0.5 mS (default), 01 = 1.0 mS, 10 = 1.5 mS, 11 = 2.0 mS		CW analog test tone override for Register 0x116 < Bits[1:0] > 00 = disable override (default) 01 = set analog test tone frequency to f_{LO} 1X = set analog test tone frequency to dc		0	0x00	Sets the frequency of the analog test tone to f_{LO} in CW Doppler mode; enables I/Q output swap; LNA offset cancellation control (global).
0x180	RESERVED_180	1	0	0	0	0	1	1	1	0x87	Reserved.
0x181	RESERVED_181	0	0	0	0	0	0	0	0	0x00	Reserved.
0x182	PLL_STARTUP	PLL auto configure: 0 = disable (default), 1 = enable	0	0	0	0	0	1	0	0x02	PLL control (global).
0x183	RESERVED_183	0	0	0	0	0	1	1	1	0x07	Reserved.
0x184	RESERVED_184	0	0	0	0	0	0	0	0	0x00	Reserved.
0x186	RESERVED_186	1	0	1	0	1	1	1	0	0xAE	Reserved.
0x187	RESERVED_187	0	0	1	0	0	0	0	0	0x20	Reserved.
0x188	START_CODE_EN	0	0	0	0	0	0	0	Start code identifier: 0 = disable, 1 = enable (default)	0x01	Enables start code identifier (global).
0x189	RESERVED_189	0	0	0	0	0	0	0	0	0x00	Reserved.
0x18A	RESERVED_18A	0	0	0	0	0	0	0	0	0x00	Reserved.
0x18B	START_CODE_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x27	Start code MSB (global).
0x18C	START_CODE_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x72	Start code LSB (global).
0x190	RESERVED_190	0	0	0	1	0	0	0	0	0x10	Reserved.
0x191	RESERVED_191	0	0	0	0	0	0	0	0	0x00	Reserved.
0x192	RESERVED_192	0	0	0	1	1	0	0	0	0x18	Reserved.
0x193	RESERVED_193	0	0	0	0	0	0	0	0	0x00	Reserved.
0x194	RESERVED_194	0	0	0	1	1	1	0	0	0x1C	Reserved.
0x195	RESERVED_195	0	0	0	0	0	0	0	0	0x00	Reserved.
0x196	RESERVED_196	0	0	0	1	1	0	0	0	0x18	Reserved.
0x197	RESERVED_197	0	0	0	0	0	0	0	0	0x00	Reserved.

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Comments
0x198	CLOCK_DOUBLING	0	0	0	0	DCO frequency doubling/divider: 0000 = 1 (default), 0001 = 2, 0010 = 4, 0011 = 8, 0100 = 16, 0101 = 32, 0110 = 64, 0111 = 128, 1000 = 1/256, 1001 = 1/128, 1010 = 1/64, 1011 = 1/32, 1100 = 1/16, 1101 = 1/8, 1110 = 1/4, 1111 = 1/2				0x00	DCO frequency control (global).
0x199	SAMPLE_CLOCK_ COUNTER	Enables clocks per sample auto calculation: 0 = off (default), 1 = on	0	0	0	0	0	0	0	0x00	Enables FCO function (global).
0x19A	DATA_OUTPUT_ INVERT	X	X	X	X	X	X	X	Inverts data output: 0 = noninverted (default), 1 = inverted	0x00	Inverts DOUT signal outputs (global).
0x19B	SERIAL_FORMAT	X	Enables FCO for start code sample: 0 = disable, 1 = enable (default)	Enables FCO for extra sample at end of burst: 0 = disable, 1 = enable (default)	Enables FCO continuously: 0 = only during burst, 1 = continuous (default)	FCO signal rotate: 0000 = FCO signal aligned with DOUT signal, 0001 = FCO 1 bit before DOUT, 0010 = FCO 2 bits before DOUT, …, 1101 = FCO 3 bits after DOUT, 1110 = FCO 2 bits after DOUT, 1111 = FCO 1 bit after DOUT				0x70	FCO signal controls (global).
0x19C	RESERVED_19C	0	0	0	1	0	0	0	0	0x10	Reserved.
0x19D	RESERVED_19D	0	0	0	0	0	0	0	0	0x00	Reserved.
0x19E	RESERVED_19E	0	0	0	1	0	0	0	0	0x10	Reserved.
0x19F	RESERVED_19F	0	0	0	0	0	0	0	0	0x00	Reserved.
0x1A0	RESERVED_1A0	0	0	0	0	0	0	0	0	0x00	Reserved.
0x1A1	RESERVED_1A1	0	0	0	0	0	0	0	0	0x00	Reserved.
Profile Memory Registers											
0xF00 to 0xFFF	Profile memory	32 × 64 bits								0x00	Vector profile memory (global).

MEMORY MAP REGISTER DESCRIPTIONS

For more information about the SPI memory map and other functions, consult the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Transfer (Register 0x0FF)

All registers except Register 0x002 update as soon as they are written. Writing to Register 0x0FF (the value written is don't care) initializes and updates the speed mode (Address 0x002) and resets all other registers to their default values (analog and ADC registers only, and not JESD204B registers, Register 0x000 or Register 0x002).

Set the speed mode in Register 0x002 and write to Register 0x0FF at the beginning of the setup of the SPI writes after the device is powered up to avoid rewriting other registers after Register 0x0FF is written.

Profile Index and Manual TX_TRIG (Register 0x10C)

The vector profile is selected using the profile index in Register 0x10C, Bits[4:0]. The manual TX_TRIG control in Bit 5 generates a TX_TRIG signal internal to the device. This signal is asynchronous to the ADC sample clock. Therefore, it cannot be used to align the data output or initiate advanced power mode across multiple devices in the system. The external pin driven TX_TRIG± control is recommended for systems that require synchronization of these features across multiple AD9674 devices.

OUTLINE DIMENSIONS

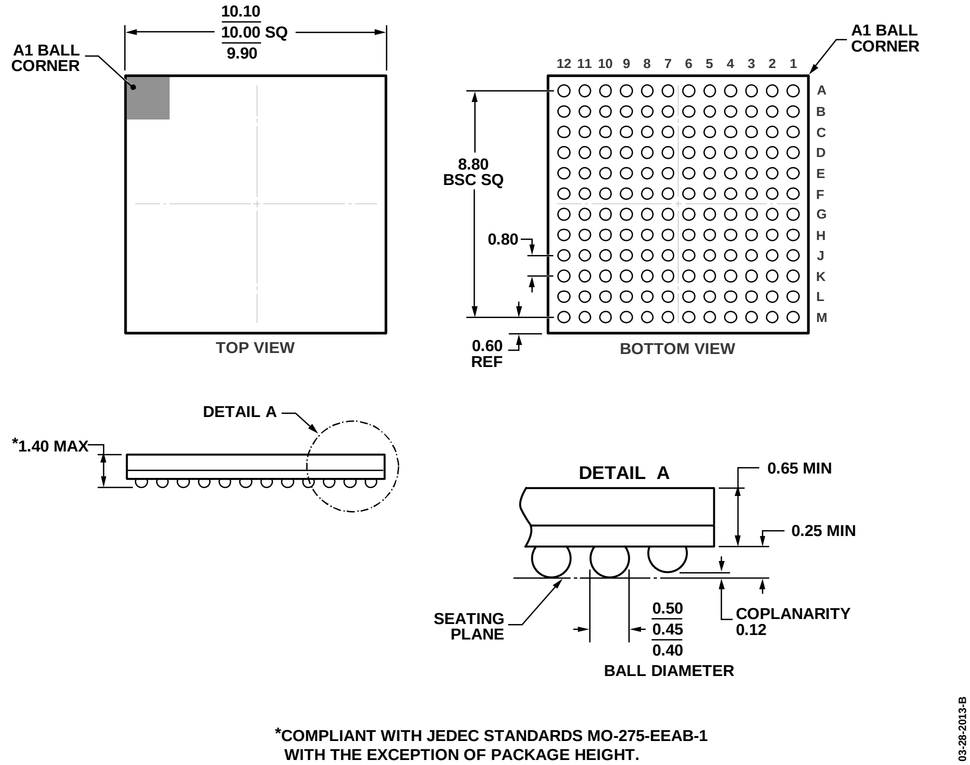

Figure 55. 144-Ball Chip Scale Package, Ball Grid Array [CSP_BGA]
(BC-144-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9674KBCZ	0°C to 85°C	144-Ball Chip Scale Package, Ball Grid Array [CSP_BGA]	BC-144-1
AD9670EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.