Self-Protected Low Side Driver with Temperature and Current Limit

NCV8405A/B is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device is suitable for harsh automotive environments.

Features

- Short-Circuit Protection
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

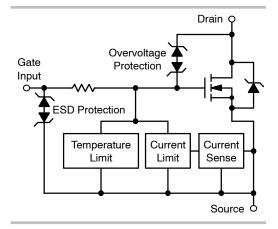


ON Semiconductor®

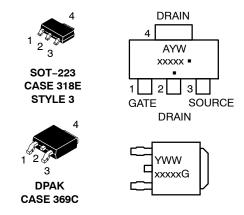
www.onsemi.com

V _{(BR)DSS} (Clamped)	R _{DS(ON)} TYP	I _D MAX
42 V	90 m Ω @ 10 V	6.0 A*

^{*}Max current limit value is dependent on input condition.



MARKING DIAGRAM



A = Assembly Location

Y = Year W, WW = Work Week xxxxx = 8405A or 8405B G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise noted)

Rating			Value	Unit
Drain-to-Source Voltage Internally Clamped		V_{DSS}	42	V
Drain-to-Gate Voltage Internally Clamped	$(R_G = 1.0 M\Omega)$	V_{DGR}	42	V
Gate-to-Source Voltage		V _{GS}	±14	V
Continuous Drain Current		I _D	Internally L	imited
Power Dissipation – SOT–223 Version Power Dissipation – DPAK Version	@ T _A = 25°C (Note 1) @ T _A = 25°C (Note 2) @ T _S = 25°C @ T _A = 25°C (Note 1) @ T _A = 25°C (Note 2) @ T _S = 25°C	P _D	1.0 1.7 11.4 2.0 2.5 40	W
Thermal Resistance – SOT-223 Version Thermal Resistance – DPAK Version	Junction-to-Ambient Steady State (Note 1) Junction-to-Ambient Steady State (Note 2) Junction-to-Soldering Point Steady State Junction-to-Ambient Steady State (Note 1) Junction-to-Ambient Steady State (Note 2) Junction-to-Soldering Point Steady State	R _{OJA}	130 72 11 60 50 3.0	°C/W
Single Pulse Drain–to–Source Avalanche Energy (V _{DD} = 40 V, V _G = 5.0 V, I _{PK} = 2.8 A, L = 80 mH, R _{G(ext)} = 25 Ω , TJ = 25°C)			275	mJ
Load Dump Voltage $V_{LD} = V_A + V_S (V_{GS} = 0 \text{ and } 10 \text{ V}, R_I = 2.0 \Omega, R_L = 6.0 \Omega, t_d = 400 \text{ ms})$			53	V
Operating Junction Temperature			-40 to 150	°C
Storage Temperature			-55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted onto min pad FR4 PCB, (2 oz. Cu, 0.06" thick).

2. Surface-mounted onto 2" sq. FR4 board (1" sq., 1 oz. Cu, 0.06" thick).

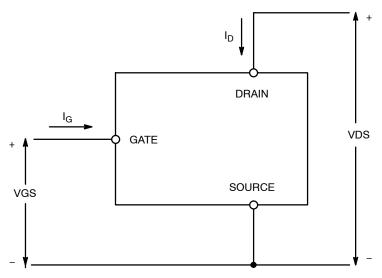


Figure 1. Voltage and Current Convention

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS			<u>l</u>			
Drain-to-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 25^{\circ}\text{C}$	V _{(BR)DSS}	42	46	51	V
(Note 3)	V _{GS} = 0 V, I _D = 10 mA, T _J = 150°C (Note 5)	· (BH)D33	42	45	51	1
Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 32 V, T _J = 25°C	I _{DSS}		0.5	2.0	μΑ
-	V _{GS} = 0 V, V _{DS} = 32 V, T _J = 150°C (Note 5)			2.0	10	
Gate Input Current	V _{DS} = 0 V, V _{GS} = 5.0 V	I _{GSSF}		50	100	μΑ
ON CHARACTERISTICS (Note 3)			•			
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 150 \mu A$	V _{GS(th)}	1.0	1.6	2.0	V
Gate Threshold Temperature Coefficient		V _{GS(th)} /T _J		4.0		-mV/°C
Static Drain-to-Source On-Resistance	V _{GS} = 10 V, I _D = 1.4 A, T _J = 25°C	R _{DS(on)}		90	100	mΩ
	V _{GS} = 10 V, I _D = 1.4 A, T _J = 150°C (Note 5)			165	190	
	V _{GS} = 5.0 V, I _D = 1.4 A, T _J = 25°C			105	120	
	V _{GS} = 5.0 V, I _D = 1.4 A, T _J = 150°C (Note 5)			185	210	1
	V _{GS} = 5.0 V, I _D = 0.5 A, T _J = 25°C			105	120	
	$V_{GS} = 5.0 \text{ V}, I_D = 0.5 \text{ A}, T_J = 150^{\circ}\text{C}$ (Note 5)			185	210	1
Source-Drain Forward On Voltage	V _{GS} = 0 V, I _S = 7.0 A	V _{SD}		1.05		V
SWITCHING CHARACTERISTICS (Note	5)		ı			
Turn-ON Time (10% V _{IN} to 90% I _D)	V _{GS} = 10 V, V _{DD} = 12 V	t _{ON}		20		μs
Turn-OFF Time (90% V _{IN} to 10% I _D)	$I_D = 2.5 \text{ A}, R_L = 4.7 \Omega$	t _{OFF}		110		
Slew-Rate ON (70% V _{DS} to 50% V _{DS})	V _{GS} = 10 V, V _{DD} = 12 V,	-dV _{DS} /dt _{ON}		1.0		V/μs
Slew-Rate OFF (50% V _{DS} to 70% V _{DS})	$R_L = 4.7 \Omega$	dV _{DS} /dt _{OFF}		0.4		
SELF PROTECTION CHARACTERISTIC	S (T _J = 25°C unless otherwise noted) (Note 4)				
Current Limit	$V_{DS} = 10 \text{ V}, V_{GS} = 5.0 \text{ V}, T_{J} = 25^{\circ}\text{C}$	I _{LIM}	6.0	9.0	11	Α
	V _{DS} = 10 V, V _{GS} = 5.0 V, T _J = 150°C (Note 5)		3.0	5.0	8.0	
	V _{DS} = 10 V, V _{GS} = 10 V, T _J = 25°C		7.0	10.5	13	
	V _{DS} = 10 V, V _{GS} = 10 V, T _J = 150°C (Note 5)		4.0	7.5	10	1
Temperature Limit (Turn-off)	V _{GS} = 5.0 V (Note 5)	T _{LIM(off)}	150	180	200	°C
Thermal Hysteresis	V _{GS} = 5.0 V	$\Delta T_{LIM(on)}$		15		
Temperature Limit (Turn-off)	V _{GS} = 10 V (Note 5)	T _{LIM(off)}	150	165	185	
Thermal Hysteresis	V _{GS} = 10 V	$\Delta T_{LIM(on)}$		15		
GATE INPUT CHARACTERISTICS (Note	5)					
Device ON Gate Input Current	$V_{GS} = 5 V I_D = 1.0 A$	I_{GON}		50		μΑ
	V _{GS} = 10 V I _D = 1.0 A			400		
Current Limit Gate Input Current	$V_{GS} = 5 \text{ V}, V_{DS} = 10 \text{ V}$	I _{GCL}		0.05		mA
	V _{GS} = 10 V, V _{DS} = 10 V			0.4		
Thermal Limit Fault Gate Input Current	V _{GS} = 5 V, V _{DS} = 10 V	I _{GTL}		0.22		mA
	V _{GS} = 10 V, V _{DS} = 10 V			1.0	_	
ESD ELECTRICAL CHARACTERISTICS	$(T_J = 25^{\circ}C \text{ unless otherwise noted})$ (No	ote 5)				
Electro-Static Discharge Capability	Human Body Model (HBM)	ESD	4000			V
	Machine Model (MM)		400			

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Fault conditions are viewed as beyond the normal operating range of the part.
 Not subject to production testing.

TYPICAL PERFORMANCE CURVES

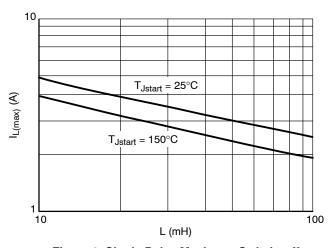


Figure 2. Single Pulse Maximum Switch-off Current vs. Load Inductance

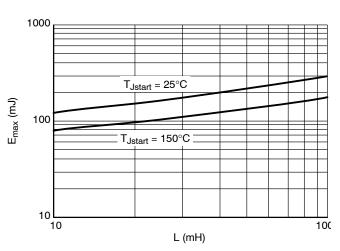


Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance

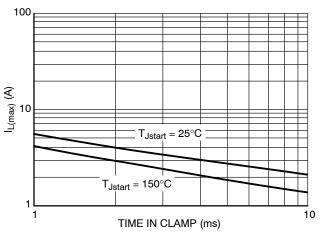


Figure 4. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp

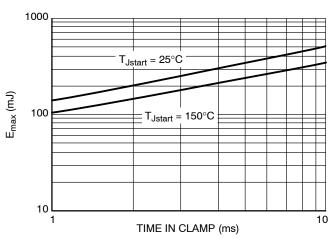


Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp

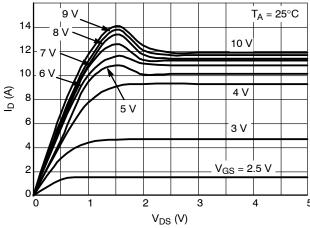


Figure 6. Output Characteristics

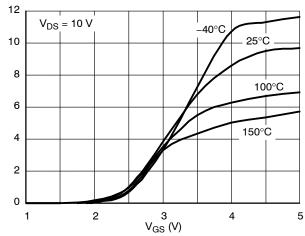


Figure 7. Transfer Characteristics

I_D (A)

TYPICAL PERFORMANCE CURVES

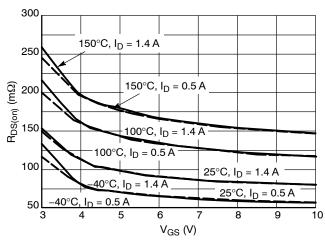


Figure 8. R_{DS(on)} vs. Gate-Source Voltage

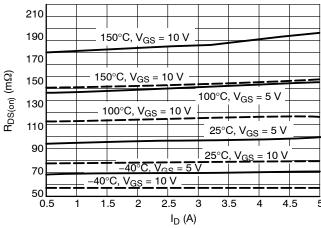


Figure 9. R_{DS(on)} vs. Drain Current

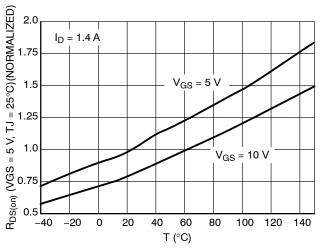


Figure 10. Normalized R_{DS(on)} vs. Temperature

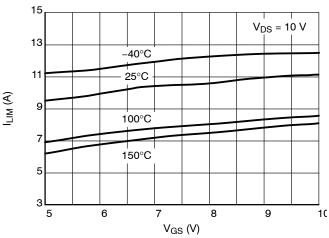


Figure 11. Current Limit vs. Gate-Source Voltage

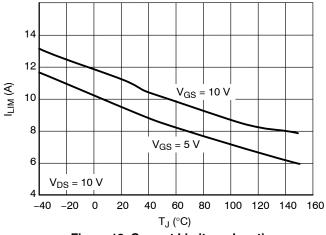


Figure 12. Current Limit vs. Junction Temperature

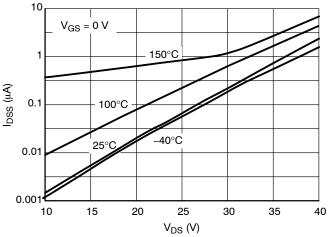


Figure 13. Drain-to-Source Leakage Current

TYPICAL PERFORMANCE CURVES

V_{SD} (V)

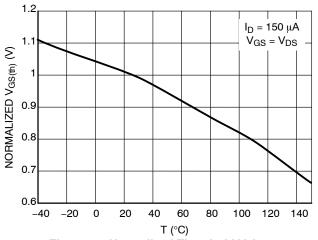


Figure 14. Normalized Threshold Voltage vs. Temperature

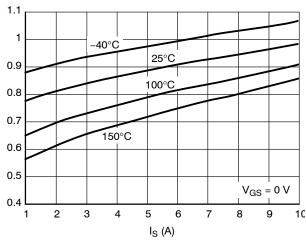


Figure 15. Body-Diode Forward Characteristics

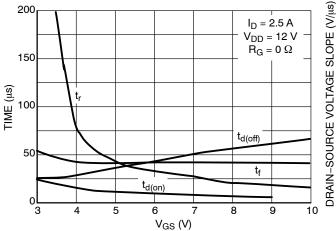


Figure 16. Resistive Load Switching Time vs.

Gate-Source Voltage

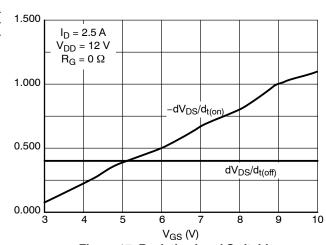


Figure 17. Resistive Load Switching
Drain-Source Voltage Slope vs. Gate-Source
Voltage

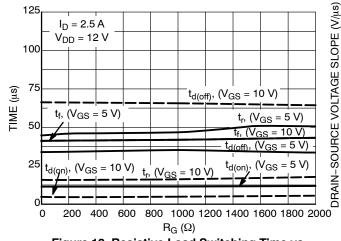


Figure 18. Resistive Load Switching Time vs.

Gate Resistance

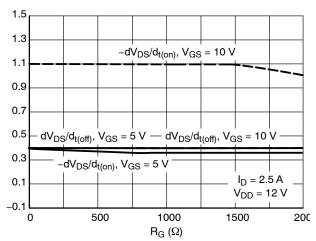


Figure 19. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

TYPICAL PERFORMANCE CURVES

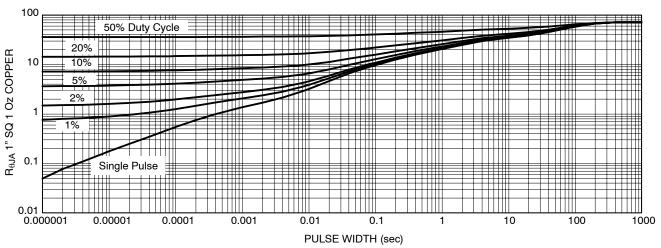


Figure 20. Transient Thermal Resistance

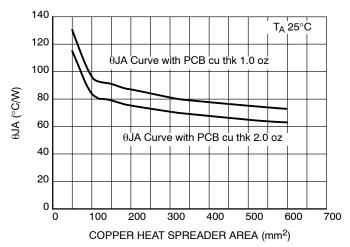


Figure 21. θ JA vs. Copper

TEST CIRCUITS AND WAVEFORMS

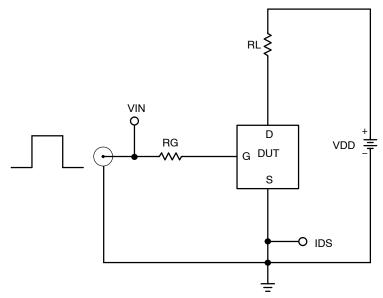


Figure 22. Resistive Load Switching Test Circuit

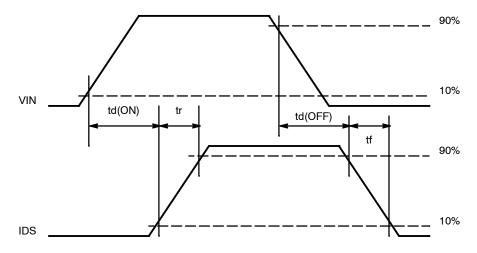


Figure 23. Resistive Load Switching Waveforms

TEST CIRCUITS AND WAVEFORMS

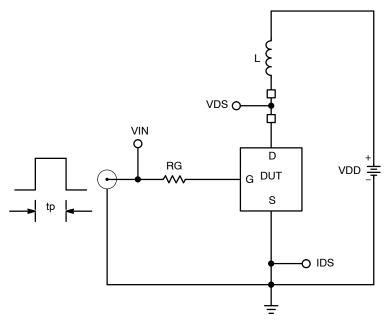


Figure 24. Inductive Load Switching Test Circuit

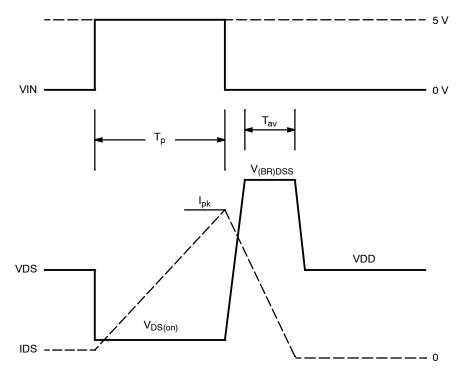


Figure 25. Inductive Load Switching Waveforms

ORDERING INFORMATION

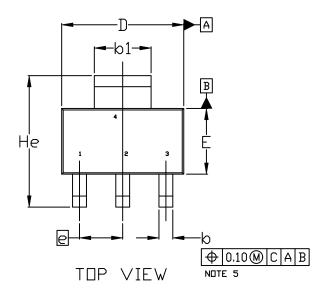
Device	Package	Shipping [†]
NCV8405ASTT1G	SOT-223 (Pb-Free)	1000 / Tape & Reel
NCV8405ASTT3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NCV8405ADTRKG	DPAK (Pb-Free)	2500 / Tape & Reel
NCV8405BDTRKG	DPAK (Pb-Free)	2500 / Tape & Reel

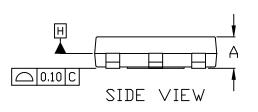
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

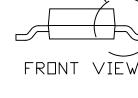


SOT-223 (TO-261) CASE 318E-04 ISSUE R

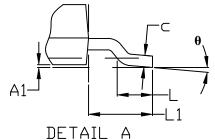
DATE 02 OCT 2018







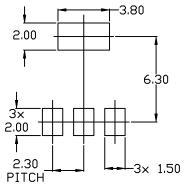
SEE DETAIL A



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
 MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
- 4. DATUMS A AND B ARE DETERMINED AT DATUM H.
- 5. ALLIS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
- 6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS 6 AND 61.

	MILLIMETERS			
DIM	MIN.	N□M.	MAX.	
Α	1.50	1.63	1.75	
A1	0.02	0.06	0.10	
b	0.60	0.75	0.89	
b1	2.90	3.06	3.20	
C	0.24	0.29	0.35	
D	6.30	6.50	6.70	
E	3.30	3.50	3.70	
е	2.30 BSC			
L	0.20			
L1	1.50	1.75	2.00	
He	6.70	7.00	7.30	
θ	0°		10°	



RECOMMENDED MOUNTING FOOTPRINT

DOCUMENT NUMBER:	98ASB42680B Electronic versions are uncontrolled except when accessed directly fro Printed versions are uncontrolled except when stamped "CONTROLLE"		
DESCRIPTION:	SOT-223 (TO-261)		PAGE 1 OF 2

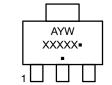
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SOT-223 (TO-261) CASE 318E-04 ISSUE R

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

GENERIC MARKING DIAGRAM*



A = Assembly Location

Y = Year W = Work Week

XXXXX = Specific Device Code

= Pb-Free Package

(Note: Microdot may be in either location)
*This information is generic. Please refer to
device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "•", may
or may not be present. Some products may
not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from Printed versions are uncontrolled except when stamped "CONTROLLED (
DESCRIPTION:	SOT-223 (TO-261)		PAGE 2 OF 2

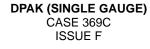
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ROTATED 90° CW

STYLE 1:

STYLE 2:





DATE 21 JUL 2015

- IOTES. 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: INCHES. 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DI-

- MENSIONS b3, L3 and Z.

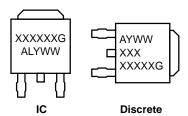
 Jimensions b And E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.

 MENSIONS D AND E ARE DETERMINED AT THE
- OUTERMOST EXTREMES OF THE PLASTIC BODY.

 6. DATUMS A AND B ARE DETERMINED AT DATUM
- 7. OPTIONAL MOLD FEATURE.

	INC	INCHES		IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.086	0.094	2.18	2.38	
A1	0.000	0.005	0.00	0.13	
b	0.025	0.035	0.63	0.89	
b2	0.028	0.045	0.72	1.14	
b3	0.180	0.215	4.57	5.46	
С	0.018	0.024	0.46	0.61	
c2	0.018	0.024	0.46	0.61	
D	0.235	0.245	5.97	6.22	
E	0.250	0.265	6.35	6.73	
е	0.090	0.090 BSC		2.29 BSC	
Н	0.370	0.410	9.40	10.41	
L	0.055	0.070	1.40	1.78	
L1	0.114 REF		2.90	REF	
L2	0.020	BSC	0.51	BSC	
L3	0.035	0.050	0.89	1.27	
L4		0.040		1.01	
Z	0.155		3.93		

GENERIC MARKING DIAGRAM*



XXXXXX = Device Code = Assembly Location Α = Wafer Lot L

Υ = Year WW = Work Week G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

В L3 Ζ Ո DETAIL A NOTE 7 **BOTTOM VIEW** Cb2 е SIDE VIEW | \oplus | 0.005 (0.13) lacktriangle C **TOP VIEW** Z Ħ L2 GAUGE C SEATING PLANE **BOTTOM VIEW** Α1 ALTERNATE CONSTRUCTIONS **DETAIL A**

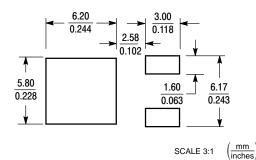
3. EMITTER	3. SOURCE	 ANODE CATHODE 	3. GATE	3. CATHODE
4. COLLECTOR	4. DRAIN		4. ANODE	4. ANODE
3. GATE 3. EMI	LECTOR 2. TTER 3.	N/C PIN CATHODE ANODE	E 9: 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE	STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE

STYLE 4:

STYLE 5:

STYLE 3:

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DESCRIPTION:	DPAK SINGLE GAUGE SURFACE MOUNT		PAGE 1 OF 2
NEW STANDARD:	REF TO JEDEC TO-252	"CONTROLLED COPY" in red.	
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Α	ADDED STYLE 8. REQ. BY S. ALLEN.	06 AUG 2008
В	ADDED STYLE 9. REQ. BY D. WARNER.	16 JAN 2009
С	ADDED STYLE 10. REQ. BY S. ALLEN.	09 JUN 2009
D	RELABELED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITTE.	29 JUN 2010
E	ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAMBALIZA.	06 FEB 2014
F	ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA.	21 JUL 2015

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