

SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374

OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

- Choice of Eight Latches or Eight D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Clock-Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)
- P-N-P Inputs Reduce DC Loading on Data Lines ('S373 and 'S374)

description

These 8-bit registers feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The high-impedance 3-state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pullup components. These devices are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

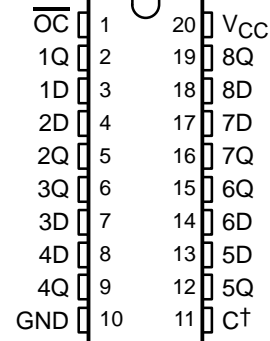
The eight latches of the 'LS373 and 'S373 are transparent D-type latches, meaning that while the enable (C or CLK) input is high, the Q outputs follow the data (D) inputs. When C or CLK is taken low, the output is latched at the level of the data that was set up.

The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output-control (\overline{OC}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

\overline{OC} does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered, even while the outputs are off.

SN54LS373, SN54LS374, SN54S373,
SN54S374 . . . J OR W PACKAGE
SN74LS373, SN74S374 . . . DW, N, OR NS PACKAGE
SN74LS374 . . . DB, DW, N, OR NS PACKAGE
SN74S373 . . . DW OR N PACKAGE
(TOP VIEW)



† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

SN54LS373, SN54LS374, SN54S373,
SN54S374 . . . FK PACKAGE
(TOP VIEW)



† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374
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ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------------|-----------------|---------------|------------------------------|-------------------------|
| 0°C to 70°C | PDIP – N | Tube | SN74LS373N | SN74LS373N |
| | | Tube | SN74LS374N | SN74LS374N |
| | | Tube | SN74S373N | SN74S373N |
| | | Tube | SN74S374N | SN74S374N |
| | SOIC – DW | Tube | SN74LS373DW | LS373 |
| | | Tape and reel | SN74LS373DWR | |
| | | Tube | SN74LS374DW | LS374 |
| | | Tape and reel | SN74LS374DWR | |
| | | Tube | SN74S373DW | S373 |
| | | Tape and reel | SN74S373DWR | |
| | | Tube | SN74S374DW | S374 |
| | | Tape and reel | SN74S374DWR | |
| | SOP – NS | Tape and reel | SN74LS373NSR | 74LS373 |
| | | Tape and reel | SN74LS374NSR | 74LS374 |
| | | Tape and reel | SN74S374NSR | 74S374 |
| | SSOP – DB | Tape and reel | SN74LS374DBR | LS374A |
| –55°C to 125°C | CDIP – J | Tube | SN54LS373J | SN54LS373J |
| | | Tube | SNJ54LS373J | SNJ54LS373J |
| | | Tube | SN54LS374J | SN54LS374J |
| | | Tube | SNJ54LS374J | SNJ54LS374J |
| | | Tube | SN54S373J | SN54S373J |
| | | Tube | SNJ54S373J | SNJ54S373J |
| | | Tube | SN54S374J | SN54S374J |
| | | Tube | SNJ54S374J | SNJ54S374J |
| | CFP – W | Tube | SNJ54LS373W | SNJ54LS373W |
| | | Tube | SNJ54LS374W | SNJ54LS374W |
| | | Tube | SNJ54S374W | SNJ54S374W |
| | LCCC – FK | Tube | SNJ54LS373FK | SNJ54LS373FK |
| | | Tube | SNJ54LS374FK | SNJ54LS374FK |
| | | Tube | SNJ54S373FK | SNJ54S373FK |
| | | Tube | SNJ54S374FK | SNJ54S374FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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Function Tables

'LS373, 'S373
(each latch)

| INPUTS | | | OUTPUT Q |
|-----------------|---|---|----------------|
| \overline{OC} | C | D | |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

'LS374, 'S374
(each latch)

| INPUTS | | | OUTPUT Q |
|-----------------|-----|---|----------------|
| \overline{OC} | CLK | D | |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**
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logic diagrams (positive logic)



Pin numbers shown are for DB, DW, J, N, NS, and W packages.



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**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**

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schematic of inputs and outputs

'LS373



'LS374



**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†
(‘LS devices)**

| | |
|--|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage, V_I | 7 V |
| Off-state output voltage | 5.5 V |
| Package thermal impedance, θ_{JA} (see Note 2): | |
| DB package | 70°C/W |
| DW package | 58°C/W |
| N package | 69°C/W |
| NS package | 60°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

| | | SN54LS' | | | SN74LS' | | | UNIT | | |
|----------|--------------------------------|----------|-----|-----|---------|-----|------|------|----|----|
| | | MIN | NOM | MAX | MIN | NOM | MAX | | | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5 | 4.75 | 5 | 5.25 | V | | |
| V_{OH} | High-level output voltage | | | 5.5 | | | 5.5 | V | | |
| I_{OH} | High-level output current | | | -1 | | | -2.6 | mA | | |
| I_{OL} | Low-level output current | | | 12 | | | 24 | mA | | |
| t_w | Pulse duration | CLK high | | 15 | | 15 | | ns | | |
| | | CLK low | | 15 | | 15 | | | | |
| t_{su} | Data setup time | 'LS373 | | 5↓ | | 5↓ | | ns | | |
| | | 'LS374 | | 20↑ | | 20↑ | | | | |
| t_h | Data hold time | 'LS373 | | 20↓ | | 20↓ | | ns | | |
| | | 'LS374‡ | | 5↑ | | 0↑ | | | | |
| T_A | Operating free-air temperature | | | -55 | | 125 | | 0 | 70 | °C |

‡ The t_h specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns (commercial only).



**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN54LS' | | | SN74LS' | | | UNIT | |
|---|--|-------------------------|------|-----|---------|------|------|------|----|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | | |
| V _{IH} High-level input voltage | | 2 | | | 2 | | | V | |
| V _{IL} Low-level input voltage | | | | | 0.7 | | | V | |
| V _{IK} Input clamp voltage | V _{CC} = MIN, I _I = -18 mA | | | | -1.5 | | | V | |
| V _{OH} High-level output voltage | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX | 2.4 | 3.4 | | 2.4 | 3.1 | | V | |
| V _{OL} Low-level output voltage | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max | I _{OL} = 12 mA | | | 0.25 | 0.4 | 0.25 | 0.4 | V |
| | | I _{OL} = 24 mA | | | | | 0.35 | 0.5 | |
| I _{OZH} Off-state output current, high-level voltage applied | V _{CC} = MAX, V _O = 2.7 V, V _{IH} = 2 V | | | | 20 | | | μA | |
| I _{OZL} Off-state output current, low-level voltage applied | V _{CC} = MAX, V _O = 0.4 V, V _{IH} = 2 V | | | | -20 | | | μA | |
| I _I Input current at maximum input voltage | V _{CC} = MAX, V _I = 7 V | | | | 0.1 | | | mA | |
| I _{IH} High-level input current | V _{CC} = MAX, V _I = 2.7 V | | | | 20 | | | μA | |
| I _{IL} Low-level input current | V _{CC} = MAX, V _I = 0.4 V | | | | -0.4 | | | mA | |
| I _{OS} Short-circuit output current§ | V _{CC} = MAX | | | | -30 | -130 | -30 | -130 | mA |
| I _{CC} Supply current | V _{CC} = MAX, Output control at 4.5 V | 'LS373 | | | 24 | 40 | 24 | 40 | mA |
| | | 'LS374 | | | 27 | 40 | 27 | 40 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'LS373 | | | 'LS374 | | | UNIT |
|------------------|-----------------|-------------|--|--------|-----|-----|--------|-----|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| f _{max} | | | R _L = 667 Ω, C _L = 45 pF, See Note 3 | | | | 35 | 50 | | MHz |
| t _{PLH} | Data | Any Q | R _L = 667 Ω, C _L = 45 pF, See Note 3 | 12 | | | 18 | | | ns |
| t _{PHL} | | | | 12 | | | 18 | | | |
| t _{PLH} | C or CLK | Any Q | R _L = 667 Ω, C _L = 45 pF, See Note 3 | 20 | | | 15 | | | ns |
| t _{PHL} | | | | 18 | | | 30 | | | |
| t _{PZH} | \overline{OC} | Any Q | R _L = 667 Ω, C _L = 45 pF, See Note 3 | 15 | | | 28 | | | ns |
| t _{PZL} | | | | 25 | | | 36 | | | |
| t _{PHZ} | \overline{OC} | Any Q | R _L = 667 Ω, C _L = 5 pF | 15 | | | 25 | | | ns |
| t _{PLZ} | | | | 12 | | | 20 | | | |

NOTE 3: Maximum clock frequency is tested with all outputs loaded.

f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level



**SN54LS373, SN54LS374, SN54S373, SN54S374,
 SN74LS373, SN74LS374, SN74S373, SN74S374
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schematic of inputs and outputs

'S373 and 'S374

'S373 and 'S374



**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†
(‘S devices)**

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage, V_I | 5.5 V |
| Off-state output voltage | 5.5 V |
| Package thermal impedance, θ_{JA} (see Note 2): DW package | 58°C/W |
| N package | 69°C/W |
| NS package | 60°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

| | | SN54S' | | | SN74S' | | | UNIT |
|----------|--------------------------------|--------|-----|-----|--------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{OH} | High-level output voltage | | | 5.5 | | | 5.5 | V |
| I_{OH} | High-level output current | | | –2 | | | –6.5 | mA |
| t_w | Pulse duration, clock/enable | High | 6 | | 6 | | | ns |
| | | Low | 7.3 | | 7.3 | | | |
| t_{su} | Data setup time | 'S373 | 0↓ | | 0↓ | | | ns |
| | | 'S374 | 5↑ | | 5↑ | | | |
| t_h | Data hold time | 'S373 | 10↓ | | 10↓ | | | ns |
| | | 'S374 | 2↑ | | 2↑ | | | |
| T_A | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |



**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (SN54S373, SN54S374, SN74S373, SN74S374)

| PARAMETER | | TEST CONDITIONS† | | | | MIN | TYP‡ | MAX | UNIT |
|-------------------|-----------------------|--|---|--|--|-----|------|------|------|
| V _{IH} | | | | | | 2 | | | V |
| V _{IL} | | | | | | | | 0.8 | V |
| V _{IK} | | V _{CC} = MIN, I _I = -18 mA | | | | | | -1.2 | V |
| V _{OH} | SN54S' | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = MAX | | | | 2.4 | 3.4 | | V |
| | SN74S' | | | | | 2.4 | 3.1 | | |
| V _{OL} | | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA | | | | | | 0.5 | V |
| I _{OZH} | | V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.4 V | | | | | | 50 | μA |
| I _{OZL} | | V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.5 V | | | | | | -50 | μA |
| I _I | | V _{CC} = MAX, V _I = 5.5 V | | | | | | 1 | mA |
| I _{IH} | | V _{CC} = MAX, V _I = 2.7 V | | | | | | 50 | μA |
| I _{IL} | | V _{CC} = MAX, V _I = 0.5 V | | | | | | -250 | μA |
| I _{OS} § | | V _{CC} = MAX | | | | -40 | | -100 | mA |
| I _{CC} | V _{CC} = MAX | 'S373 | Outputs high | | | | 160 | mA | |
| | | | Outputs low | | | | 160 | | |
| | | | Outputs disabled | | | | 190 | | |
| | | 'S374 | Outputs high | | | | 110 | | |
| | | | Outputs low | | | | 140 | | |
| | | | Outputs disabled | | | | 160 | | |
| | | | CLK and \overline{OC} at 4 V, D inputs at 0 V | | | | 180 | | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'S373 | | | 'S374 | | | UNIT |
|------------------|-----------------|-------------|--|-------|-----|-----|-------|-----|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| f _{max} | | | R _L = 280 Ω, C _L = 15 pF, See Note 3 | | | | 75 | 100 | | MHz |
| t _{PLH} | Data | Any Q | R _L = 280 Ω, C _L = 15 pF, See Note 3 | 7 | 12 | | | | | ns |
| t _{PHL} | | | | 7 | 12 | | | | | |
| t _{PLH} | C or CLK | Any Q | R _L = 280 Ω, C _L = 15 pF, See Note 3 | 7 | 14 | | 8 | 15 | | ns |
| t _{PHL} | | | | 12 | 18 | | 11 | 17 | | |
| t _{PZH} | \overline{OC} | Any Q | R _L = 280 Ω, C _L = 15 pF, See Note 3 | 8 | 15 | | 8 | 15 | | ns |
| t _{PZL} | | | | 11 | 18 | | 11 | 18 | | |
| t _{PHZ} | \overline{OC} | Any Q | R _L = 280 Ω, C _L = 5 pF | 6 | 9 | | 5 | 9 | | ns |
| t _{PLZ} | | | | 8 | 12 | | 7 | 12 | | |

NOTE 3. Maximum clock frequency is tested with all outputs loaded.

f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

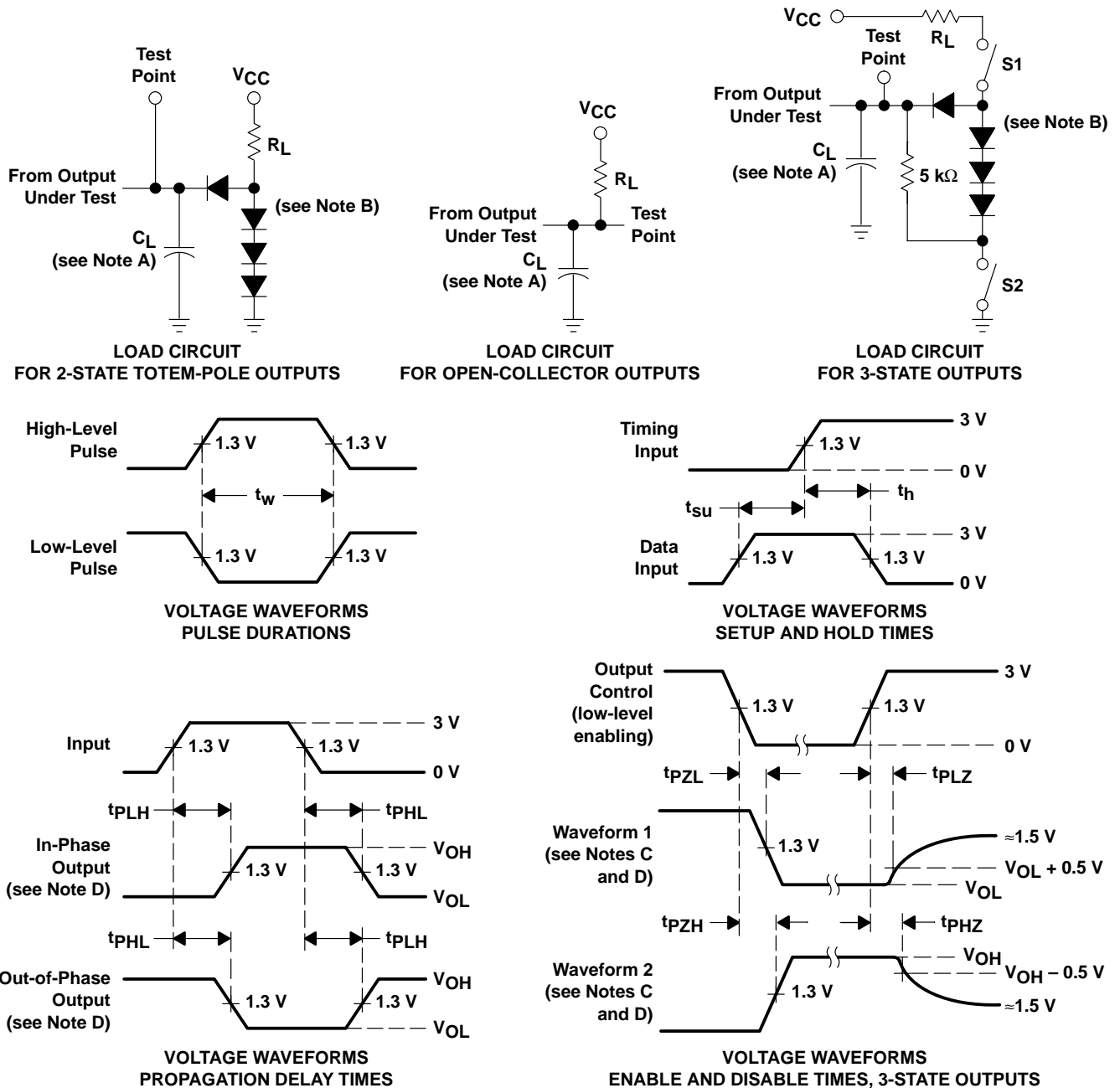
t_{PLZ} = output disable time from low level



**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**

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**PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES**



- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.
 G. The outputs are measured one at a time with one input transition per measurement.
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374
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**PARAMETER MEASUREMENT INFORMATION
SERIES 54S/74S DEVICES**



- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
 F. The outputs are measured one at a time with one input transition per measurement.
 G. All parameters and waveforms are not applicable to all devices.

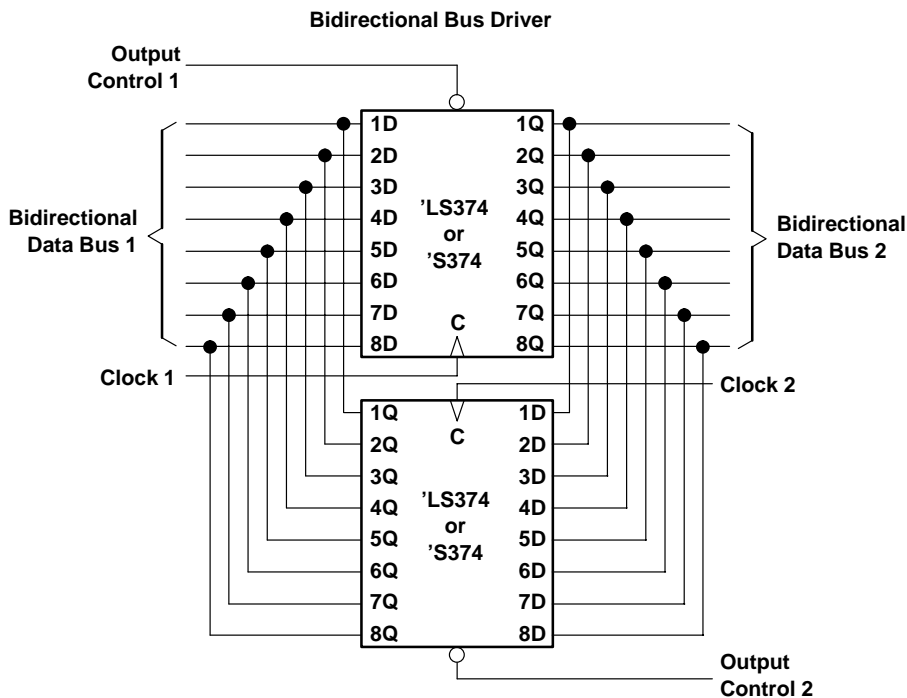
Figure 2. Load Circuits and Voltage Waveforms



**SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374**

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TYPICAL APPLICATION DATA



Clock Circuit for Bus Exchange

Expandable 4-Word by 8-Bit General Register File



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------------|-------------------------|
| 78011022A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 78011022A SNJ54LS 374FK | Samples |
| 7801102RA | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 7801102RA SNJ54LS374J | Samples |
| 7801102SA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 7801102SA SNJ54LS374W | Samples |
| JM38510/32502B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32502B2A | Samples |
| JM38510/32502BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32502BRA | Samples |
| JM38510/32502BSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32502BSA | Samples |
| JM38510/32502SRA | ACTIVE | CDIP | J | 20 | 20 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32502SRA | Samples |
| JM38510/32502SSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32502SSA | Samples |
| JM38510/32503B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32503B2A | Samples |
| JM38510/32503BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32503BRA | Samples |
| JM38510/32503BSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32503BSA | Samples |
| M38510/32502B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32502B2A | Samples |
| M38510/32502BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32502BRA | Samples |
| M38510/32502BSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32502BSA | Samples |
| M38510/32502SRA | ACTIVE | CDIP | J | 20 | 20 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32502SRA | Samples |
| M38510/32502SSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32502SSA | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| M38510/32503B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 32503B2A | Samples |
| M38510/32503BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32503BRA | Samples |
| M38510/32503BSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 32503BSA | Samples |
| SN54LS373J | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | SN54LS373J | Samples |
| SN54LS374J | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | SN54LS374J | Samples |
| SN54S373J | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | SN54S373J | Samples |
| SN54S374J | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | SN54S374J | Samples |
| SN74LS373DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS373 | Samples |
| SN74LS373DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS373 | Samples |
| SN74LS373N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS373N | Samples |
| SN74LS373NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS373N | Samples |
| SN74LS373NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS373 | Samples |
| SN74LS374DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS374A | Samples |
| SN74LS374DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS374 | Samples |
| SN74LS374DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS374 | Samples |
| SN74LS374DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS374 | Samples |
| SN74LS374N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS374N | Samples |
| SN74LS374NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS374N | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|--------------------------------------|----------------------|--------------|---------------------------|-------------------------|
| SN74LS374NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS374 | Samples |
| SN74LS374NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS374 | Samples |
| SN74S373N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S373N | Samples |
| SN74S374N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S374N | Samples |
| SNJ54LS373FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54LS373FK | Samples |
| SNJ54LS373J | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54LS373J | Samples |
| SNJ54LS373W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SNJ54LS373W | Samples |
| SNJ54LS374FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 78011022A SNJ54LS374FK | Samples |
| SNJ54LS374J | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 7801102RA SNJ54LS374J | Samples |
| SNJ54LS374W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 7801102SA SNJ54LS374W | Samples |
| SNJ54S373FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54S373FK | Samples |
| SNJ54S373J | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54S373J | Samples |
| SNJ54S374FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54S374FK | Samples |
| SNJ54S374J | ACTIVE | CDIP | J | 20 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54S374J | Samples |
| SNJ54S374W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SNJ54S374W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS373, SN54LS373-SP, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 :

- Catalog: [SN74LS373](#), [SN54LS373](#), [SN74LS374](#), [SN74S373](#), [SN74S374](#)
- Military: [SN54LS373](#), [SN54LS374](#), [SN54S373](#), [SN54S374](#)
- Space: [SN54LS373-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS373DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS373NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LS374DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS374DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS374NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS373DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS373NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS374DBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LS374DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS374NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

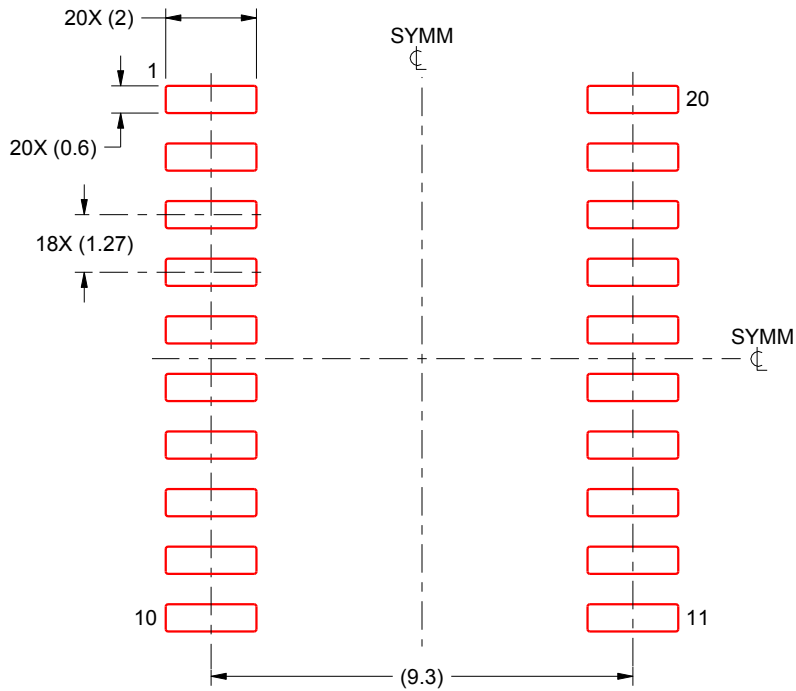
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

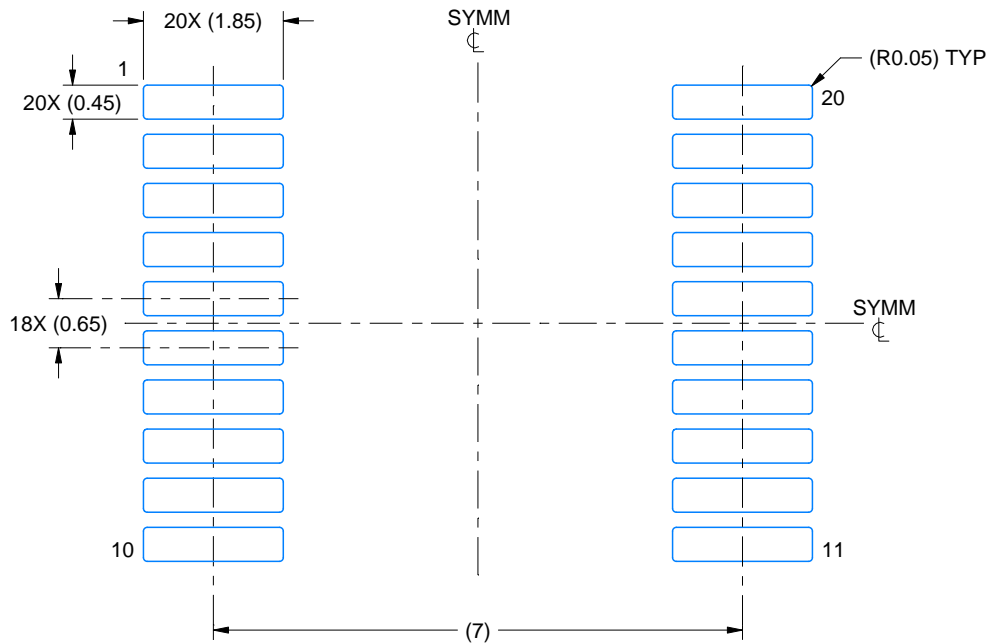
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

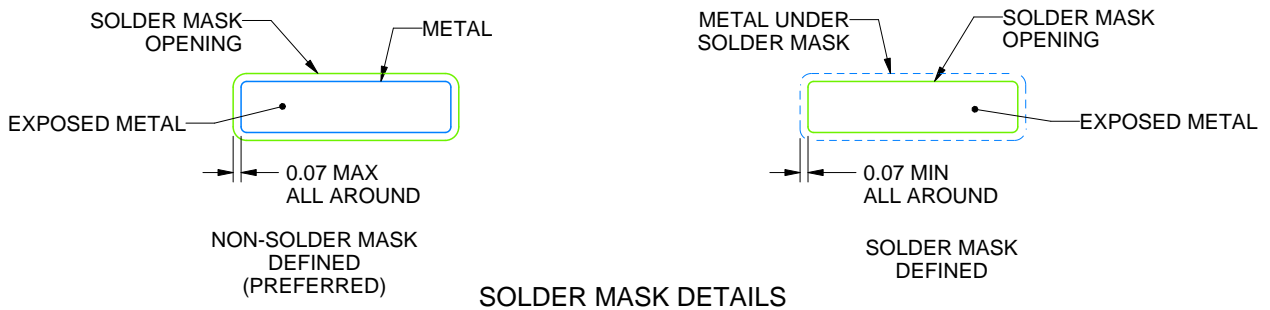
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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