Low Power, High Output Current, Quad Op Amp, Dual-Channel ADSL/ADSL2+ Line Driver

Data Sheet **AD8392A**

FEATURES

- Four current feedback, high current amplifiers
- Ideal for use as ADSL/ADSL2+ dual-channel central office (CO) line drivers
- Low power operation
  - Power supply operation from ±5 V (+10 V) up to ±12 V (+24 V)
  - Less than 3 mA/amp quiescent supply current for full power ADSL/ADSL2+ CO applications (20.4 dBm line power, 5.5 CF)
  - Three active power modes plus shutdown
- High output voltage and current drive
  - 500 mA peak output drive current
  - 42.6 V p-p differential output voltage
- Low distortion
  - −93 dBc @1 MHz second harmonic
  - −103 dBc @ 1 MHz third harmonic
- High speed: 515 V/µs differential slew rate
- Additional functionality of AD8392AACP
  - On-chip, common-mode voltage generation

APPLICATIONS

- ADSL/ADSL2+ CO line drivers
- XDSL line drivers

GENERAL DESCRIPTION

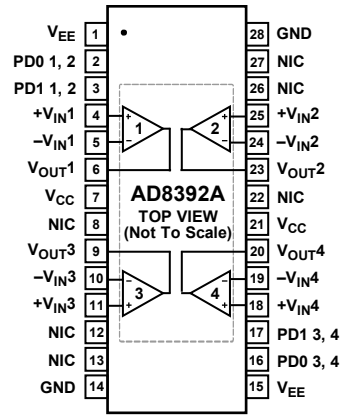
The AD8392A is comprised of four high output current, low power consumption, operational amplifiers. It is particularly well suited for the CO driver interface in digital subscriber line systems, such as ADSL and ADSL2+. The driver is capable of providing enough power to deliver 20.4 dBm to a line, while compensating for losses due to hybrid insertion and back termination resistors.

The AD8392A is available in two thermally enhanced packages, a 28-lead TSSOP_EP (AD8392AARE) and a 5 mm × 5 mm, 32-lead LFCSP (AD8392AACP). Four bias modes are available via the use of two digital bits (PD1, PD0).

Additionally, the AD8392AACP provides V_{COM} pins for on-chip, common-mode voltage generation.

The low power consumption, high output current, high output voltage swing, and robust thermal packaging enable the AD8392A to be used as the CO line drivers in ADSL and other xDSL systems.

PIN CONFIGURATIONS



NOTES
1. NIC = NO INTERNAL CONNECTION.
2. EXPOSED PAD. CONNECT THE EXPOSED PAD TO GROUND PLANE.

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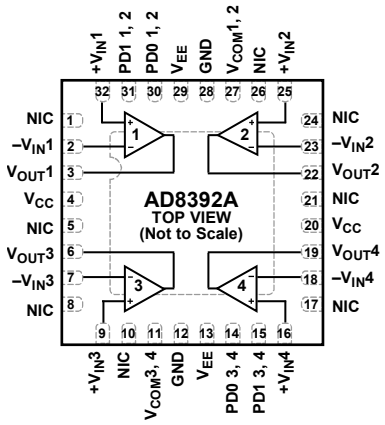
Figure 1. AD8392AARE, 28-Lead TSSOP_EP



NOTES
1. NIC = NO INTERNAL CONNECTION.
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Figure 2. AD8392AACP, 5 mm × 5 mm, 32-Lead LFCSP

Rev. A Document Feedback

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TABLE OF CONTENTS

Features 1
Applications 1
General Description 1
Pin Configurations 1
Revision History 2
Specifications 3
Absolute Maximum Ratings 4
Thermal Resistance 4
ESD Caution 4
Typical Performance Characteristics 5
Theory of Operation 7
Applications 8
Supplies, Grounding, and Layout 8
Power Management 8
Thermal Considerations 8
Typical ADSL/ADSL2+ Application 9
Multitone Power Ratio 10
Outline Dimensions 11
Ordering Guide 11
Notes 12

REVISION HISTORY

6/2016—Rev. 0 to Rev. A

Changed CP-32-2 to CP-32-7 ..... Throughout
Change to Applications Section, Figure 1, and Figure 2 1
Updated Outline Dimensions 12
Changes to Ordering Guide 12

10/2006—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±12 V or +24 V, R_L = 100 Ω, G = +5, PD = (0, 0), T = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	25	37		MHz	V_{OUT} = 0.1 V p-p, R_F = 2 kΩ
−3 dB Large Signal Bandwidth	23	30		MHz	V_{OUT} = 4 V p-p, R_F = 2 kΩ
Peaking		0.06		dB	V_{OUT} = 0.1 V p-p, R_F = 2 kΩ
Slew Rate		515		V/µs	V_{OUT} = 20 V p-p, R_F = 2 kΩ
NOISE/DISTORTION PERFORMANCE					
Second Harmonic Distortion		−93		dBc	f_C = 1 MHz, V_{OUT} = 2 V p-p
Third Harmonic Distortion		−103		dBc	f_C = 1 MHz, V_{OUT} = 2 V p-p
Multitone Input Power Ratio		70		dBc	26 kHz to 2.2 MHz, Z_{LINE} = 100 Ω differential load
Voltage Noise (RTI)		2.5		nV/√Hz	f = 10 kHz
+Input Current Noise		7.6		pA/√Hz	f = 10 kHz
−Input Current Noise		12.5		pA/√Hz	f = 10 kHz
INPUT CHARACTERISTICS					
RTI Offset Voltage	−4	±2	+4	mV	$V_{+IN} - V_{-IN}$
+Input Bias Current		2	7	µA	
−Input Bias Current		3	10	µA	
Input Resistance		8		MΩ	
Input Capacitance		1		pF	
Common-Mode Rejection Ratio	63	66		dB	$(\Delta V_{OS, DM (RTI)})/(\Delta V_{IN, CM})$
OUTPUT CHARACTERISTICS					
Differential Output Voltage Swing	41.2	42.6		V p-p	ΔV_{OUT}
Single-Ended Output Voltage Swing	20.6	21.3		V p-p	ΔV_{OUT}, R_L = 50 Ω
Linear Output Current		500		mA	R_L = 10 Ω, f_C = 100 kHz
POWER SUPPLY					
Operating Range (Dual Supply)	±5		±12	V	
Operating Range (Single Supply)	10		24	V	
Total Quiescent Current					
PD1, PD0 = (0, 0)		5.8	6.5	mA/amp	
PD1, PD0 = (0, 1)		3.0	3.5	mA/amp	
PD1, PD0 = (1, 0)		2.6	3.0	mA/amp	
PD1, PD0 = (1, 1) (Shutdown State)		0.4	0.08	mA/amp	
PD = 0 Threshold			0.8	V	
PD = 1 Threshold	1.8			V	
+Power Supply Rejection Ratio	72	74		dB	$\Delta V_{OS, DM (RTI)}/\Delta V_{CC}$, ΔV_{CC} = ±1 V
−Power Supply Rejection Ratio	65	69		dB	$\Delta V_{OS, DM (RTI)}/\Delta V_{EE}$, ΔV_{EE} = ±1 V

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±13 V (+26 V)
Power Dissipation	See Figure 3
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in the circuit board for surface-mount packages.

Table 3.

Package Type	θ_{JA}	Unit
LFCSP-32 (CP)	27.27	°C/W
TSSOP_EP (RE)	35.33	°C/W

Maximum Power Dissipation

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming that the load (R_L) is midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$).

RMS output voltages should be considered. If R_L is referenced to V_{S-} as in single-supply operation, the total power is $V_S \times I_{OUT}$.

In single supply with R_L to V_{S-}, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the LFCSP-32 and TSSOP_EP packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

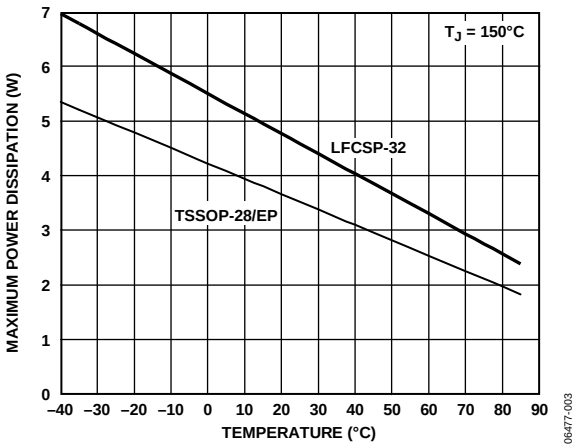

Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

See the Thermal Considerations section for additional thermal design guidance.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

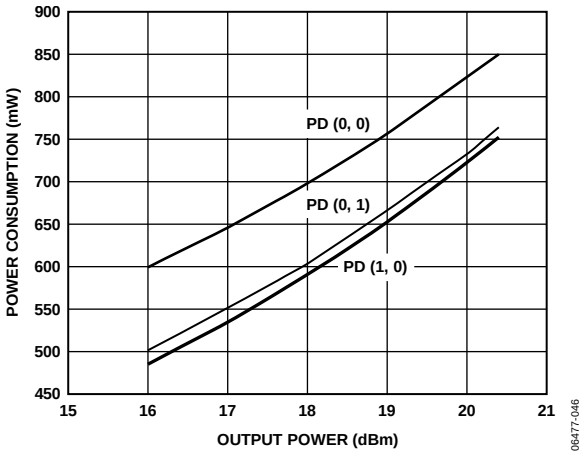

Figure 4. Power Consumption vs. Output Power (138 kHz to 2.2 MHz), ADSL/ADSL2+ Circuit (Figure 15), V_S = ±12 V, R_{LOAD} = 100 Ω, CF = 5.5

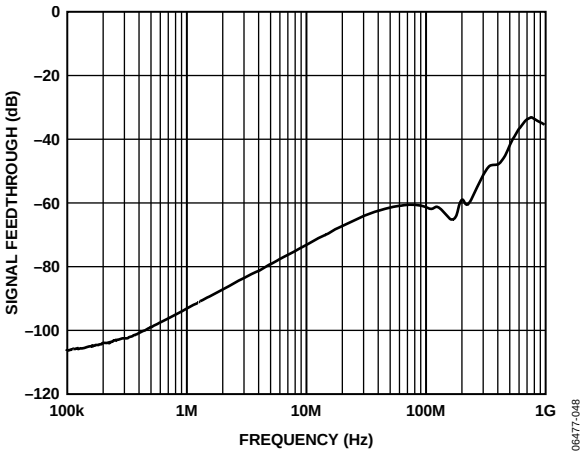

Figure 7. Signal Feedthrough vs. Frequency
V_S = ±12 V, G = +5, V_{IN} = 800 mV p-p, PD (1, 1), R_F = 2 kΩ

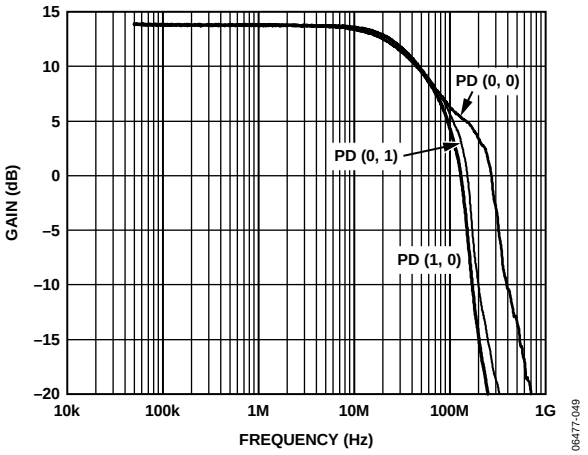

Figure 5. Small Signal Frequency Response
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 100 mV p-p, R_F = 2 kΩ

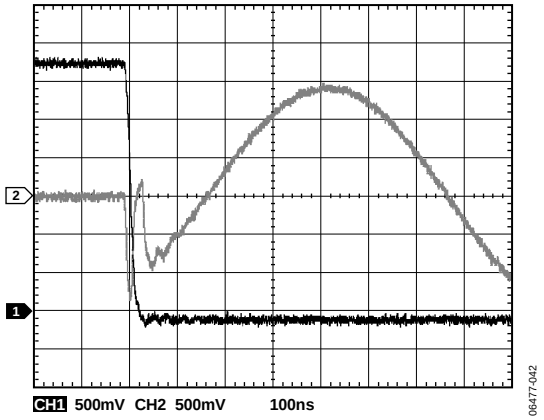

Figure 8. Power-Up Time: PD (1, 1) to PD (0, 0)
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 1 V p-p, R_F = 2 kΩ

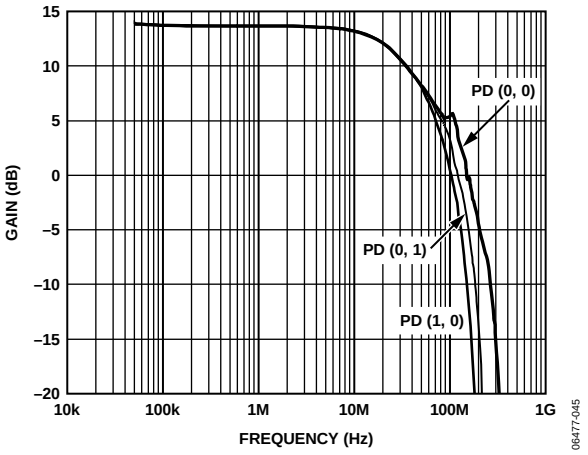

Figure 6. Large Signal Frequency Response
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 4 V p-p, R_F = 2 kΩ

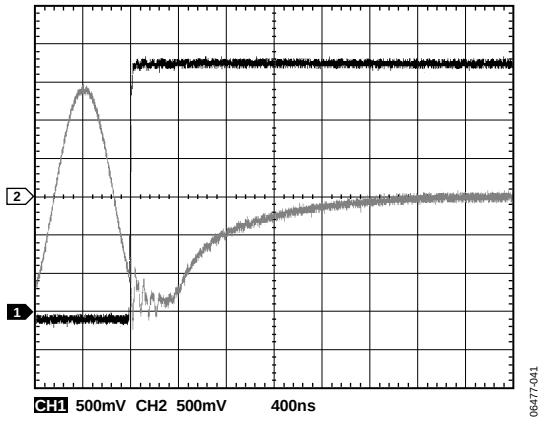

Figure 9. Power-Down Time: PD (0, 0) to PD (1, 1)
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 1 V p-p, R_F = 2 kΩ

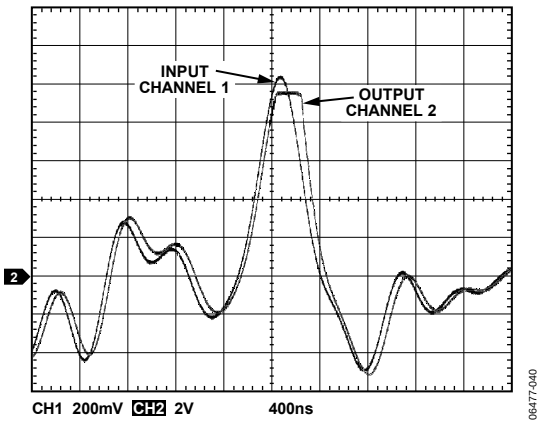

Figure 10. Output Overdrive Recovery, ADSL/ADSL2+ Circuit (Figure 15), DMT Waveform, $V_S = \pm 12$ V

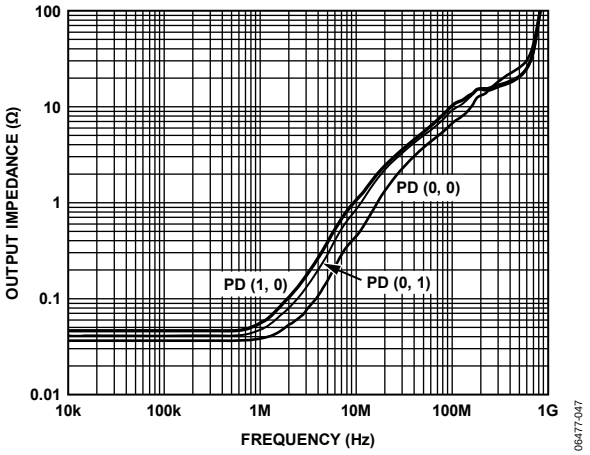

Figure 13. Output Impedance vs. Frequency $V_S = \pm 12$ V, $G = +5$, $R_F = 2$ kΩ

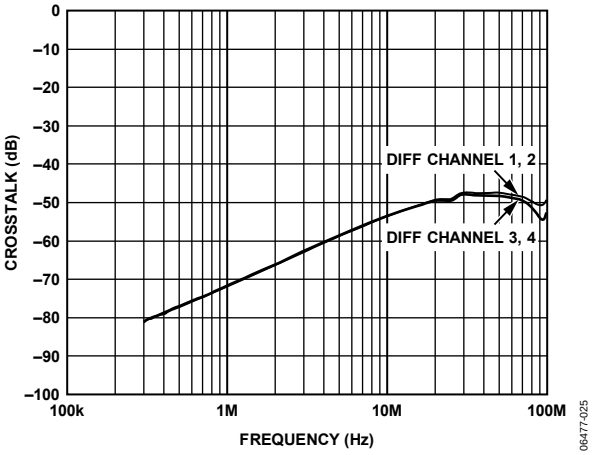

Figure 11. Crosstalk vs. Frequency, Dual Differential Driver Circuit (Figure 14), $V_S = \pm 12$ V, $V_{IN} = 800$ mV p-p

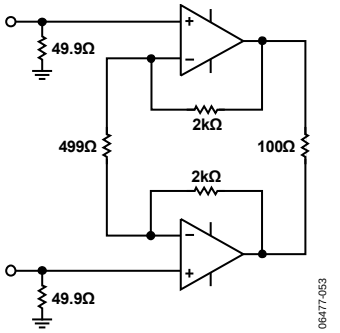

Figure 14. Dual Differential Driver Circuit

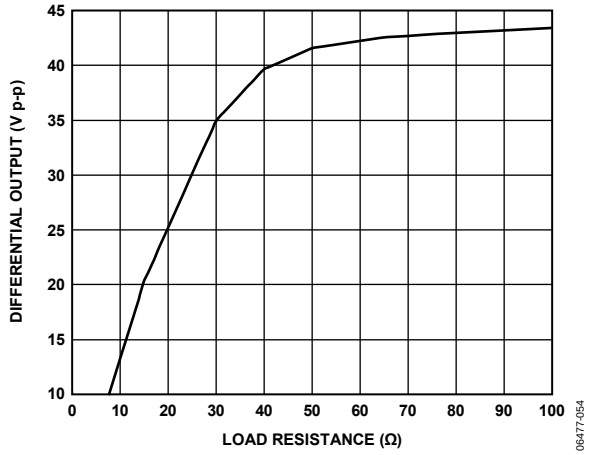

Figure 12. Differential Output Swing vs. R_{LOAD} Dual Differential Driver Circuit (Figure 14)

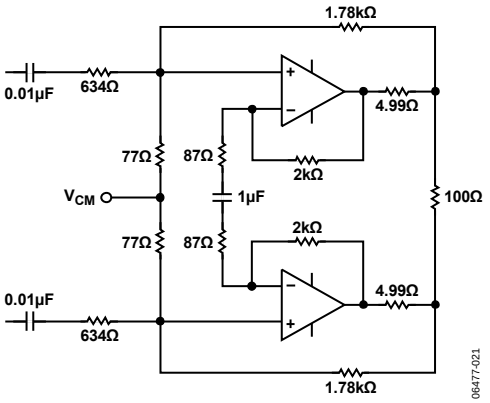

Figure 15. ADSL/ADSL2+ Circuit

THEORY OF OPERATION

The AD8392A is a current feedback amplifier with high (500 mA) output current capability. With a current feedback amplifier, the current into the inverting input is the feedback signal, and the open-loop behavior is that of a transimpedance, dV_O/dI_{IN} or T_Z.

The open-loop transimpedance is analogous to the open-loop voltage gain of a voltage feedback amplifier. Figure 16 shows a simplified model of a current feedback amplifier. Because R_{IN} is proportional to $1/g_m$, the equivalent voltage gain is $T_Z \times g_m$, where g_m is the transconductance of the input stage. Basic analysis of the follower with gain circuit yields

$$\frac{V_O}{V_{IN}} = G \times \frac{T_Z(S)}{T_Z(S) + G \times R_{IN} + R_F}$$

where:

$$G = 1 + \frac{R_F}{R_G}$$

$$R_{IN} = \frac{1}{g_m} \approx 50\ \Omega$$

Because $G \times R_{IN} << R_F$ for low gains, a current feedback amplifier has relatively constant bandwidth vs. gain, the 3 dB point being set when $|T_Z| = R_F$.

Of course, for a real amplifier there are additional poles that contribute excess phase, and there is a value for R_F below which the amplifier is unstable. Tolerance for peaking and desired flatness determines the optimum R_F in each application.

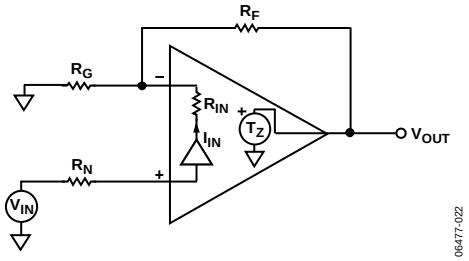

Figure 16. Simplified Block Diagram

The AD8392A is capable of delivering 500 mA of output current while swinging to within 2 V of either power supply rail. The AD8392A also has a power management system included on-chip. It features four user-programmable power levels (three active power modes as well as the provision for complete shutdown).

APPLICATIONS

SUPPLIES, GROUNDING, AND LAYOUT

The AD8392A can be powered from either single or dual supplies, with the total supply voltage ranging from 10 V to 24 V. For optimum performance, a well regulated low ripple supply should be used.

As with all high speed amplifiers, close attention should be paid to supply decoupling, grounding, and overall board layout. Low frequency supply decoupling should be provided with 10 µF tantalum capacitors from each supply to ground. In addition, all supply pins should be decoupled with 0.1 µF quality ceramic chip capacitors placed as close as possible to the driver. An internal low impedance ground plane should be used to provide a common ground point for all driver and decoupling capacitor ground requirements. Whenever possible, separate ground planes should be used for analog and digital circuitry.

High speed layout techniques should be followed to minimize parasitic capacitance around the inverting inputs. Some practical examples of these techniques are keeping feedback traces as short as possible and clearing away ground plane in the area of the inverting inputs. Input and output traces should be kept short and as far apart from each other as practical to avoid crosstalk. When used as a differential driver, all differential signal traces should be kept as symmetrical as possible.

POWER MANAGEMENT

The AD8392A can be configured in any of three active bias states as well as a shutdown state via the use of two sets of digitally programmable logic pins. Pin PD0 (1, 2) and Pin PD1 (1, 2) control Amplifier 1 and Amplifier 2, while PD0 (3, 4) and Pin PD1 (3, 4) control Amplifier 3 and Amplifier 4. These pins can be controlled directly with either 3.3 V or 5 V CMOS logic by using the GND pins as a reference. If left unconnected, the PD pins float low, placing the amplifier in the full bias mode. Refer to the Specifications for the per amplifier quiescent current for each of the available bias states.

As is shown in Figure 13, the AD8392A exhibits low output impedance for the three active states. The shutdown state (PD1, PD0 = 1, 1) provides a high impedance output.

THERMAL CONSIDERATIONS

When using a quad, high output current amplifier, such as the AD8392A, special consideration should be given to system level thermal design. In applications such as the ADSL/ADSL2+, the AD8392A could be required to dissipate as much as 1.4 W or more on-chip. Under these conditions, particular attention should be paid to the thermal design to maintain safe operating temperatures on the die. To aid in the thermal design, the thermal information in the Thermal Resistance section can be combined with what follows here.

The information in Table 3 and Figure 3 is based on a standard JEDEC 4-layer board and a maximum die temperature of 150°C. To provide additional guidance and design suggestions, a thermal study was performed under a set of conditions more closely aligned with an actual ADSL/ADSL2+ application.

In a typical ADSL/ADSL2+ line card, component density usually dictates that most of the copper plane used for thermal dissipation be internal. Additionally, each ADSL/ADSL2+ port may be allotted only 1 square inch, or even less, of board space. For these reasons, a special thermal test board was constructed for this study. The 4-layer board measured approximately 4 inches × 4 inches and contained two internal 1 oz copper ground planes, each measuring 2 inches × 3 inches. The top layer contained signal traces and an exposed copper strip ¼ inch × 3 inches to accommodate heat sinking, with no other copper on the top or bottom of the board.

Three 28-lead TSSOPs were placed on the board representing six ADSL channels, or one channel per square inch of copper, with each channel dissipating 700 mW on-chip (1.4 W per package). The die temperature is then measured in still air and in a wind tunnel with calibrated airflow of 100 LFM, 200 LFM, and 400 LFM. Figure 17 shows the power dissipation vs. the ambient temperature for each airflow condition. The figure assumes a maximum die temperature of 135°C. No heat sink was used.

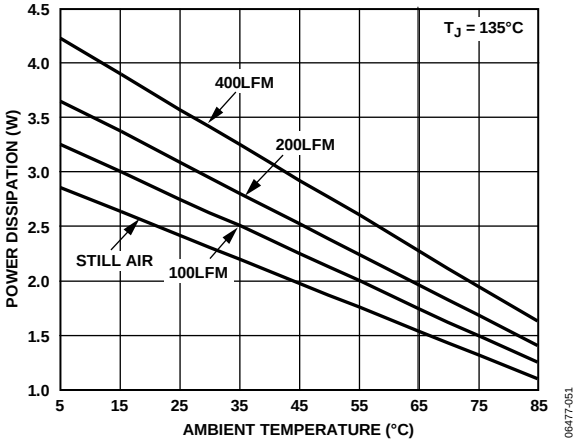

Figure 17. Power Dissipation vs. Ambient Temperature and Air Flow 28-Lead TSSOP/EP

This data is only provided as guidance to assist in the thermal design process. Due diligence should be performed with regards to power dissipation because there are many factors that can affect thermal performance.

TYPICAL ADSL/ADSL2+ APPLICATION

In a typical ADSL/ADSL2+ application, a differential line driver is used to take the signal from the analog front end (AFE) and drive it onto the twisted pair telephone line. Referring to the typical circuit representation in Figure 18, the differential input appears at V_{IN+} and V_{IN-} from the AFE, while the differential output is transformer coupled to the telephone line at tip and ring. The common-mode operating point, generally midway between the supplies, is set through V_{COM}.

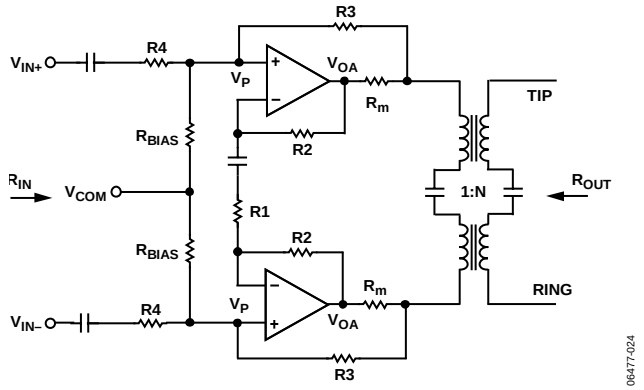

Figure 18. Typical ADSL/ADSL2+ Application Circuit

In ADSL/ADSL2+ applications, it is common practice to conserve power by using positive feedback to synthesize the output resistance, thereby lowering the required ohmic value of the line matching resistors, R_m. The circuit in Figure 18 is somewhat unique in that the positive feedback introduced via R3 has the effect of synthesizing the input resistance as well. The following definitions and equations can be used to calculate the resistor values necessary to obtain the desired gain, input resistance, and output resistance for a given application. For simplicity, the following calculations assume a lossless transformer.

The following values are used in the design equations and are assumed already known or chosen by the designer.

Value	Definition
V_{IN}	Differential input voltage
R_{IN}	Desired differential input resistance
N	Transformer turns ratio
V_{LINE}	Differential output voltage at tip and ring
R_m	Each is typically 5% to 15% of the transformer reflected line impedance
$R2$	Recommended in the amplifier data sheet
V_P	Voltage at the + inputs to the amplifier, approximately ½ V_{IN} (must be less than V_{IN} for positive input resistance)
R_L	Transformer reflected line impedance

Additional definitions for calculating resistor values include:

Value	Definition
V_{OA}	Voltage at the amplifier outputs
K	Matching resistance reduction factor
A_V	Gain from V_{IN} to transformer primary
β	Negative feedback factor
α	Positive feedback factor

Note: R1 must be calculated before β and α.

$$V_{OA} = \frac{V_{LINE}(1+k)}{N} \qquad k = \frac{2R_m}{R_L} \qquad A_V = \frac{V_{LINE}}{N V_{IN}}$$

$$\beta = \frac{R1}{R1+2R2} \qquad \alpha = \beta(1-k)$$

With the above known quantities and definitions, the remaining resistors can readily be calculated.

$$R1 = \frac{2V_P R2}{V_{OA} - V_P}$$

$$R4 = \frac{R_{IN}(V_{IN} - V_P)}{2V_{IN}}$$

$$R3 = \frac{A_V R4\left(2R1R_m + R1R_L - \alpha R1R_L - 2\alpha R2R_L\right)}{\alpha R_L(R1+2R2)}$$

$$R_{BIAS} = \frac{\alpha R3R4}{R4 - \alpha(R3+R4)}$$

After building the circuit with the closest 1% resistor values, the actual gain, input resistance, and output resistance can be verified with the following equations.

$$GAIN_{(V_{IN}\ to\ LINE)} = \frac{N}{\beta(k+1)\left(1 + \frac{R4}{R3} + \frac{R4}{R_{BIAS}}\right) - \frac{R4}{R3}}$$

$$R_{IN} = \frac{2}{\frac{1}{R4} - A_V\beta\left(\frac{2R_m + R_L}{R4R_L}\right)}$$

$$R_{OUT} = \frac{2R_m N^2}{1 - \left(\frac{R4R_{BIAS}}{R1(R4+R_{BIAS})}\right)\left(\frac{R1+2R2}{R3 + \frac{R4R_{BIAS}}{R4+R_{BIAS}}}\right)}$$

MULTITONE POWER RATIO

The DMT signal used in ADSL/ADSL2+ systems carries data in discrete tones or bins, which appear in the frequency domain in evenly spaced 4.3125 kHz intervals. In applications using this type of waveform, multitone power ratio (MTPR) is a commonly used measure of linearity. MTPR is defined as the measured difference from the peak of one tone that is loaded with data to the peak of an adjacent tone that is intentionally left empty. Figure 19 and Figure 20 show the AD8392A MTPR for a 5.5 crest factor waveform for empty bins in the ADSL and extended ADSL2+ bandwidths.

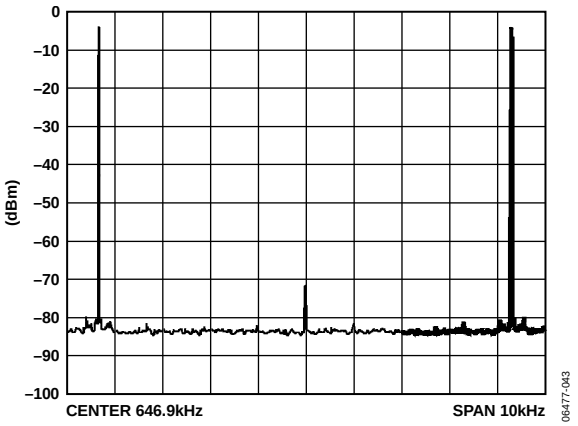

Figure 19. MTPR at 647 kHz

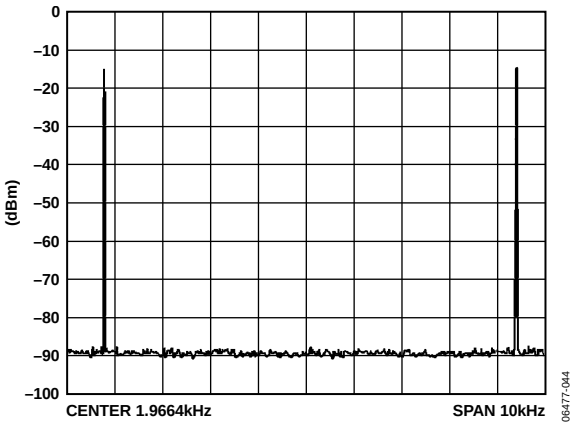

Figure 20. MTPR at 1.966 MHz

OUTLINE DIMENSIONS

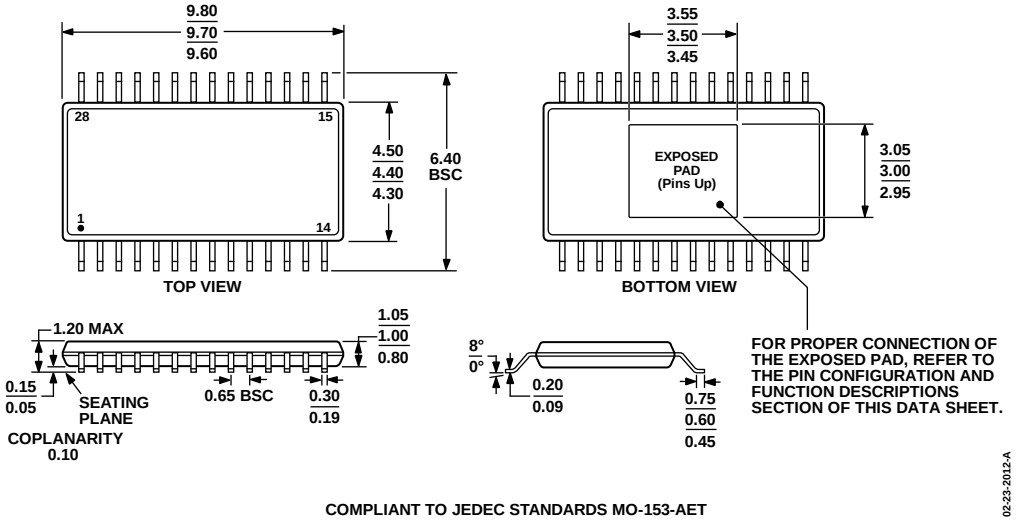

Figure 21. 28-Lead Thin Shrink Small Outline with Exposed Pad [TSSOP_EP]
(RE-28-1)
Dimensions shown in millimeters

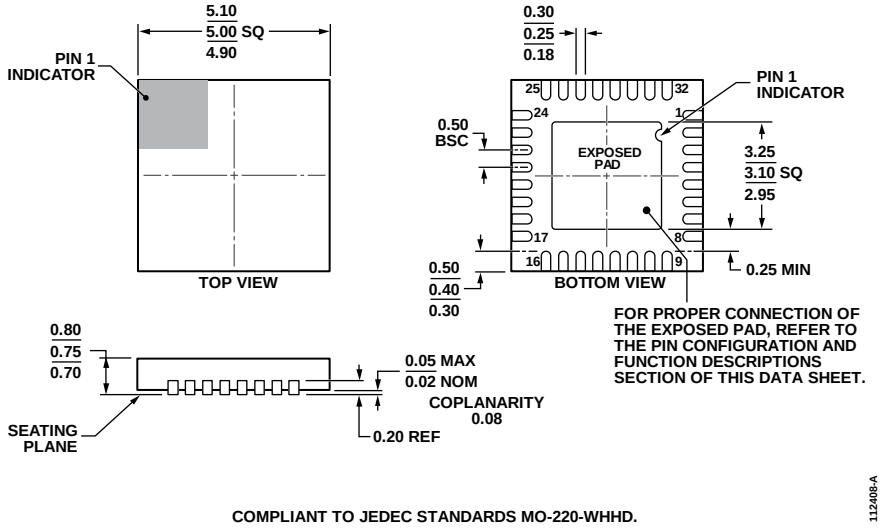

Figure 22. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8392AAREZ	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP_EP)	RE-28-1
AD8392AAREZ-RL	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP_EP)	RE-28-1
AD8392AAREZ-R7	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP_EP)	RE-28-1
AD8392AACPZ-R2	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP)	CP-32-7
AD8392AACPZ-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP)	CP-32-7
AD8392AACPZ-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP)	CP-32-7

[1] Z = RoHS Compliant Part.

NOTES

D06477-0-6/16(A)

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AD8392AACPZ-R2