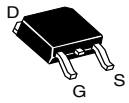
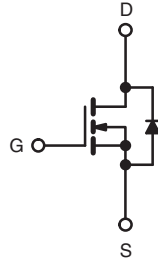
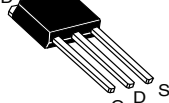


Power MOSFET

| PRODUCT SUMMARY | |
|---------------------------|----------------------------|
| V_{DS} (V) | 200 |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10\text{ V}$ 1.5 |
| Q_g (Max.) (nC) | 8.2 |
| Q_{gs} (nC) | 1.8 |
| Q_{gd} (nC) | 4.5 |
| Configuration | Single |

 DPAK
(TO-252)

 IPAK
(TO-251)


N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR210, SiHFR210)
- Straight Lead (IRFU210, SiHFU210)
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

| ORDERING INFORMATION | | | | | |
|---------------------------------|---------------|------------------------------|---------------------------|------------------------------|---------------|
| Package | DPAK (TO-252) | DPAK (TO-252) | DPAK (TO-252) | DPAK (TO-252) | IPAK (TO-251) |
| Lead (Pb)-free and Halogen-free | SiHFR210-GE3 | SiHFR210TRL-GE3 ^a | - | SiHFR210TRR-GE3 ^a | SiHFU210-GE3 |
| Lead (Pb)-free | IRFR210PbF | IRFR210TRLPbF ^a | IRFR210TRPbF ^a | - | IRFU210PbF |
| | SiHFR210-E3 | SiHFR210TL-E3 ^a | SiHFR210T-E3 ^a | - | SiHFU210-E3 |

Note

- a. See device orientation.

| ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | |
|---|----------------------------------|-----------------------------------|---------------|---------------------|
| PARAMETER | SYMBOL | | LIMIT | UNIT |
| Drain-Source Voltage | V_{DS} | | 200 | V |
| Gate-Source Voltage | V_{GS} | | ± 20 | |
| Continuous Drain Current | V_{GS} at 10 V | $T_C = 25\text{ }^\circ\text{C}$ | 2.6 | A |
| | | $T_C = 100\text{ }^\circ\text{C}$ | 1.7 | |
| Pulsed Drain Current ^a | I_{DM} | | 10 | W/ $^\circ\text{C}$ |
| Linear Derating Factor | | | 0.20 | |
| Linear Derating Factor (PCB Mount) ^e | | | 0.020 | |
| Single Pulse Avalanche Energy ^b | E_{AS} | | 95 | mJ |
| Avalanche Current ^a | I_{AR} | | 2.7 | A |
| Repetitive Avalanche Energy ^a | E_{AR} | | 2.5 | mJ |
| Maximum Power Dissipation | $T_C = 25\text{ }^\circ\text{C}$ | | 25 | W |
| | $T_A = 25\text{ }^\circ\text{C}$ | | 2.5 | |
| Peak Diode Recovery dV/dt ^c | dV/dt | | 5.0 | V/ns |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | | - 55 to + 150 | $^\circ\text{C}$ |
| Soldering Recommendations (Peak Temperature) ^d | for 10 s | | 260 | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 28\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 2.6\text{ A}$ (see fig. 12).
 c. $I_{SD} \leq 2.6\text{ A}$, $di/dt \leq 70\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
 d. 1.6 mm from case.
 e. When mounted on 1" square PCB (FR-4 or G-10 material).



| THERMAL RESISTANCE RATINGS | | | | | |
|--|------------|------|------|------|------|
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R_{thJA} | - | - | 110 | °C/W |
| Maximum Junction-to-Ambient (PCB Mount) ^a | R_{thJA} | - | - | 50 | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | - | 5.0 | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|---------------------|--|--|------|------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 200 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$ | | - | 0.30 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 25 | μA |
| | | $V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 1.6\text{ A}^b$ | - | - | 1.5 | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = 50\text{ V}, I_D = 1.6\text{ A}^b$ | | 0.80 | - | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5 | | - | 140 | - | μF |
| Output Capacitance | C_{oss} | | | - | 53 | - | |
| Reverse Transfer Capacitance | C_{rss} | | | - | 15 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 3.3\text{ A}, V_{DS} = 160\text{ V}$, see fig. 6 and 13 ^b | - | - | 8.2 | nC |
| Gate-Source Charge | Q_{gs} | | | - | - | 1.8 | |
| Gate-Drain Charge | Q_{gd} | | | - | - | 4.5 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 100\text{ V}, I_D = 3.3\text{ A}, R_g = 24\text{ }\Omega, R_D = 30\text{ }\Omega$, see fig. 10 ^b | | - | 8.2 | - | ns |
| Rise Time | t_r | | | - | 17 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 14 | - | |
| Fall Time | t_f | | | - | 8.9 | - | |
| Internal Drain Inductance | L_D | Between lead, 6 mm (0.25") from package and center of die contact | | - | 4.5 | - | nH |
| Internal Source Inductance | L_S | | | - | 7.5 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode | | - | - | 2.6 | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | | - | - | 10 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 2.6\text{ A}, V_{GS} = 0\text{ V}^b$ | | - | - | 2.0 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = 3.3\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$ | | - | 150 | 310 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | - | 0.60 | 1.4 | μC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

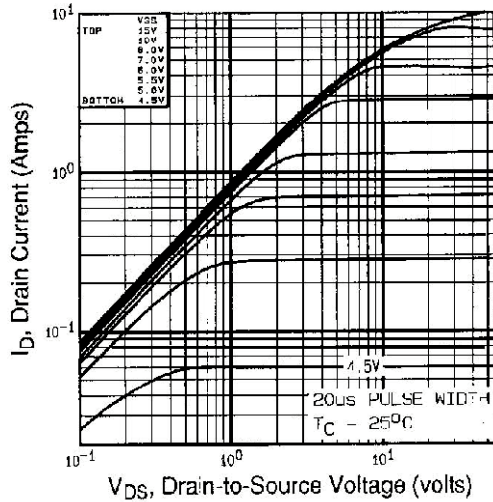


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

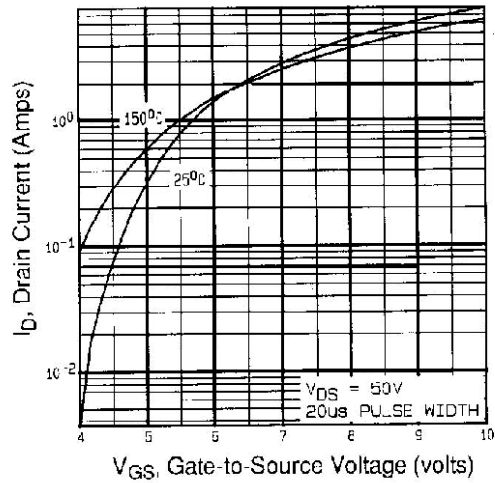


Fig. 3 - Typical Transfer Characteristics

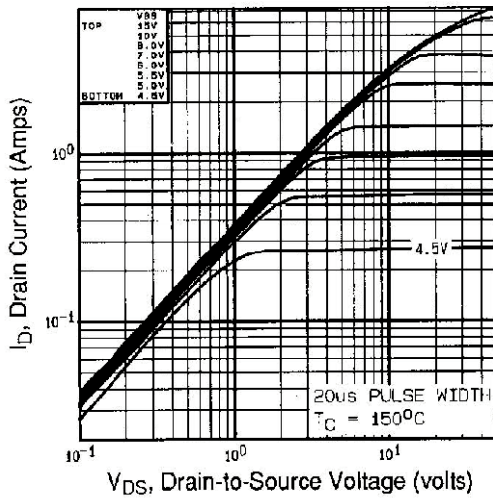


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

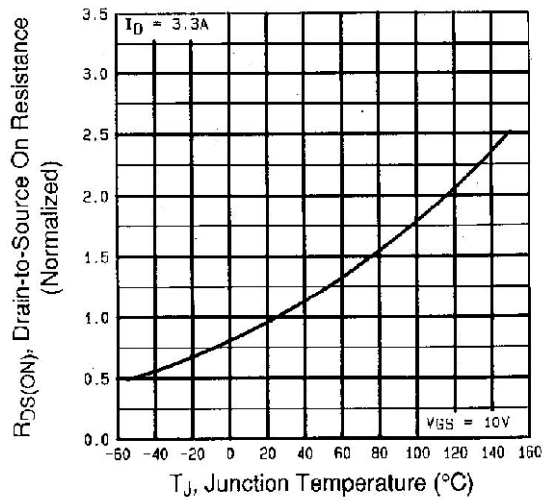


Fig. 4 - Normalized On-Resistance vs. Temperature

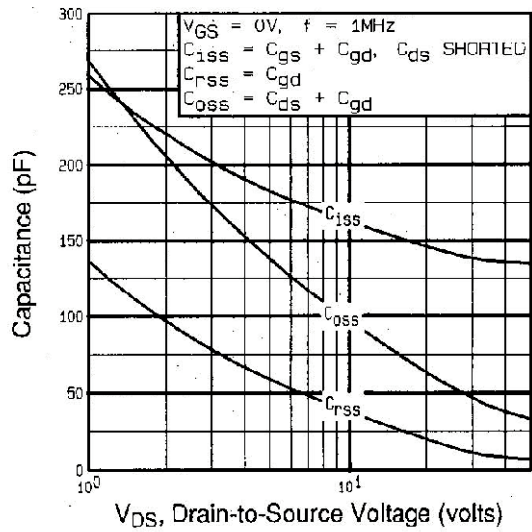


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

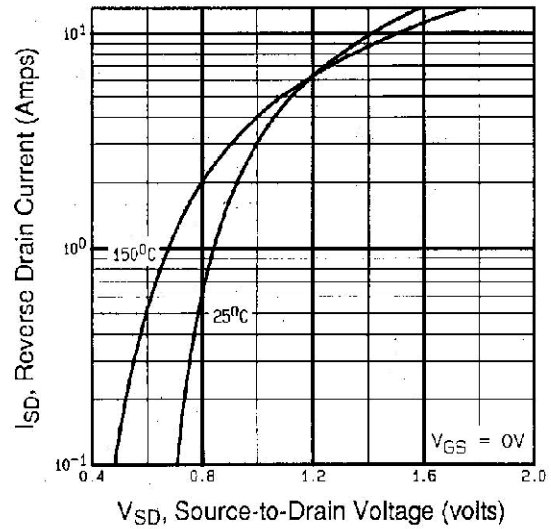


Fig. 7 - Typical Source-Drain Diode Forward Voltage

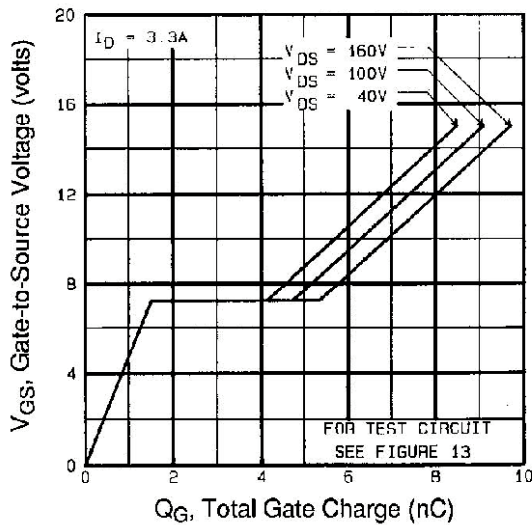


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

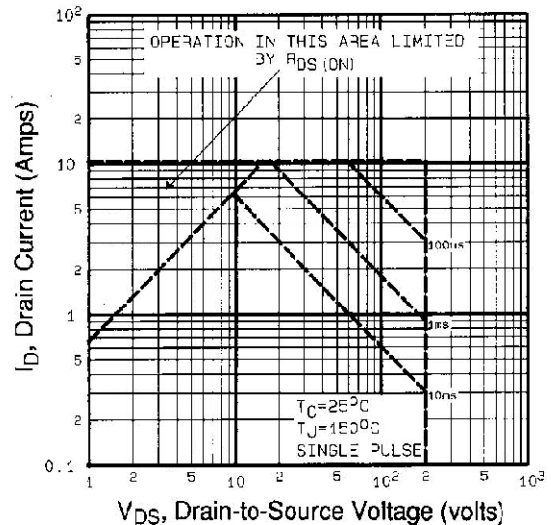


Fig. 8 - Maximum Safe Operating Area

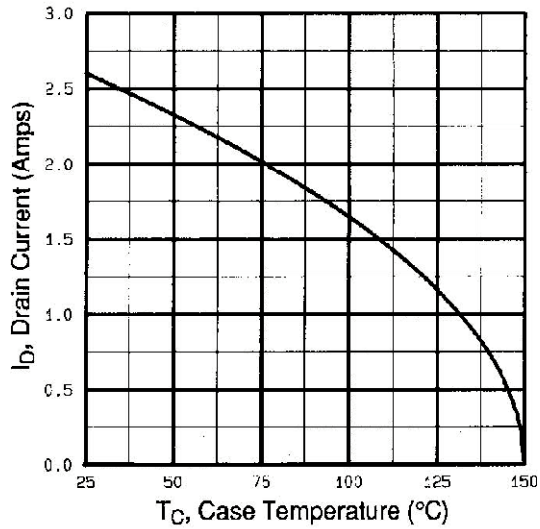


Fig. 9 - Maximum Drain Current vs. Case Temperature

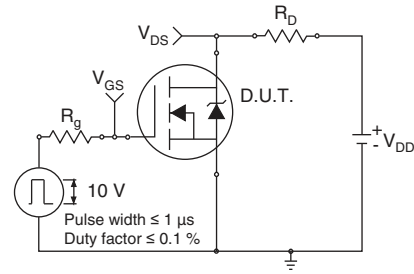


Fig. 10a - Switching Time Test Circuit

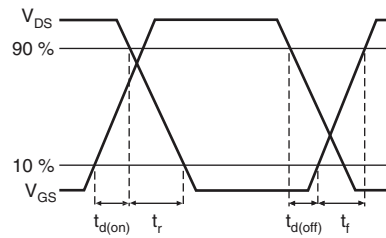


Fig. 10b - Switching Time Waveforms

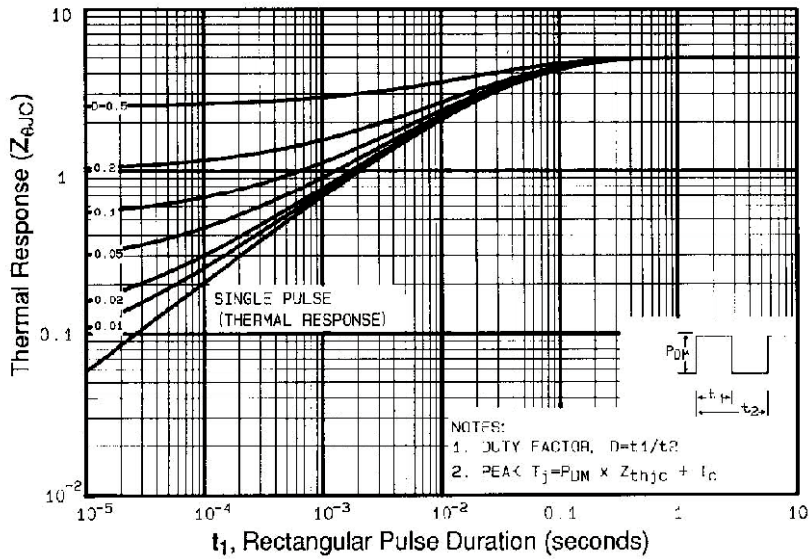


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

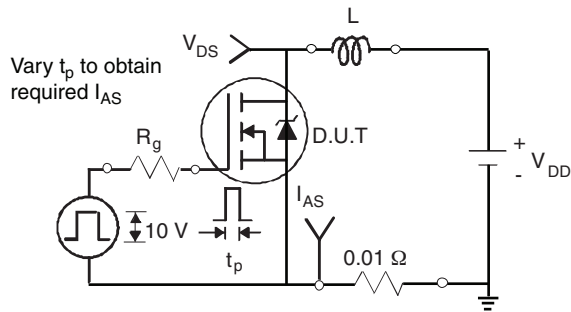


Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms

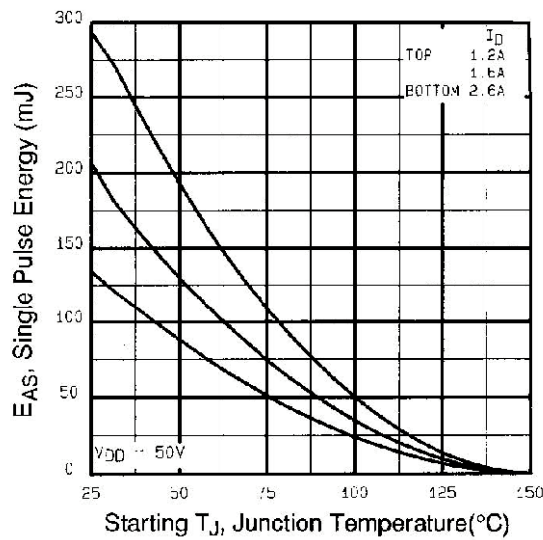


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

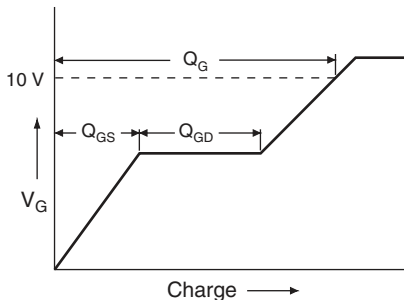


Fig. 13a - Basic Gate Charge Waveform

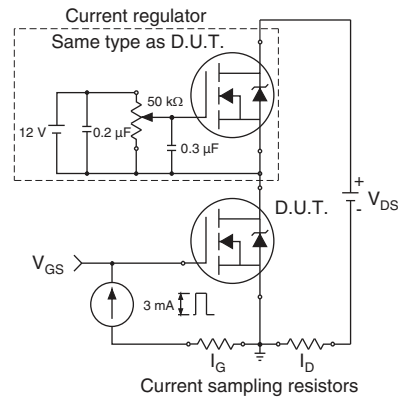
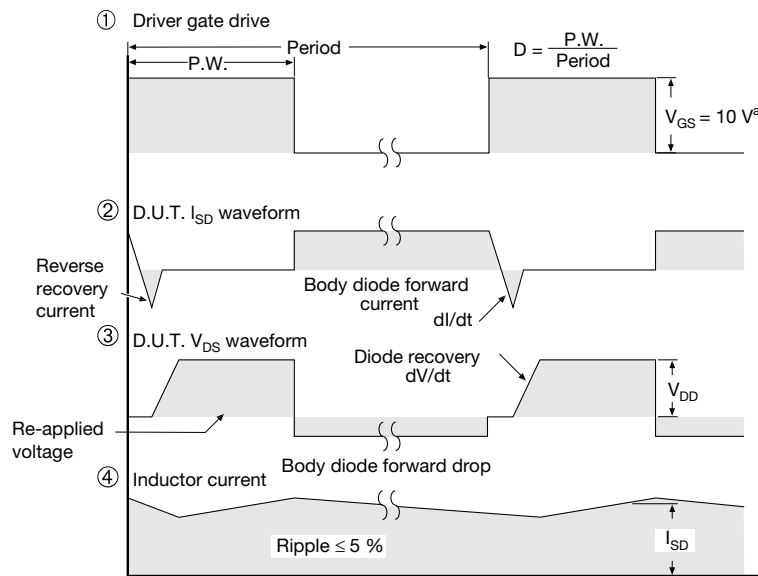
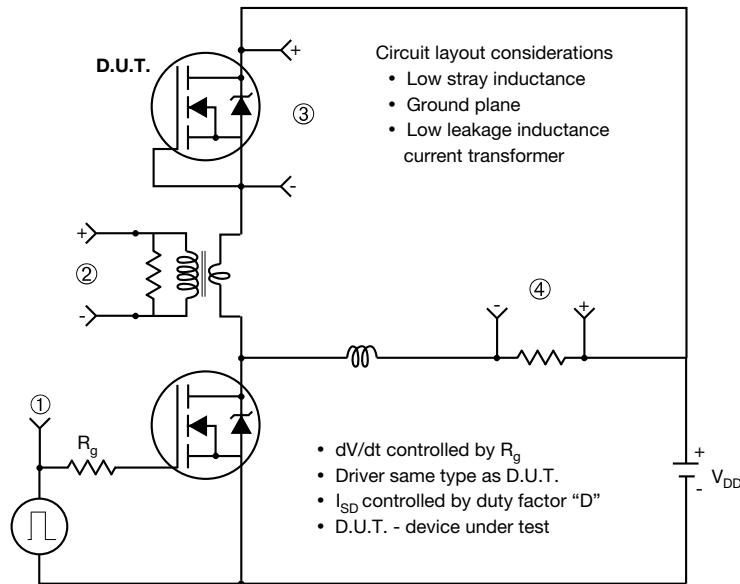


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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TO-252AA Case Outline



| DIM. | MILLIMETERS | | INCHES | |
|--|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 2.18 | 2.38 | 0.086 | 0.094 |
| A1 | - | 0.127 | - | 0.005 |
| b | 0.64 | 0.88 | 0.025 | 0.035 |
| b2 | 0.76 | 1.14 | 0.030 | 0.045 |
| b3 | 4.95 | 5.46 | 0.195 | 0.215 |
| C | 0.46 | 0.61 | 0.018 | 0.024 |
| C2 | 0.46 | 0.89 | 0.018 | 0.035 |
| D | 5.97 | 6.22 | 0.235 | 0.245 |
| D1 | 4.10 | - | 0.161 | - |
| E | 6.35 | 6.73 | 0.250 | 0.265 |
| E1 | 4.32 | - | 0.170 | - |
| H | 9.40 | 10.41 | 0.370 | 0.410 |
| e | 2.28 BSC | | 0.090 BSC | |
| e1 | 4.56 BSC | | 0.180 BSC | |
| L | 1.40 | 1.78 | 0.055 | 0.070 |
| L3 | 0.89 | 1.27 | 0.035 | 0.050 |
| L4 | - | 1.02 | - | 0.040 |
| L5 | 1.01 | 1.52 | 0.040 | 0.060 |
| ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347 | | | | |

Notes

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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