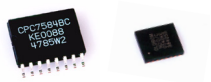
CPC7584

Line Card Access Switch



Features

- Small 16-pin SOIC or micro-leadframe package
- Micro-leadframe package (MLP) printed circuit board footprint is 70% smaller than 4TH generation EMRs and 60% smaller than SOIC version
- Monolithic IC reliability
- Low matched R_{ON}
- Eliminates the need for zero cross switching
- Flexible switch timing to transition from ringing mode to talk mode.
- Clean, bounce free switching
- Tertiary protection consisting of integrated current limiting, voltage clamping, and thermal shutdown for SLIC protection
- 5V operation with power consumption < 10 mW
- Intelligent battery monitor
- Latched logic level inputs, no external drive circuitry required

Applications

- Central office (CO)
- Digital Loop Carrier (DLC)
- PBX Systems
- Digitally Added Main Line (DAML)
- Hybrid Fiber Coax (HFC)
- Fiber in the Loop (FITL)
- Pair Gain System
- Channel Banks

Description

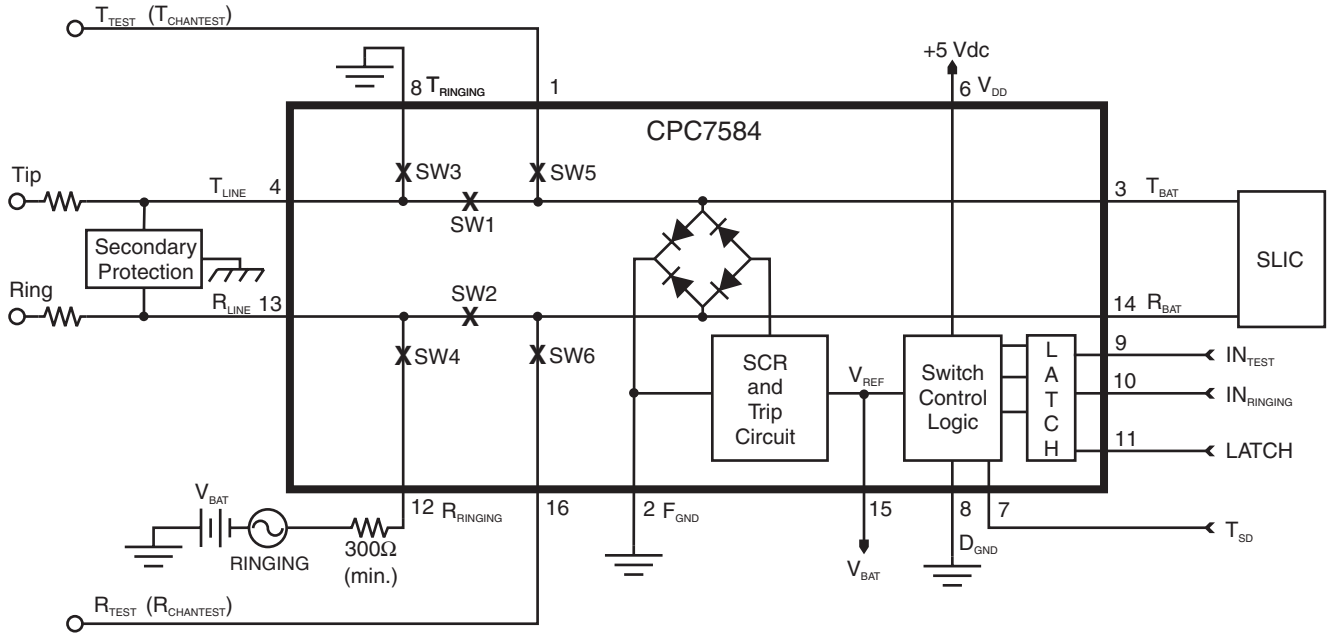
The CPC7584 is a monolithic solid state switch in a 16-pin SOIC or MLP surface mount package. It provides the necessary functions to replace two 2-Form-C electro-mechanical relays on traditional analog and integrated voice and data (IVD) line cards found in Central Office, Access, and PBX equipment. The device contains solid state switches for tip and ring line break, ringing injection/ringing return and channel test access. The CPC7584 requires only a +5V supply and offers “break-before-make” or “make-before-break” switch operation using simple logic-level input control.

The CPC7584xC logic differs from the CPC7584xA/B with an enhancement permitting channel monitoring in the test state. See “Functional Description” on page 9 for more information. The CPC7584xC also has a higher trigger and hold current for the protection SCR. Specify CPC7584Bx for SOIC or specify CPC7582Mx for MLP devices shipped in tubes. Append the part number with the suffix TR for tape and reel packaging.

Ordering Information

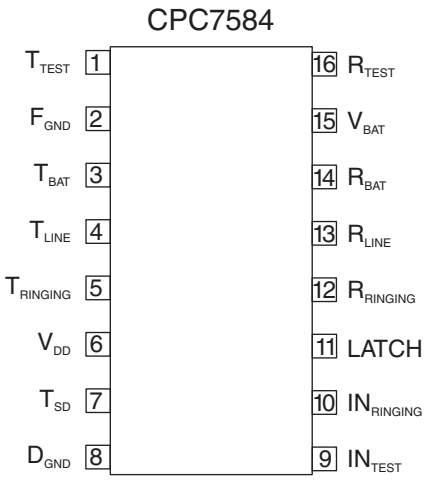
Part Number	Description
CPC7584xA	With protection SCR
CPC7584xB	Without protection SCR
CPC7584xC	With protection SCR and “Monitor” test state

Figure 1. CPC7584 Block Diagram



1. Specifications

1.1 Package Pinout



1.2 Pinout

Pin	Name	Description
1	T_{TEST}	Connect to Tip lead of test bus
2	F_{GND}	Fault ground
3	T_{BAT}	Connect to tip lead of SLIC
4	T_{LINE}	Connect to tip lead of the line (drop)
5	$T_{RINGING}$	Connect to ringing generator return
6	V_{DD}	+5 V supply
7	T_{SD}	Temperature shutdown indicator pin. Bi-directional I/O with internal pull up to V_{DD}. Output function indicates status of thermal shutdown circuitry, Input function can be used to set the “All-Off” mode using an open-drain type output.
8	D_{GND}	Digital ground
9	IN_{TEST}	Logic-level switch control input
10	$IN_{RINGING}$	Logic-level switch control input
11	LATCH	Data latch control, active high, transparent low
12	$R_{RINGING}$	Connect to ringing generator current limiting resistor
13	R_{LINE}	Connect to ring lead of the line (drop)
14	R_{BAT}	Connect to ring lead of the SLIC
15	V_{BAT}	Connect to ring lead of SLIC
16	R_{TEST}	Battery voltage supply. Must be capable of sourcing the trigger current for proper operation of the protection SCR.

1.3 Absolute Maximum Ratings (at 25° C)

Parameter	Minimum	Maximum	Unit
Operating temperature	-40	+110	°C
Storage temperature	-40	+150	°C
Operating relative humidity	5	95	%
Pin soldering temperature (10 seconds max)	-	+260	°C
+5 V power supply	-0.3	7	V
Battery Supply	-	-85	V
Logic input voltage	-0.3	V_{DD}+0.3	V
Logic input to switch output isolation	-	330	V
Switch isolation (SW1, SW2, SW3, SW5, SW6)	-	330	V
Switch Isolation (SW4)	-	465	V

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4.1 Power Supply Specifications

Supply	Minimum	Typical	Maximum	Unit
V_{DD}	+4.5	+5.0	+5.5	V
V_{BAT}[1]	-19	-	-72	V

[1] V_{BAT} is used only for internal protection circuitry. If V_{BAT} rises above -10 V, the device will enter and remain in the all-off state until the battery exceeds -15 V.

ESD Rating (Human Body Model)
1000 V

1.4 Electrical Characteristics, T_A = -40° C to +85° C

Unless otherwise specified:
Minimum and maximum values are production testing requirements. Typical values are provided for information purposes only and are not part of the testing requirements. They are characteristic of the device and are the result of engineering evaluations.
V_{DD} = +5V_{dc} and V_{BAT} = -48V_{dc}

1.4.2 Break Switches, SW1 and SW2

Parameter	Conditions		Symbol	Minimum	Typical	Maximum	Unit
Open Contact Isolation - Off-state leakage current	V_{SW1} = T_{LINE} to T_{BAT} V_{SW2} = R_{LINE} to R_{BAT}						
	V_{SW} = -320V to GND V_{SW} = +260 V to -60 V	+25°C	I_{SW}	-	0.1	1	µA
	V_{SW} = -330V to GND V_{SW} = +270 V to -60 V	+85°C			0.3		
	V_{SW} = -310 V to GND V_{SW} = +250 V to -60 V	-40°C			0.1		
On Resistance	I_{SW} = ±10 mA, ±40 mA, T_{BAT} = -2 V	+25°C	R_{ON}	-	14.5	-	Ω
	I_{SW} = ±10 mA, ±40 mA, T_{BAT} = -2 V	+85°C		-	20.5	28	
	I_{SW} = ±10 mA, ±40 mA, T_{BAT} = -2 V	-40°C		-	10.5	-	
Switch Resistance Matching	Per On Resistance test conditions above. Magnitude R_{ON} SW1 - R_{ON} SW2		ΔR_{ON}	-	0.15	0.8	
DC Current Limit	V_{SW} (on) = ±10 V	+25°C	I_{LIM}	-	300	-	mA
	V_{SW} (on) = ±10 V	+85°C		80	160	-	
	V_{SW} (on) = ±10 V	-40°C		-	400	425	

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Dynamic Current Limit (t = <0.5 µs)	Break switches on, all other switches off, apply ±1 kV 10/1000 µs pulse to Tip/Ring interface with appropriate protection in place.	I_{SW}	-	2.5	-	A
Contacts to Input Isolation	V_{SW} (T_{LINE}, R_{LINE}) = ±320 V +25°C logic inputs = GND	I_{SW}	-	0.1	1	µA
	V_{SW} (T_{LINE}, R_{LINE}) = ±330 V +85°C logic inputs = GND			0.3		
	V_{SW} (T_{LINE}, R_{LINE}) = ±310 V, -40°C logic inputs = GND			0.1		
dv/dt sensitivity	Applied voltage = 100 V p-p square wave at 100 Hz	-	-	200	-	V/µs

1.4.3 Ringing Return Switch, SW3

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Open Contact Isolation - Off-state leakage current	V_{SW3} = T_{LINE} to $T_{RINGING}$	I_{SW}	-	0.1	1	µA
	V_{SW} = -320V to GND +25°C V_{SW} = +260 V to -60 V					
	V_{SW} = -330 V to GND +85°C V_{SW} = +270 V to -60 V			0.3		
	V_{SW} = -310 V to GND -40°C V_{SW} = +250 V to -60 V			0.1		
On Resistance	I_{SW} (on) = ±0 mA, ±10 mA +25°C	R_{ON}	-	60	-	Ω
	I_{SW} (on) = ±0 mA, ±10 mA +85°C			85	100	
	I_{SW} (on) = ±0 mA, ±10 mA -40°C			45	-	
DC Current Limit	V_{SW} (on) = ±10 V +25°C	I_{SW}	-	135	-	mA
	V_{SW} (on) = ±10 V +85°C			85		
	V_{SW} (on) = ±10 V -40°C			210		
Dynamic current limit (t = <0.5 µs)	Ringing switches on, all other switches off, apply ±1 kV 10/1000 µs pulse to Tip/Ring interface with appropriate protection in place.	I_{SW}	-	2.5	-	A
Contacts to Input Isolation	V_{SW} (T_{LINE}, $T_{RINGING}$) = ±320 V +25°C logic inputs = GND	I_{SW}	-	0.1	1	µA
	V_{SW} (T_{LINE}, $T_{RINGING}$) = ±330 V +85°C logic inputs = GND			0.3		
	V_{SW} (T_{LINE}, $T_{RINGING}$) = ±310 V -40°C logic inputs = GND			0.1		
dv/dt sensitivity	Applied voltage = 100 V p-p square wave at 100 Hz	-	-	200	-	V/µs

1.4.4 Ringing Switch, SW4

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Open Contact Isolation - Off-state leakage current	V_{SW4} = R_{LINE} to $R_{RINGING}$					
	V_{SW} = -255 V to +210 V, V_{SW} = +255 V to -210 V, +25°C	I_{SW}	-	0.05	1	µA
	V_{SW} = -270 V to +210 V, V_{SW} = +270 V to -210 V, +85°C			0.1		
	V_{SW} = -245 V to +210 V, V_{SW} = +245 V to -210 V, -40°C			0.05		
On Voltage	I_{SW} (on) = ± 1 mA	V_{SW}	-	1.5	3	V
On Resistance	I_{SW} (on) = ±70 mA, ±80 mA	R_{ON}	-	8.5	12	Ω
Ringing generator current to ground	Ringing switches on.	$I_{RINGING}$	-	0.1	0.25	mA
On steady-state current*	Ringing switches on.	-	-	-	2	A
Surge current*	Ringing switches on.	-	-	-	2	A
Release current	Remove ringing mode, SW4 on.	I_{SW}	-	300	-	µA
Contacts to Inout Isolation	V_{SW} (R_{LINE}, $R_{RINGING}$) = ±320 V, logic inputs = GND, +25°C	I_{SW}	-	0.05	1	µA
	V_{SW} (R_{LINE}, $R_{RINGING}$) = ±330 V, logic inputs = GND, +85°C			0.1		
	V_{SW} (R_{LINE}, $R_{RINGING}$) = ±310 V, logic inputs = GND, -40°C			0.05		
dv/dt sensitivity	Applied voltage = 100 V p-p square wave at 100 Hz	-	-	200	-	V/µs

** Secondary protection and ringing source current limiting must prevent exceeding these parameters.*

1.4.5 Test Switches, SW5 and SW6

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Open Contact Isolation - Off-state leakage current	V_{SW5} = T_{TEST} to T_{BAT}, V_{SW6} = R_{TEST} to R_{BAT}					
	V_{SW} = -320 V to GND, V_{SW} = +260 V to -60 V, +25°C	I_{SW}	-	0.1	1	µA
	V_{SW} = -330 V to GND, V_{SW} =+270 V to -60 V, +85°C			0.3		
	V_{SW} = -310 V to GND, V_{SW} = +250 V to -60 V, -40°C			0.1		

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
On Resistance	T_{LINE} = ±10 mA, ±40 mA, T_{BAT} = -2 V +25°C	R_{ON}	-	38	-	Ω
	T_{LINE} = ±10 mA, ±40 mA, T_{BAT} = -2 V +85°C			46	70	
	T_{LINE} = ±10 mA, ±40 mA, T_{BAT} = -2 V -40°C			28	-	
DC Current Limit	V_{SW} (on) = ±10 V +25°C	I_{SW}	-	175	-	mA
	V_{SW} (on) = ±10 V +85°C		80	110	-	
	V_{SW} (on) = ±10 V -40°C		-	210	250	
Dynamic current limit (t = <0.5 µs)	Test switches on , ringing access switches off, apply ±1 kV at 10/1000 µs pulse, with appropriate secondary protection in place.	I_{SW}	-	2.5	-	A
Contacts to Input Isolation	V_{SW} (T_{TEST}, R_{TEST}) = ±320 V +25°C logic inputs = GND	I_{SW}	-	0.1	1	µA
	V_{SW} (T_{TEST}, R_{TEST}) = ±330 V +85°C logic inputs = GND			0.3		
	V_{SW} (T_{TEST}, R_{TEST}) = ±310 V -40°C logic inputs = GND			0.1		
dv/dt sensitivity	Applied voltage = 100 V p-p square wave at 100 Hz	-	-	200	-	V/µs

1.5 Digital Input Characteristics - IN_{TEST},$IN_{RINGING}$ and LATCH Pins

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Input Threshold	Logic low	V_{IL}	-	-	1.5	V
	Logic high	V_{IH}	3.5	-	-	
Input Leakage Current	V_{DD} = 5.5 V, V_{BAT} = -75 V, V_{IH} = 5 V	I_{IH}	-	0.1	1	µA
	V_{DD} = 5.5 V, V_{BAT} = -75 V, V_{IL} = 0 V	I_{IL}	-	0.1	1	

1.6 Power Consumption Characteristics

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
V_{DD} Current Consumption	V_{DD} = 5 V, V_{BAT} = -48V, Talk or All-Off states.	I_{DD}	-	1.1	2.0	mA
	V_{DD} = 5 V, V_{BAT} = -48 V, Ringing or Test states.		-	1.3	2.0	
V_{BAT} Current Consumption	V_{DD} = 5 V, V_{BAT} = -48 V, Any state	I_{BAT}	-	0.1	10	µA
Power Consumption	V_{DD} = 5 V, V_{BAT} = -48 V, Talk or All-Off states.	P	-	5.5	10	mW
	V_{DD} = 5 V, V_{BAT} = -48 V, Ringing or Test states.			6.5	10	

1.7 Thermal Shutdown Characteristics

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Activation Temperature	T_{SD} => Low	T	110	125	150	°C
Hysteresis	T_{SD} => High	ΔT	10	-	25	°C

1.8 Protection Circuitry Electrical Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Parameters Related to the Diodes in the Diode Bridge						
Voltage drop at continuous current (50/60 Hz)	Apply ± dc current limit of break switches	V_F	-	2.1	3	V
Voltage drop at surge current	Apply ± dynamic current limit of break switches	V_F	-	5	-	
Parameters Related to the Protection SCR						
Surge current	-	-	-	-	*	A
Trigger current	+25°C	I_{TRIG}	-	60	-	mA
	+85°C			35		
Hold current	+25°C	I_{HOLD}	-	100	-	mA
	+85°C		60	70		
Gate trigger voltage	$I_{GATE} = I_{Trigger}$ **	V_{TBAT} or V_{RBAT}	V_{BAT} -4	-	V_{BAT} -2	V
Reverse leakage current	V_{BAT} = -48V	I_{VBAT}	-	-	1.0	µA
On-state voltage	0.5 A, t = 0.5 ms	V_{TBAT} or V_{RBAT}	-	-3	-	V
	2.0 A, t = 0.5 ms			-5		

*Passes GR1089 and ITU-T K.20 with appropriate protection in place.
** V_{BAT} must be capable of sourcing $I_{TRIGGER}$ for the internal SCR to activate.

1.9 Truth Table - CPC7584xA/B

State	$IN_{RINGING}$	IN_{Test}	LATCH	TSD [1]	Break Switches	Ringing Switches	Test Switches
Talk	0	0	0	1 or Floating	On	Off	Off
Ringing	1	0			Off	On	Off
Test	0	1			Off	Off	On
All Off	1	1			Off	Off	Off
Latched	X	X	1		Unchanged	Unchanged	Unchanged
All off	X	X	X	0	Off	Off	Off

[1]If TSD = 5V, thermal shutdown is disabled. If TSD is left floating, the thermal shutdown mechanism is enabled.

1.10 Truth Table - CPC7584xC

State	$IN_{RINGING}$	IN_{Test}	LATCH	TSD [1]	Break Switches	Ringing Switches	Test Switches
Talk	0	0	0	1 or Floating	On	Off	Off
Ringing	1	0			Off	On	Off
Test / Monitor	0	1			On	Off	On
All Off	1	1			Off	Off	Off
Latched	X	X	1		Unchanged	Unchanged	Unchanged
All off	X	X	X	0	Off	Off	Off

[1]If TSD = 5V, thermal shutdown is disabled. If TSD is left floating, the thermal shutdown mechanism is enabled.

2. Functional Description

2.1 Introduction

The CPC7584xA/B has four states:

- **Talk**. Line break switches SW1 and SW2 closed, ringing switches SW3 and SW4 open, and test switches SW5 and SW6 open.
- **Ringing**. Line break switches SW1 and SW2 open, ringing switches SW3 and SW4 closed, and test-in switches SW5 and SW6 open.
- **Test**. Line break switches SW1 and SW2 open, ringing switches SW3 and SW4 open, and test-in switches SW5 and SW6 closed.
- **All off**. Line break switches SW1 and SW2 open, ringing switches SW3 and SW4 open, and loop test switches SW5 and SW6 open.

The CPC7584xC replaces the Test state with the Test/Monitor state as defined below.

- **Test/Monitor**. Line break switches SW1 and SW2 closed, ringing switches SW3 and SW4 open, and test-in switches SW5 and SW6 closed.

The CPC7584 offers break-before-make and make-before-break switching with simple logic-level input control. Solid-state switch construction means no impulse noise is generated when switching during ring cadence or ring trip, eliminating the need for external zero-cross switching circuitry. State-control is via logic-level input so no additional driver circuitry is required. The line break switches SW1 and SW2 are linear switches that have exceptionally low RDS_{ON} and excellent matching characteristics. The ringing access switch SW4 has a breakdown voltage rating of greater than 480 V. This is sufficiently high, with proper protection, to prevent breakdown in the presence of a transient fault condition (i.e., passing the transient on to the ring generator).

Integrated into the CPC7584 is a diode bridge/SCR clamping circuit, current limiting, and a thermal shutdown mechanism to provide protection to the SLIC device during a fault condition. Positive and negative surges are reduced by the current limiting circuitry and steered to ground via diodes and the integrated SCR. Power-cross transients are also reduced by the current limiting and thermal shutdown circuits. Note that only the CPC7584xA and CPC7584xC parts include the integrated protection SCR.

To protect the CPC7584 from an overvoltage fault condition, use of a secondary protector is required. The secondary protector must limit the voltage seen at the tip and ring terminals to a level below the maximum breakdown voltage of the switches. To minimize the stress on the solid-state contacts, use of a foldback or crowbar type secondary protector is recommended. With proper selection of the secondary protector, a line card using the CPC7582BC will meet all relevant ITU, LSSGR, FCC and UL protection requirements.

The CPC7584 operates from a +5 V supply only. This gives the device extremely low idle and active power dissipation and allows use with virtually any range of battery voltage. A battery voltage is also used by the CPC7584 as a reference for the integrated protection circuit. In the event of a loss of battery voltage, the CPC7584 enters the all-off state.

2.2 Switch Timing

The CPC7584 provides, when switching from the ringing state to the idle/talk state, the ability to control the release timing of the ringing access switches SW3 and SW4 relative to the state of the line break switches SW1 and SW2 using simple logic-level input. This is referred to a make-before-break or break-before-make operation. When the line break switch contacts (SW1 and SW2) are closed (or made) before the ringing access switch contacts (SW3 and SW4) are opened (or broken), this is referred to make-before-break operation. Break-before-make operation occurs when the ringing access contacts (SW3 and SW4) are opened (broken) before the line break switch contacts (SW1 and SW2) are closed (made). With the CPC7584, the make-before-break and break-before-make operations can easily be selected by applying logic-level inputs to pins 9 and 10 (IN_{RING} and $IN_{TEST-IN}$) of the device.

The logic sequences for either mode of operation are given in “Make-Before-Break Operation (Ringing to Talk Transition)” on page 11 and “Break-Before-Make Operation (Ringing to Talk Transition)” on page 11. Logic states and explanations are given in “Truth Table - CPC7584xA/B” on page 9.

Break-before-make operation can also be achieved using pin 7 (TSD) as an input. In “Break-Before-Make Operation (Ringing to Talk Transition)” on page 11 lines 2 and 3, it is possible to induce the switches to the all-off state by grounding pin 7 (TSD) instead of

apply logic input to the pins. This has the effect of overriding the logic inputs and forcing the device to the all-off state. Hold this input state for 25 ms. During this hold period, toggle the inputs from the ringing state (10) to the idle/talk state (00). After the 25 ms, release pin 7 (TSD) to return the switch control to the input pins 9 and 10 and reset the device to the idle/talk state.

Setting TSD to +5 V allows switch control using the logic pins 9 and 10. This setting, however, also disables the thermal shutdown circuit and is therefore not recommended. When using logic controls via the input pins 9 and 10, pin 7 (TSD) should be allowed to float. As a result, the two recommended states when using pin 7 (TSD) as a control are 0, which forces the device to the all-off state, or float, which allows logic inputs to pins 9 and 10 to remain active. This may require the use of an open-collector buffer.

2.2.1 Make-Before-Break Operation (Ringing to Talk Transition)

State	$IN_{RINGING}$	IN_{TEST}	T_{SD}	Timing	Break Switches	Ringing Return Switch (SW3)	Ringing Switch (SW4)	Test Switches
Ringing	1	0	Floating	-	Open	Closed	Closed	Open
Make-before-break	0	0	Floating	SW4 waiting for next zero-current crossing to turn off. Maximum time is one-half of ringing. In this transition state, current that is limited to the dc break switch current limit value will be sourced from the ring node of the SLIC.	Closed	Open	Closed	Open
Talk	0	0	Floating	Zero-cross current has occurred	Closed	Open	Open	Open

2.2.2 Break-Before-Make Operation (Ringing to Talk Transition)

State	$IN_{RINGING}$	IN_{TEST}	T_{SD}	Timing	Break Switches	Ringing Return Switch (SW3)	Ringing Switch (SW4)	Test Switches
Ringing	1	0	Floating	-	Open	Closed	Closed	Open
All-off	1	1	Floating	Hold this state for at least 25 ms. SW4 waiting for zero current to turn off.	Open	Open	Closed	Open
				SW4 has opened.			Open	
Talk	0	0	Floating	Close Break Switches	Closed	Open	Open	Open

2.2.3 Alternate Break-Before-Make Operation

Break-before-make operation can also be achieved using TSD as an input. In lines 2 and 3 of "Break-Before-Make Operation (Ringing to Talk Transition)" on page 11, instead of using the logic input pins to force the all-off state, force TSD to ground. This overrides the logic inputs and also forces the all off state. Hold this state for 25 ms. During this 25 ms all-off state, toggle the inputs from the ringing state (Ring = 5 V, Test-In = 0 V) to the idle/talk state (Ring = 0 V, Test-In=0 V). After 25 ms, release TSD to return switch control to the input pins which will set the idle talk state.

When using the CPC7584 in this mode, forcing TSD to ground overrides the input pins and force an all off state. Setting TSD to +5 V allows switch control via the logic input pins. However, setting TSD to +5 V also disables the thermal shutdown mechanism. This is not recommended. Therefore, to allow switch control via the logic input pins, allow TSD to float.

When using TSD as an input, the two recommended states are 0 (overrides logic input pins and forces all off state) and float (allows switch control via logic input pins and the thermal shutdown mechanism is active). This may require use of an open-collector buffer.

2.3 Ring Access Switch Zero-Cross Current Turn Off

After the application of a logic input to turn SW4 off, the ring access switch is designed to delay the change in state until the next zero-crossing. Once on, the switch requires a zero-current cross to turn off, and therefore should not be used to switch a pure DC signal. The switch will remain in the on state no matter what logic input until the next zero crossing. For proper operation, pin 12 (R_{RING}) should be connected using proper impedance to a ring generator or other AC source. These switching characteristics will reduce and possibly eliminate overall system impulse noise normally associated with ringing access switches. The attributes of ringing access switch SW4 may make it possible to eliminate the need for a zero-cross switching scheme. A minimum impedance of 300 Ω in series with the ring generator is recommended.

2.4 Power Supplies

Both a +5 V supply and battery voltage are connected to the CPC7584. CPC7584 switch state control is powered exclusively by the +5 V supply. As a result, the CPC7584 exhibits extremely low power dissipation during both active and idle states.

The battery voltage is not used for switch control but rather as a reference for the integrated secondary protection circuitry. The integrated SCR is designed to trigger when pin 3 (T_{BAT}) or pin 14 (R_{BAT}) drops 2 to 4 V below the battery. This trigger prevents a fault induced overvoltage event at the T_{BAT} or R_{BAT} nodes.

2.5 Battery Voltage Monitor

The CPC7584 also uses the voltage reference to monitor battery voltage. If battery voltage is lost, the CPC7582BC immediately enters the all-off state. It remains in this state until the battery voltage is restored. The device also enters the all-off state if the battery voltage rises above –10 V and remains in the all-off state until the battery voltage drops below –15 V. This battery monitor feature draws a small current from the battery (less than 1 mA typical) and will add slightly to the device's overall power dissipation.

2.6 Protection

2.6.1 Diode Bridge/SCR

The CPC7584 uses a combination of current limited break switches, a diode bridge/SCR clamping circuit, and a thermal shutdown mechanism to protect the SLIC device or other associated circuitry from damage during line transient events such as lightning. During a positive transient condition, the fault current is conducted through the diode bridge to ground. Voltage is clamped to the diode drop above ground. During a negative transient of 2 to 4 V more negative than the battery, the SCR conducts and faults are shunted to ground via the SCR and diode bridge.

In order for the SCR to crowbar or foldback, the on voltage (see "Protection Circuitry Electrical Specifications" on page 8) of the SCR must be less negative than the battery reference voltage. If the battery voltage is less negative the SCR on voltage, the SCR will not crowbar, however it will conduct fault currents to ground.

For power induction or power-cross fault conditions, the positive cycle of the transient is clamped to the diode drop above ground and the fault current directed to ground. The negative cycle of the transient will cause the SCR to conduct when the voltage exceeds the battery reference voltage by two to four volts, steering the current to ground.

2.6.2 Current Limiting function

If a lightning strike transient occurs when the device in the talk/idle state, the current is passed along the line to the integrated protection circuitry and limited by the dynamic current limit response of break switches SW1 and SW2. When a 1000V 10/1000 pulse (LSSGR lightning) is applied to the line though a properly clamped external protector, the current seen at pins 2 (T_{BAT}) and pin 15 (R_{BAT}) will be a pulse with a typical magnitude of 2.5 A and a duration of less than 0.5 ms.

If a power-cross fault occurs with the device in the talk/idle state, the current is passed though break switches SW1 and SW2 on to the integrated protection circuit and is limited by the dynamic DC current limit response of the two break switches. The DC current limit, specified over temperature, is between 80 mA and 425 mA, and the circuitry has a negative temperature coefficient. As a result, if the device is subjected to extended heating due to power cross fault, the measured current at pin 2 (T_{BAT}) and pin 15 (R_{BAT}) will decrease as the device temperature increases. If the device temperature rises sufficiently, the temperature shutdown mechanism will activate and the device will default to the all-off state.

2.7 Temperature Shutdown

The thermal shutdown mechanism will activate when the device temperature reaches a minimum of 110° C, placing the device in the all-off state regardless of logic input. During thermal shutdown mode, pin 7 (TSD) will read 0 V. Normal output of TSD is $+V_{DD}$.

If presented with a short duration transient such as a lightning event, the thermal shutdown feature will typically not activate. But in an extended power-cross transient, the device temperature will rise and the thermal shutdown will activate forcing the switches to the all-off state. At this point the current measured at pin 3 (T_{BAT}) and pin 14 (R_{BAT}) will drop to zero. Once the device enters thermal shutdown it will remain in the all-off state until the temperature of the device drops below the activation level of the thermal shutdown circuit. This will return the device to the state prior to thermal shutdown. If the transient has not passed, current will flow at the value allowed by the dynamic DC current limiting of the switches and heating will begin again, reactivating the thermal shutdown mechanism. This cycle of entering and exiting the thermal shutdown mode will continue as long as the fault condition persists. If the magnitude of the fault condition is great enough, the external secondary protector could activate and shunt all current to ground.

The thermal shutdown mechanism of the CPC7584 can be disable by applying $+V_{DD}$ to pin 7 (TSD).

2.8 External Protection Elements

The CPC7584 requires only one overvoltage secondary protector on the loop side of the device. The integrated protection feature described above negates the need for protection on the line side. The secondary protector limits voltage transients to levels that do not exceed the breakdown voltage or input-output isolation barrier of the CPC7584. A foldback or crowbar type protector is recommended to minimize stresses on the device.

Consult Clare's application note, AN-100, "Designing Surge and Power Fault Protection Circuits for Solid State Subscriber Line Interfaces" for equations related to the specifications of external secondary protectors, fused resistors and PTCs.

2.9 Data Latch

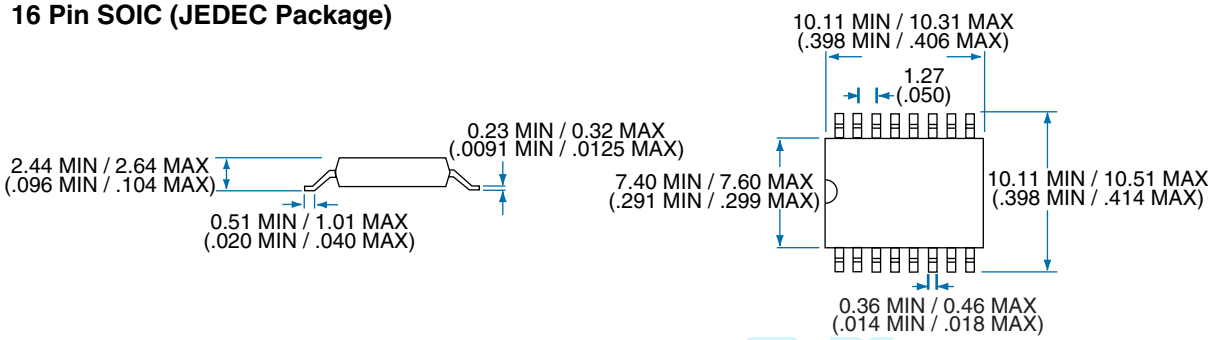
The CPC7584 has an integrated data latch. The latch operation is controlled by logic-level input pin 11 (LATCH). The data input of the latch is pin 10 (IN_{RING}) and pin 9 ($IN_{TEST-IN}$) of the device while the output of the data latch is an internal node used for state control. When LATCH control pin is at logic 0, the data latch is transparent and data control signals flow directly through to state control. A change in input will be reflected in a change is switch state. When LATCH control pin is at logic 1, the data latch is active and a change in input control will not affect switch state. The switches will remain in the position they were in when the LATCH changed from logic 0 to logic 1 and will not respond to changes in input as long as the latch is at logic 1. The TSD input is not tied to the data latch. Therefore, TSD is not affected by the LATCH input and the TSD input will override state control via pin 10 (IN_{RING}) and pin 9 ($IN_{TEST-IN}$) and the LATCH.

3. Manufacturing Information

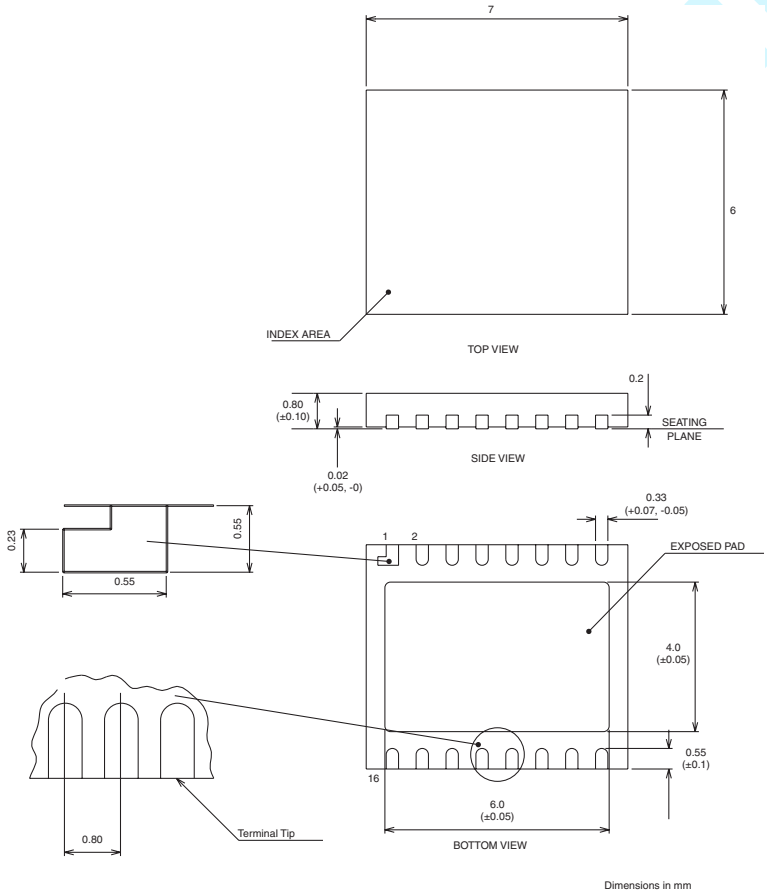
3.1 Mechanical Dimensions

3.1.1 SOIC

16 Pin SOIC (JEDEC Package)



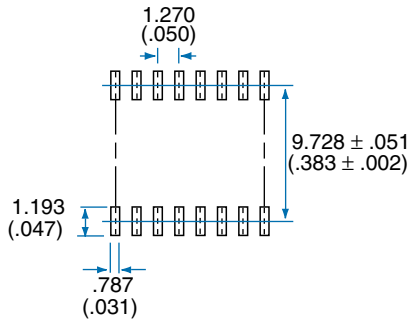
3.1.2 MLP



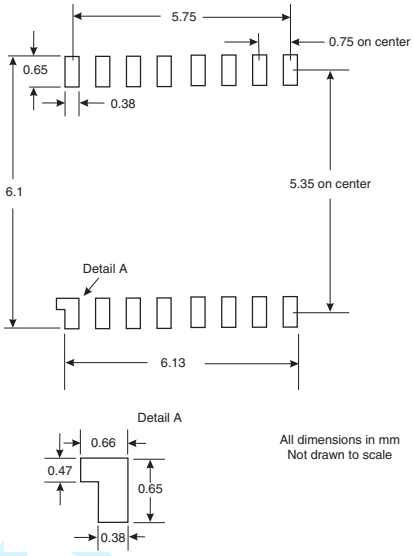
3.2 Printed-Circuit Board Layout

3.2.1 SOIC

PC Board Pattern (Top View)

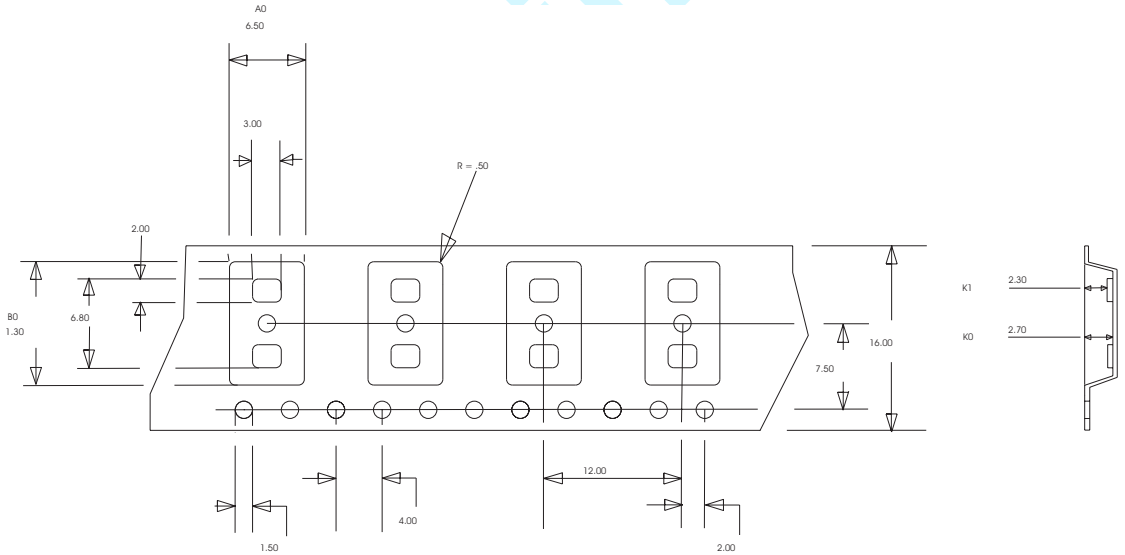


3.2.2 MLP



3.3 Tape and Reel Packaging

3.3.1 SOIC



NOTES: 1. ALL DIMENSIONS ARE IN MILLIMETERS AND CARRY TOLERANCES OF EIA STANDARD 481-2. 2. THE TAPE COMPLIES WITH ALL "NOTES" FOR CONSTANT DIMENSIONS LISTED ON PAGE 5 OF EIA-481-2.

A0 =	6.5 mm
B0 =	10.3 mm
K0 =	2.3 mm
K1 =	2.7 mm

3.4 Soldering

3.4.1 Moisture Reflow Sensitivity

Clare has characterized the moisture reflow sensitivity of LCAS products using IPC/JEDEC standard J-STD-020A. Moisture uptake from atmospheric humidity occurs by diffusion. During the solder reflow process, in which the component is attached to the PCB, the whole body of the component is exposed to high process temperatures. The combination of moisture uptake and high reflow soldering

temperatures may lead to moisture induced delamination and cracking of the component. To prevent this, this component must be handled in accordance with IPC/JEDEC standard J-STD-020A per the labeled moisture sensitivity level (MSL), level 1 for the SOIC package, and level 2 for the MLP package.

3.4.2 Reflow Profile

The maximum ramp rates, dwell times, and temperatures of the assembly reflow profile should not exceed those specified in IPC/JEDEC standard J-STD-020A, which were used to determine the moisture sensitivity level of this component.

3.5 Washing

Clare does not recommend ultrasonic cleaning of LCAS parts.

Specifications: DS-CPC7584 - R0B

1/23/2004

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