LM77 9-Bit + Sign Digital Temperature Sensor and Thermal Window Comparator with Two-Wire Interface

Check for Samples: LM77

FEATURES

- **Window Comparison Simplifies Design of ACPI Compatible Temperature Monitoring and Control.**
- **Serial Bus Interface**
- **Separate Open-Drain Outputs for Interrupt and Critical Temperature Shutdown**
- **Shutdown Mode to Minimize Power Consumption**
- **Up to 4 LM77s Can be Connected to a Single Bus**
- **9-bit + Sign Output; Full-Scale Reading of Over 128°C**
- **SOIC and VSSOP 8-lead Packages**

APPLICATIONS

- **System Thermal Management**
- **Personal Computers**
- **Office Electronics**
- **Electronic Test Equipment**
- **Automotive**
- **HVAC**

KEY SPECIFICATIONS

- **Supply Voltage 3.0V to 5.5V**
- **Supply Current**
  - **Operating**
    - **250 µA (typ)**
    - **500 µA (max)**
  - **Shutdown**
    - **5 µA (typ)**
- **Temperature Accuracy**
  - **−10°C to 65°C, ±1.5°C(max)**
  - **−25°C to 100°C, ±2°C(max)**
  - **−55°C to 125°C, ±3°C(max)**

DESCRIPTION

The LM77 is a digital temperature sensor and thermal window comparator with an I^2C Serial Bus interface. The window-comparator architecture of the LM77 eases the design of temperature control systems conforming to the ACPI (Advanced Configuration and Power Interface) specification for personal computers. The open-drain Interrupt (INT) output becomes active whenever temperature goes outside a programmable window, while a separate Critical Temperature Alarm (T_CRIT_A) output becomes active when the temperature exceeds a programmable critical limit. The INT output can operate in either a comparator or event mode, while the T_CRIT_A output operates in comparator mode only.

The host can program both the upper and lower limits of the window as well as the critical temperature limit. Programmable hysterisis as well as a fault queue are available to minimize false tripping. Two pins (A0, A1) are available for address selection. The sensor powers up with default thresholds of 2°C T_{HYST}, 10°C T_{LOW}, 64°C T_{HIGH}, and 80°C T_CRIT.

The LM77's 3.0V to 5.5V supply voltage range, Serial Bus interface, 9-bit + sign output, and full-scale range of over 128°C make it ideal for a wide range of applications. These include thermal management and protection applications in personal computers, electronic test equipment, office electronics, automotive, and HVAC applications.

Simplified Block Diagram

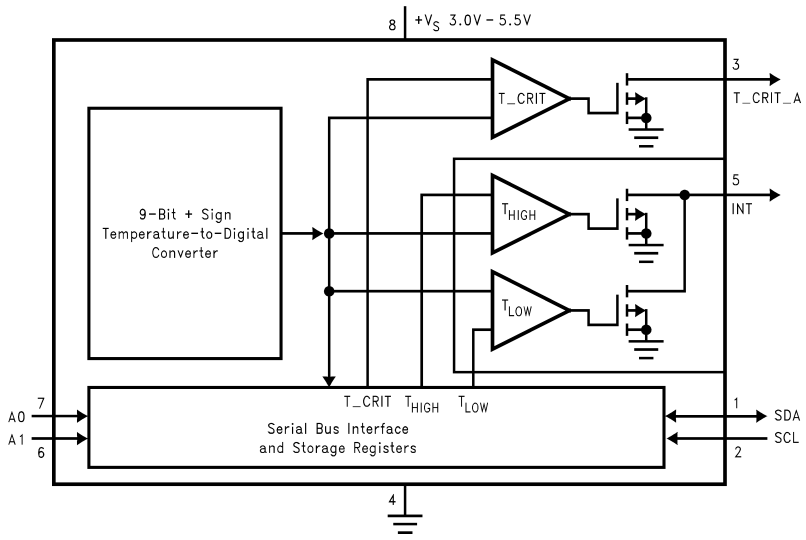


Figure 1.

Connection Diagram

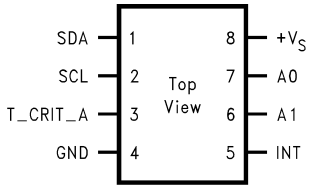


Figure 2. SOIC-8 or VSSOP Package
See Package Number D0008A or DGK0008A

PIN DESCRIPTIONS

Pin Name	Pin No.	Description	Typical Connection
SDA	1	Serial Bi-Directional Data Line. Open Drain Output	From Controller
SCL	2	Serial Bus Clock Input	From Controller
T_CRIT_A	3	Critical Temperature Alarm Open Drain Output	Pull Up Resistor, Controller Interrupt Line or System Hardware Shutdown
GND	4	Power Supply Ground	Ground
INT	5	Interrupt Open Drain Output	Pull Up Resistor, Controller Interrupt Line
$+V_S$	8	Positive Supply Voltage Input	DC Voltage from 3V to 5.5V
A0–A1	7,6	User-Set Address Inputs	Ground (Low, “0”) or $+V_S$ (High, “1”)

Typical Application

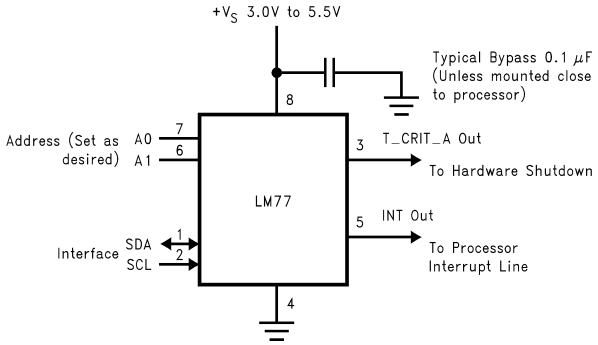


Figure 3. Typical Application

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage	−0.3V to 6.5V
Voltage at any Pin	−0.3V to (+V_S + 0.3V)
Input Current at any Pin	5 mA
Package Input Current(2)	20 mA
T_CRIT_A and INT Output Sink Current	10 mA
T_CRIT_A and INT Output Voltage	6.5V
Storage Temperature	−65°C to +125°C
Soldering Information, Lead Temperature	
ESD Susceptibility(3)	
Human Body Model	2500V
Machine Model	250V
For soldering specifications: http://www.ti.com/lit/SNOA549(4)	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) When the input voltage (V_I) at any pin exceeds the power supplies (V_I < GND or V_I > +V_S) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.
(3) Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin.
(4) Reflow temperature profiles are different for lead-free and non-lead-free packages.

Operating Ratings(1)(2)

Specified Temperature Range	T_{MIN} to T_{MAX}
See(3)	−55°C to +125°C
Supply Voltage Range (+V_S)(4)	+3.0V to +5.5V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) LM77 θ_{JA} (thermal resistance, junction-to-ambient) when attached to a printed circuit board with 2 oz. foil is: 200°C/W for the SOIC-8 (D0008A) package, 250°C/W for the VSSOP-8 (DGK0008A) package.
(3) While the LM77 has a full-scale-range in excess of 128°C, prolonged operation at temperatures above 125°C is not recommended.
(4) Both part numbers of the LM77 will operate properly over the +V_S supply voltage range of 3V to 5.5V . The devices are tested and specified for rated accuracy at their nominal supply voltage. Accuracy will typically degrade 1°C/V of variation in +V_S as it varies from the nominal value.

Temperature-to-Digital Converter Characteristics

Unless otherwise noted, these specifications apply for $+V_S$=+5 Vdc ±10% for LM77CIM-5, LM77CIMM-5 and $+V_S$=+3.3 Vdc ±10% for LM77CIM-3, LM77CIMM-3(1). **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$=+25°C, unless otherwise noted.

Parameter	Test Conditions	Typical(2)	Limits(3)	Units (Limit)
Accuracy	T_A = −10°C to +65°C		**±1.5**	°C (max)
	T_A = −25°C to +100°C		**±2.0**	
	T_A = −55°C to +125°C		**±3.0**	
Resolution	See(4)	10 0.5		Bits °C
Temperature Conversion Time	See(5)	70	**125**	ms
Quiescent Current	I^2C Inactive	0.25		mA
	I^2C Active	0.25	**0.5**	mA (max)
	Shutdown Mode	5	**10**	µA
T_{HYST} Default Temperature	See(6)(7)	2		°C
T_{LOW} Default Temperature	See(7)	10		°C
T_{HIGH} Default Temperature	See(7)	64		°C
T_C Default Temperature	See(7)	80		°C

(1) Both part numbers of the LM77 will operate properly over the $+V_S$ supply voltage range of 3V to 5.5V . The devices are tested and specified for rated accuracy at their nominal supply voltage. Accuracy will typically degrade 1°C/V of variation in $+V_S$ as it varies from the nominal value.
(2) Typicals are at T_A = 25°C and represent most likely parametric norm.
(3) Limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).
(4) 9 bits + sign, two's complement
(5) This specification is provided only to indicate how often temperature data is updated. The LM77 can be read at any time without regard to conversion state (and will yield last conversion result). If a conversion is in process it will be interrupted and restarted after the end of the read.
(6) Hysteresis value adds to the T_{LOW} setpoint value (e.g.: if T_{LOW} setpoint = 10°C, and hysteresis = 2°C, then actual hysteresis point is 10+2 = 12°C); and subtracts from the T_{HIGH} and T_CRIT setpoints (e.g.: if T_{HIGH} setpoint = 64°C, and hysteresis = 2°C, then actual hysteresis point is 64−2 = 62°C). For a detailed discussion of the function of hysteresis refer to *Section 1.1*, TEMPERATURE COMPARISON, and Figure 7.
(7) Default values set at power up.

Logic Electrical Characteristics Digital DC Characteristics

Unless otherwise noted, these specifications apply for $+V_S$=+5 Vdc ±10% for LM77CIM-5, LM77CIMM-5 and $+V_S$=+3.3 Vdc ±10% for LM77CIM-3, LM77CIMM-3. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$=+25°C, unless otherwise noted.

Parameter		Test Conditions	Typical(1)	Limits(2)	Units (Limit)
$V_{IN(1)}$	SDA and SCL Logical “1” Input Voltage			**+V_S × 0.7**	V (min)
				+V_S+0.3	V (max)
$V_{IN(0)}$	SDA and SCL Logical “0” Input Voltage			**−0.3**	V (min)
				+V_S × 0.3	V (max)
$V_{IN(1)}$	A0 and A1 Logical “1” Input Voltage			**2.0**	V (min)
				+V_S+0.3	V (max)
$V_{IN(0)}$	A0 and A1 Logical “0” Input Voltage			**−0.3**	V (min)
				0.8	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = + V_S	0.005	**1.0**	µA (max)
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V	−0.005	**−1.0**	µA (max)
C_{IN}	Capacitance of All Digital Inputs		20		pF
I_{OH}	Logic “1” Output Leakage Current	V_{OH} = + V_S		**10**	µA (max)

(1) Typicals are at T_A = 25°C and represent most likely parametric norm.
(2) Limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).

Logic Electrical Characteristics Digital DC Characteristics (continued)

Unless otherwise noted, these specifications apply for $+V_S$=+5 Vdc ±10% for LM77CIM-5, LM77CIMM-5 and $+V_S$=+3.3 Vdc ±10% for LM77CIM-3, LM77CIMM-3. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$=+25°C, unless otherwise noted.

Parameter		Test Conditions	Typical(1)	Limits(2)	Units (Limit)
V_{OL}	Low Level Output Voltage	I_{OL} = 3 mA		**0.4**	V (max)
	T_CRIT_A Output Saturation Voltage	I_{OUT} = 4.0 mA(3)		**0.8**	V (max)
	T_CRIT_A Delay			**1**	Conversions (max)
t_{OF}	Output Fall Time	C_L = 400 pF		**250**	ns (max)
		I_O = 3 mA			

(3) For best accuracy, minimize output loading. Higher sink currents can affect sensor accuracy with internal heating. This can cause an error of 0.64°C at full rated sink current and saturation voltage based on junction-to-ambient thermal resistance.

Logic Electrical Characteristics Serial Bus Digital Switching Characteristics

Unless otherwise noted, these specifications apply for $+V_S$=+5 Vdc ±10% for LM77CIM-5 and LM77CIMM-5, $+V_S$=+3.3 Vdc ±10% for LM77CIM-3 and LM77CIMM-3, CL (load capacitance) on output lines = 80 pF unless otherwise specified. Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = +25°C, unless otherwise noted.

Parameter		Test Conditions	Typical(1)	Limits(2)(3)	Units (Limit)
t_1	SCL (Clock) Period			**2.5**	µs(min)
t_2	Data in Set-Up Time to SCL High			**100**	ns(min)
t_3	Data Out Stable after SCL Low			**0**	ns(min)
t_4	SDA Low Set-Up Time to SCL Low (Start Condition)			**100**	ns(min)
t_5	SDA High Hold Time after SCL High (Stop Condition)			**100**	ns(min)

(1) Typicals are at T_A = 25°C and represent most likely parametric norm.
(2) Limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).
(3) Timing specifications are tested at the bus input logic levels (Vin(0)=0.3xVA for a falling edge and Vin(1)=0.7xVA for a rising edge) when the SCL and SDA edge rates are similar.

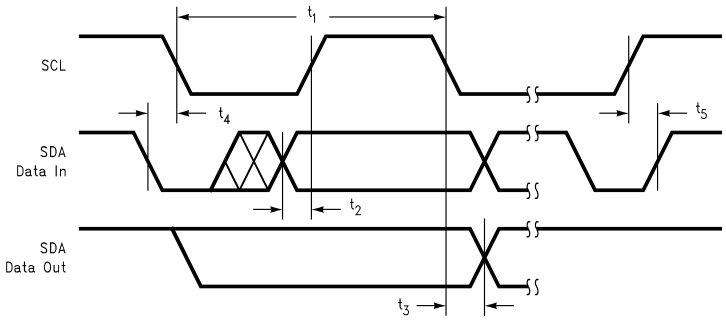


Figure 4.

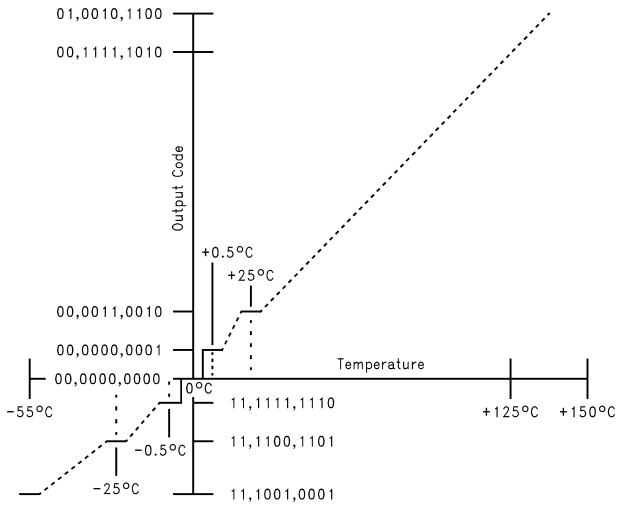


Figure 5. Temperature-to-Digital Transfer Function (Non-linear scale for clarity)

FUNCTIONAL DESCRIPTION

The LM77 temperature sensor incorporates a band-gap type temperature sensor, 10-bit ADC, and a digital comparator with user-programmable upper and lower limit values. The comparator activates either the INT line for temperatures outside the T_{LOW} and T_{HIGH} window, or the T_CRIT_A line for temperatures which exceed T_CRIT. The lines are programmable for mode and polarity.

TEMPERATURE COMPARISON

LM77 provides a window comparison against a lower (T_{LOW}) and upper (T_{HIGH}) trip point. A second upper trip point (T_CRIT) functions as a critical alarm shutdown. Figure 7 depicts the comparison function as well as the modes of operation.

Status Bits

The internal Status bits operate as follows:

"**True**": Temperature above a T_{HIGH} or T_CRIT is "true" for those respective bits. A "true" for T_{LOW} is temperature below T_{LOW}.

"**False**": Assuming temperature has previously crossed above T_{HIGH} or T_CRIT, then the temperature must drop below the points corresponding T_{HYST}(T_{HIGH} − T_{HYST} or T_CRIT − T_{HYST}) in order for the condition to be false. For T_{LOW}, assuming temperature has previously crossed below T_{LOW}, a "false" occurs when temperature goes above T_{LOW} + T_{HYST}.

The Status bits are not affected by reads or any other actions, and always represent the state of temperature vs. setpoints.

Hardwire Outputs

The T_CRIT_A hardwire output mirrors the T_CRIT_A flag unless the part is read. When the flag is true, the T_CRIT_A output is asserted regardless of Interrupt Mode. Reading the LM77 resets the T_CRIT_A output until the internal conversion is completed. In a typical system, T_CRIT_A is used to immediately shutdown or reset the system. Thus, once T_CRIT_A asserts the system normally would not be reading the LM77 via the I2C bus.

The behavior of the INT hardwire output is as follows:

Comparator Interrupt Mode (Default): User reading part resets output until next measurement completes. If condition is still true, output is set again at end of next conversion cycle. For example, if a user never reads the part, and temperature goes below T_{LOW} then INT becomes active. It would stay that way until temperature goes above T_{LOW} + T_{HYST}. However if the user reads the part, the output would be reset. At the end of the next conversion cycle, if the condition is true, it is set again. If not, it remains reset.

Event Interrupt Mode: User reading part resets output until next condition "event" occurs (in other words, output is only set once for a true condition, if reset by a read, it remains reset until the next triggering threshold has been crossed). Conversely, if a user never read the part, the output would stay set indefinitely after the first event that set the output. An "event" for Event Interrupt Mode is defined as:

1. Transitioning upward (downward) across a setpoint, or
2. Transitioning downward (upward) across a setpoint's corresponding hysteresis (after having exceeded that setpoint).

For example, if a user never read the part, and temperature went below T_{LOW} then INT would become active. It would stay that way forever if a user never read the part.

However if the user read the part, the output would be reset. Even if the condition is true, it will remain reset. The temperature must cross above T_{LOW} + T_{HYST} to set the output again.

In either mode, reading any register in the LM77 restarts the conversion. This allows a designer to know exactly when the LM77 begins a comparison. This prevents unnecessary Interrupts just after reprogramming setpoints. Typically, system Interrupt inputs are masked prior to reprogramming trip points. By doing a read just after resetting trip points, but prior to unmasking, unexpected Interrupts are prevented.

Avoid programming setpoints so close that their hysteresis values overlap. An example would be that with a T_{HYST} value of 2°C then setting T_{HIGH} and T_{LOW} to within 4°C of each other will violate this restriction. To be more specific, with T_{HYST} set to 2°C assume T_{HIGH} set to 64°C. If T_{LOW} is set equal to, or higher than 60°C this restriction is violated.

DEFAULT SETTINGS

The LM77 always powers up in a known state. LM77 power up default conditions are:

1. Comparator Interrupt Mode
2. T_{LOW} set to 10°C
3. T_{HIGH} set to 64°C
4. T_CRIT set to 80°C
5. T_{HYST} set to 2°C
6. INT and T_CRIT_A active low
7. Pointer set to “00”; Temperature Register

The LM77 registers will always reset to these default values when the power supply voltage is brought up from zero volts as the supply crosses the voltage level plotted in the following curve. The LM77 registers will reset again when the power supply drops below the voltage plotted in this curve.

Average Power on Reset Voltage vs Temperature

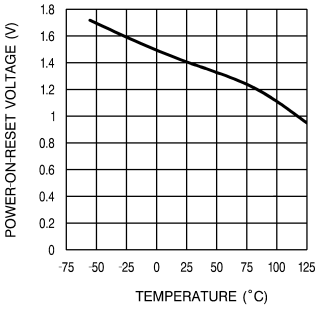


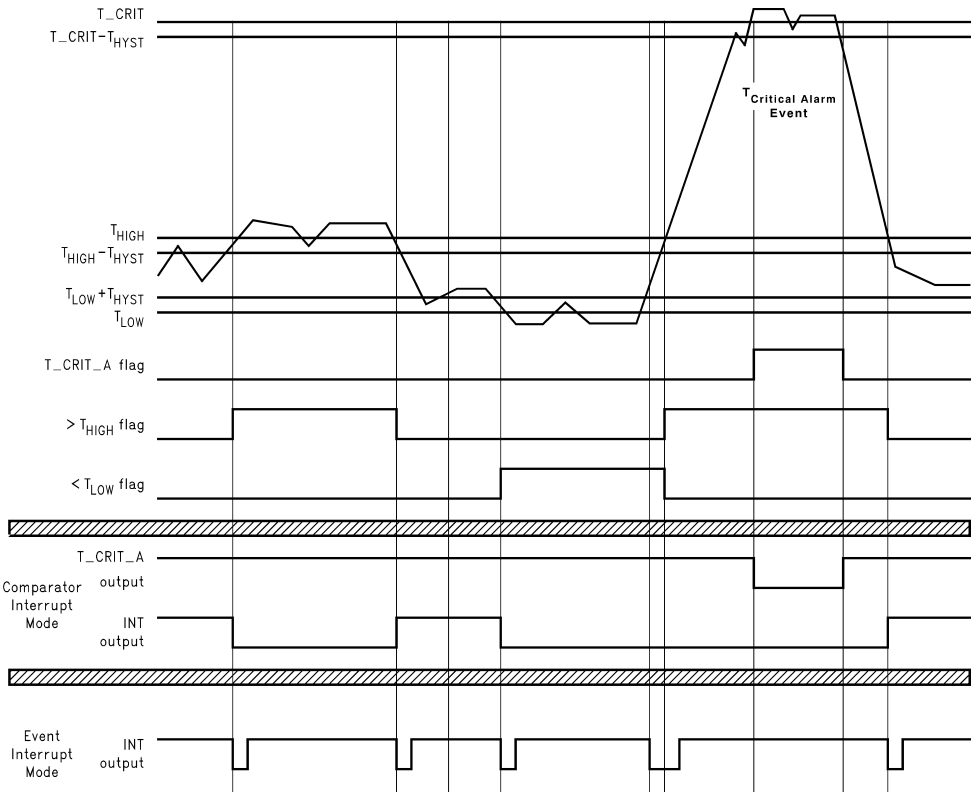
Figure 6.

SERIAL BUS INTERFACE

The LM77 operates as a slave on the Serial Bus, so the SCL line is an input (no clock is generated by the LM77) and the SDA line is a bi-directional serial data line. According to Serial Bus specifications, the LM77 has a 7-bit slave address. The five most significant bits of the slave address are hard wired inside the LM77 and are “10010”. The two least significant bits of the address are assigned to pins A1–A0, and are set by connecting these pins to ground for a low, (0); or to $+V_S$ for a high, (1).

Therefore, the complete slave address is:

1	0	0	1	0	A1	A0
MSB						LSB



Note: Event Interrupt mode is drawn as if the user is reading the part. If the user doesn't read, the outputs would go low and stay that way until the LM77 is read.

Figure 7. Temperature Response Diagram

TEMPERATURE DATA FORMAT

Temperature data can be read from the Temperature and Set Point registers; and written to the Set Point registers. Temperature data can be read at any time, although reading faster than the conversion time of the LM77 will prevent data from being updated. Temperature data is represented by a 10-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.5°C:

Temperature	Digital Output	
	Binary	Hex
+130°C	01 0000 0100	104h
+125°C	00 1111 1010	0FAh
+25°C	00 0011 0010	032h
+0.5°C	00 0000 0001	001h
0°C	00 0000 0000	000h
−0.5°C	11 1111 1111	3FFh
−25°C	11 1100 1110	3CEh
−55°C	11 1001 0010	392h

SHUTDOWN MODE

Shutdown mode is enabled by setting the shutdown bit in the Configuration register via the Serial Bus. Shutdown mode reduces power supply current to 5 µA typical. T_CRIT_A is reset if previously set. Since conversions are stoped during shutdown, T_CRIT_A and INT will not be operational. The Serial Bus interface remains active. Activity on the clock and data lines of the Serial Bus may slightly increase shutdown mode quiescent current. Registers can be read from and written to in shutdown mode. The LM77 takes miliseconds to respond to the shutdown command.

INT AND T_CRIT_A OUTPUT

The INT and T_CRIT_A outputs are open-drain outputs and do not have internal pull-ups. A "high" level will not be observed on these pins until pull-up current is provided from some external source, typically a pull-up resistor. Choice of resistor value depends on many system factors but, in general, the pull-up resistor should be as large as possible. This will minimize any errors due to internal heating of the LM77. The maximum allowable resistance of the pull up resistor is 90K Ohms based on the Logic “1” Output Leakage Current and a 2 volt high output level.

FAULT QUEUE

A fault queue of up to 4 faults is provided to prevent false tripping when the LM77 is used in noisy environments. The 4 faults must occur consecutively to set flags as well as INT and T_CRIT_A outputs. The fault queue is enabled by setting bit 4 of the Configuration Register high (see Table 3).

INTERNAL REGISTER STRUCTURE

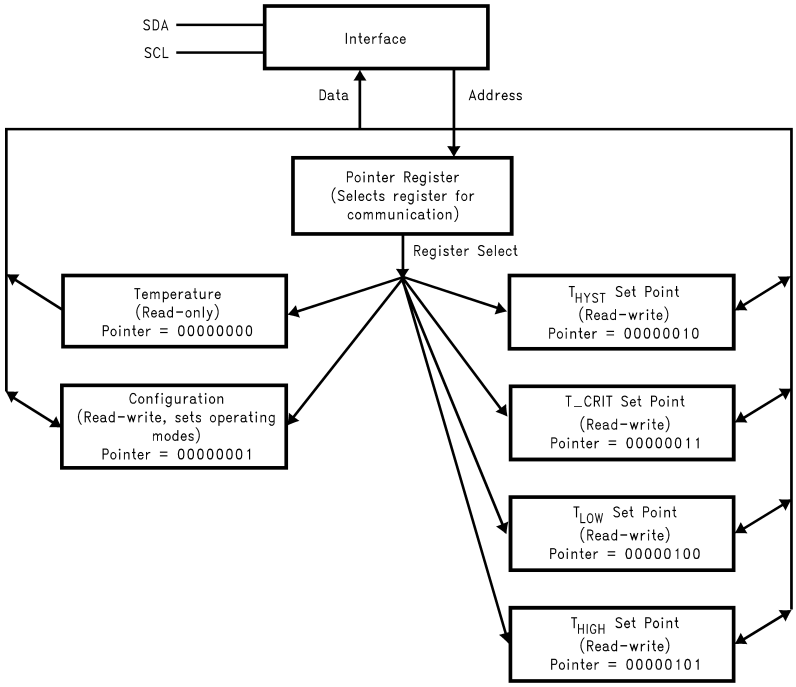


Figure 8.

The data registers in the LM77 are selected by the Pointer register. At power-up the Pointer is set to “00”; the location for the Temperature Register. The Pointer register latches the last location it was set to. In Comparator Interrupt Mode, a read from the LM77 resets the INT output. Placing the device in Shutdown mode resets the INT and T_CRIT_A outputs. All registers are read and write, except the Temperature register which is read only.

A write to the LM77 will always include the address byte and the Pointer byte. A write to the Configuration register requires one data byte, while the T_{LOW}, T_{HIGH}, and T_CRIT registers require two data bytes.

Reading the LM77 can take place either of two ways: If the location latched in the Pointer is correct (most of the time it is expected that the Pointer will point to the Temperature register because it will be the data most frequently read from the LM77), then the read can simply consist of an address byte, followed by retrieving the corresponding number of data bytes. If the Pointer needs to be set, then an address byte, pointer byte, repeat start, and another address byte plus required number of data bytes will accomplish a read.

The first data byte is the most significant byte with most significant bit first, permitting only as much data as necessary to be read to determine the temperature condition. For instance, if the first four bits of the temperature data indicates a critical condition, the host processor could immediately take action to remedy the excessive temperature. At the end of a read, the LM77 can accept either Acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).

An inadvertent 8-bit read from a 16-bit register, with the D7 bit low, can cause the LM77 to stop in a state where the SDA line is held low as shown in Figure 9. This can prevent any further bus communication until at least 9 additional clock cycles have occurred. Alternatively, the master can issue clock cycles until SDA goes high, at which time issuing a “Stop” condition will reset the LM77.

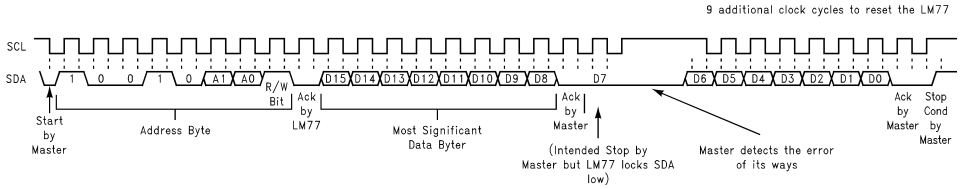


Figure 9. Inadvertent 8-Bit Read from 16-Bit Register where D7 is Zero (“0”)

(Selects which registers will be read from or written to):

Table 1. POINTER REGISTER

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	Register Select		

P0–P2: Register Select:

P2	P1	P0	Register
0	0	0	Temperature (Read only) (Power-up default)
0	0	1	Configuration (Read/Write)
0	1	0	T_{HYST} (Read/Write)
0	1	1	T_CRIT (Read/Write)
1	0	0	T_{LOW} (Read/Write)
1	0	1	T_{HIGH} (Read/Write)

P3–P7: Must be kept zero.

Table 2. TEMPERATURE REGISTER (Read Only):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Sign	Sign	Sign	Sign	MSB	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CRIT	HIGH	LOW
													Status Bits		

D0–D2: Status Bits

D3–D15: Temperature Data. One LSB = 0.5°C. Two's complement format.

Table 3. CONFIGURATION REGISTER (Read/Write):

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	Fault Queue	INT Polarity	T_CRIT_A Polarity	INT Mode	Shutdown

D0: Shutdown - When set to 1 the LM77 goes to low power shutdown mode. Power up default of “0”.

D1: Interrupt mode - 0 is Comparator Interrupt mode, 1 is Event Interrupt mode. Power up default of “0”.

D2, D3: T_CRIT_A and INT Polarity - 0 is active low, 1 is active high. Outputs are open-drain. Power up default of “0”

D4: Fault Queue - When set to 1 the Fault Queue is enabled, see FAULT QUEUE. Power up default of “0”.

D5–D7: These bits are used for production testing and must be kept zero for normal operation.

Table 4. T_{HYST}, T_{LOW}, T_{HIGH} AND T_CRIT_A REGISTERS (Read/Write):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Sign	Sign	Sign	Sign	MSB	Bit7	Bit6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	X	X	X

D0–D2: Undefined

D3–D15: T_{HYST}, T_{LOW}, T_{HIGH} or T_CRIT Trip Temperature Data. Power up default is T_{LOW} = 10°C, T_{HIGH} = 64°C, T_CRIT = 80°C, T_{HYST} = 2°C.

T_{HYST} is subtracted from T_{HIGH}, and T_CRIT, and added to T_{LOW}.

Avoid programming setpoints so close that their hysteresis values overlap. See TEMPERATURE COMPARISON.

TEST CIRCUIT DIAGRAMS

I^2C Timing Diagrams

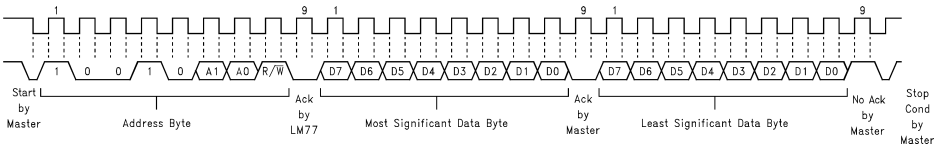


Figure 10. Typical 2-Byte Read From Preset Pointer Location Such as Temp or Comparison Registers

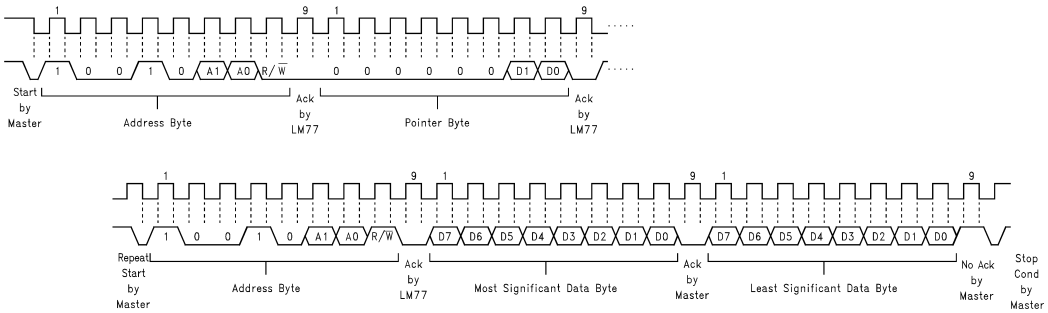


Figure 11. Typical Pointer Set Followed by Immediate Read for 2-Byte Register such as Temp or Comparison Registers

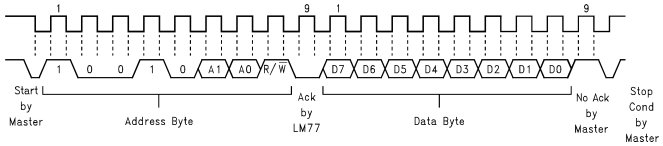


Figure 12. Typical 1-Byte Read from Configuration Register with Preset Pointer

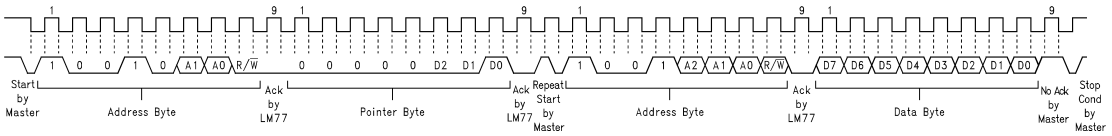


Figure 13. Typical Pointer Set Followed by Immediate Read from Configuration Register

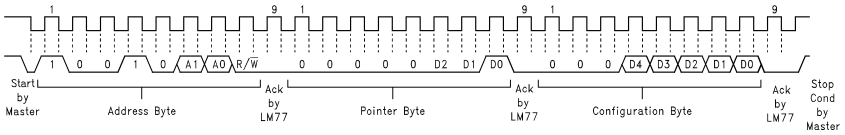
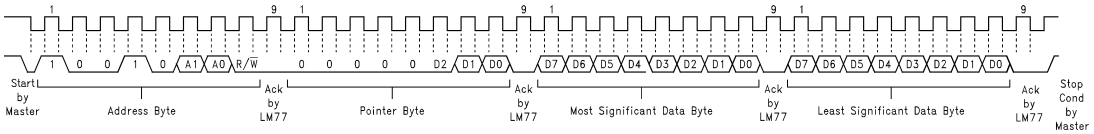


Figure 14. Configuration Register Write



Comparison Register Write

Figure 15. Timing Diagrams

Application Hints

The temperature response graph in Figure 16 depicts a typical application designed to meet ACPI requirements. In this type of application, the temperature scale is given an arbitrary value of "granularity", or the window within which temperature notification events should occur. The LM77 can be programmed to the window size chosen by the designer, and will issue interrupts to the processor whenever the window limits have been crossed. The internal flags permit quick determination of whether the temperature is rising or falling.

The T_CRIT limit would typically use its separate output to activate hardware shutdown circuitry separate from the processor. This is done because it is expected that if temperature has gotten this high that the processor may not be responding. The separate circuitry can then shut down the system, usually by shutting down the power supply.

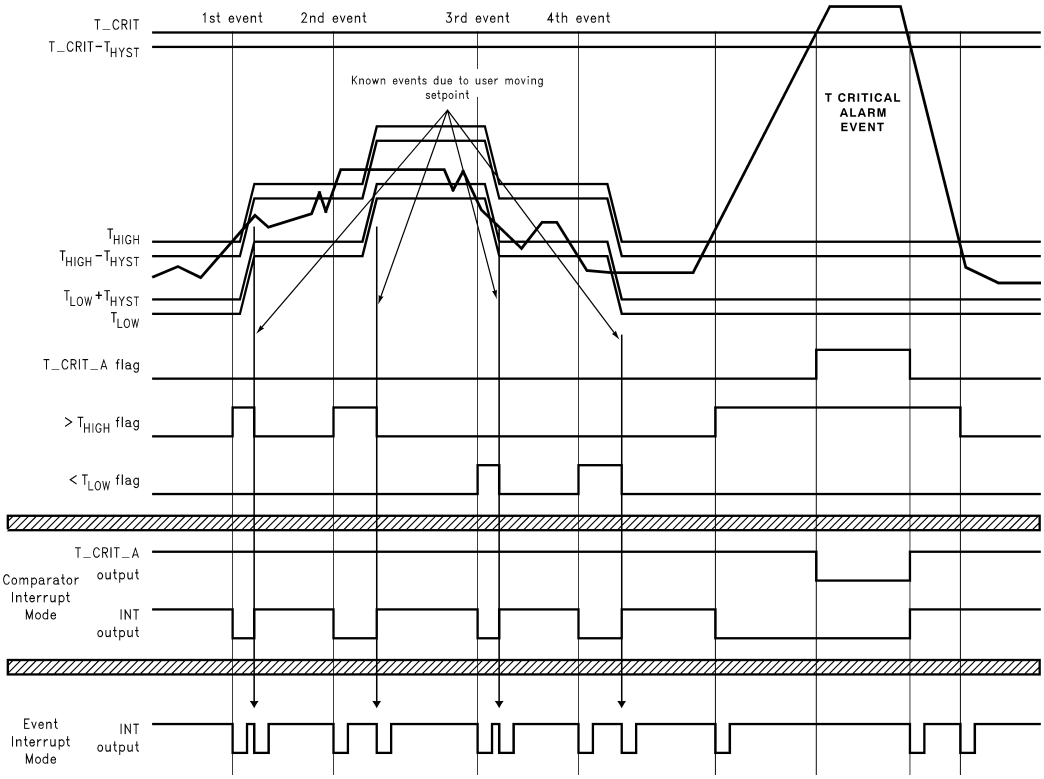
Note that the INT and T_CRIT_A outputs are separate, but can be wire-or'd together. Alternatively the T_CRIT_A can be diode or'd to the INT line in such a way that a T_CRIT_A event activates the INT line, but an INT event does not activate the T_CRIT_A line. This may be useful in the event that it is desirable to notify both the processor and separate T_CRIT_A shutdown circuitry of a critical temperature alarm at the same time (maybe the processor is still working and can coordinate a graceful shutdown with the separate shutdown circuit).

To implement ACPI compatible sensing it is necessary to sense whenever the temperature goes outside the window, issue an interrupt, service the interrupt, and reprogram the window according to the desired granularity of the temperature scale. The reprogrammed window will now have the current temperature inside it, ready to issue an interrupt whenever the temperature deviates from the current window.

To understand this graph, assume that at the left hand side the system is at some nominal temperature. For the 1st event temperature rises above the upper window limit, T_{HIGH}, causing INT to go active. The system responds to the interrupt by querying the LM77's status bits and determines that T_{HIGH} was exceeded, indicating that temperature is rising. The system then reprograms the temperature limits to a value higher by an amount equal to the desired granularity. Note that in Event Interrupt Mode, reprogramming the limits has caused a second, known, interrupt to be issued since temperature has been returned within the window. In Comparator Interrupt Mode, the LM77 simply stops issuing interrupts.

The 2nd event is another identical rise in temperature. The 3rd event is typical of a drop in temperature. This is one of the conditions that demonstrates the power of the LM77, as the user receives notification that a lower limit is exceeded in such a way that temperature is dropping.

The Critical Alarm Event activates the separate T_CRIT_A output. Typically, this would feed circuitry separate from the processor on the assumption that if the system reached this temperature, the processor might not be responding.



Note: Event Interrupt mode is drawn as if the user is reading the part. If the user doesn't read, the outputs would go low and stay that way until the LM77 is read.

Figure 16. Temperature Response Diagram for ACPI Implementation

Typical Applications

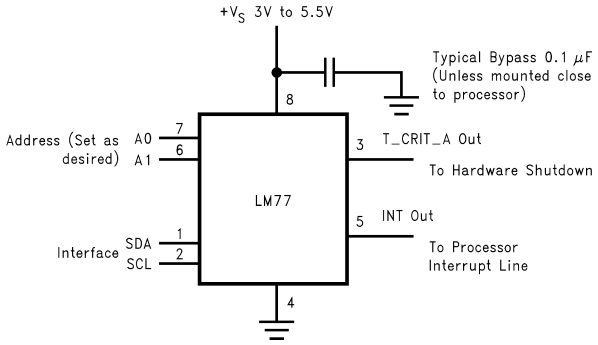


Figure 17. Typical Application

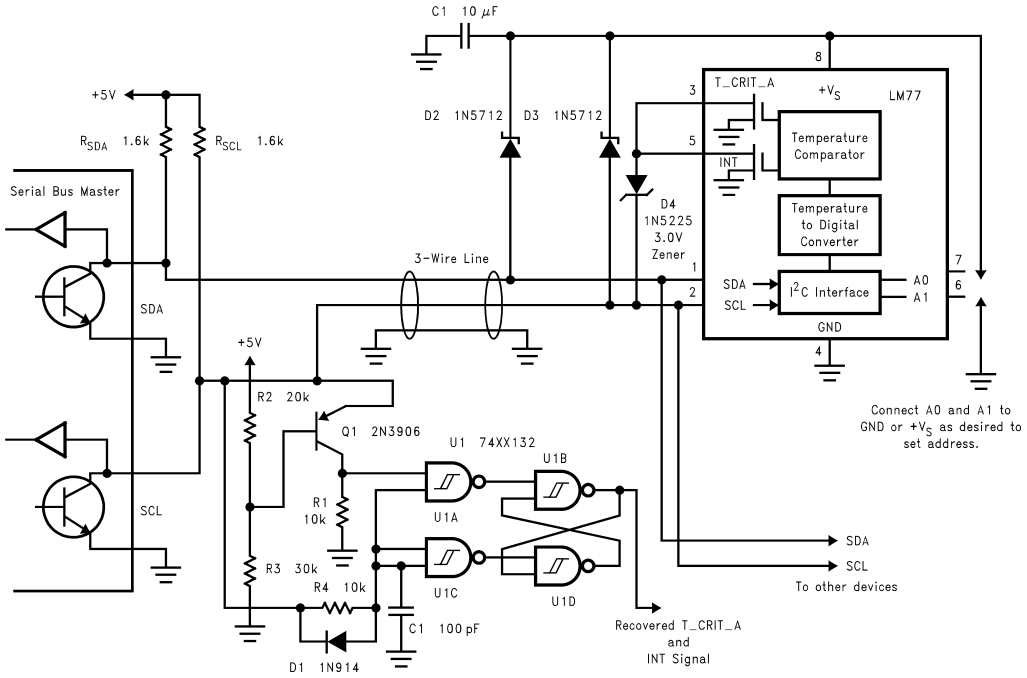
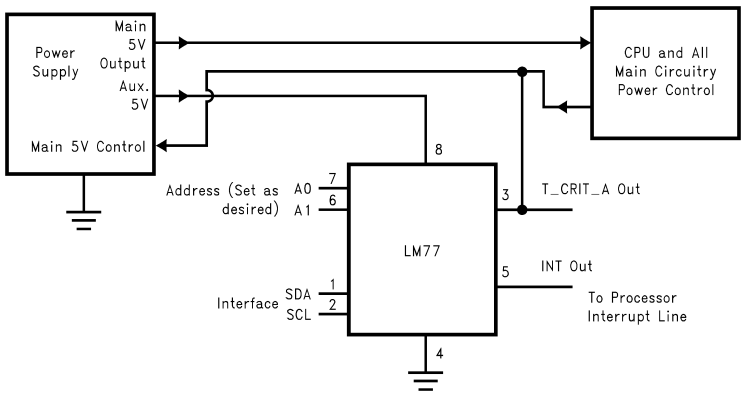


Figure 18. Remote HVAC temperature sensor communicates via 3 wires including thermostat signals



By powering the LM77 from auxilary output of the power supply, a non-functioning overheated computer can be powered down to preserve as much of the system as possible.

Figure 19. ACPI Compatible Terminal Alarm Shutdown

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM77CIM-3	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-55 to 125	LM77 CIM-3	
LM77CIM-3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 125	LM77 CIM-3	Samples
LM77CIM-5/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 125	LM77 CIM-5	Samples
LM77CIMM-3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 125	T06C	Samples
LM77CIMM-5/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 125	T07C	Samples
LM77CIMMX-3/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 125	T06C	Samples
LM77CIMX-3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 125	LM77 CIM-3	Samples
LM77CIMX-5/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 125	LM77 CIM-5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

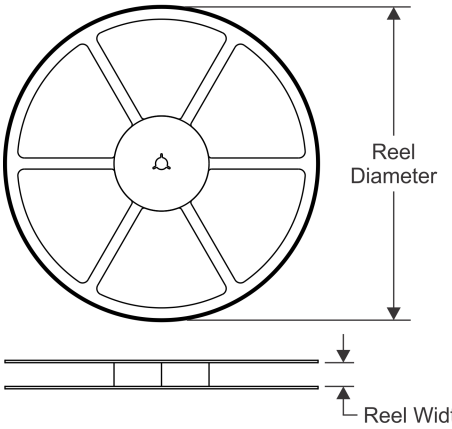
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

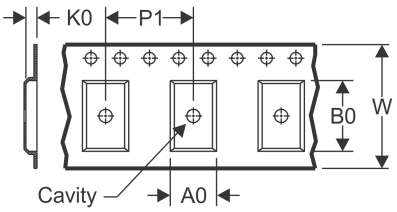
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

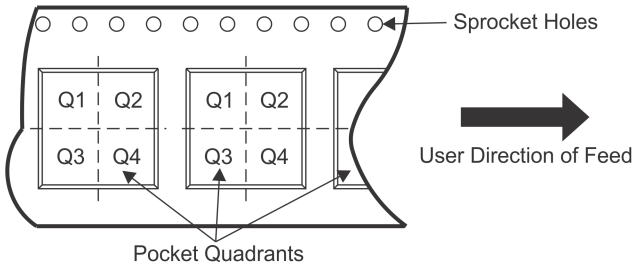


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

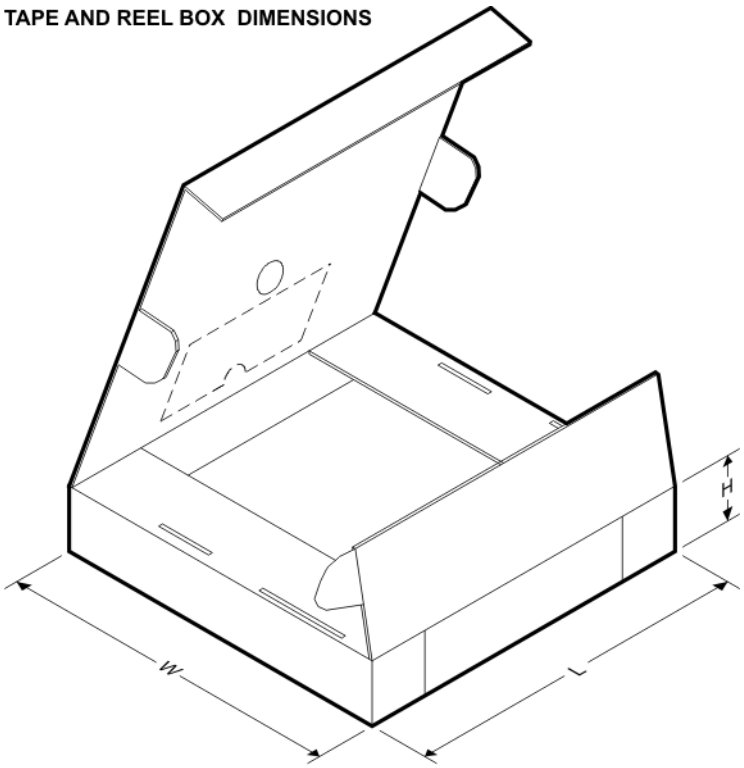
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

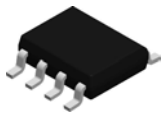
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM77CIMM-3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM77CIMM-5/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM77CIMMX-3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM77CIMX-3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM77CIMX-5/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM77CIMM-3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM77CIMM-5/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM77CIMMX-3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM77CIMX-3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM77CIMX-5/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

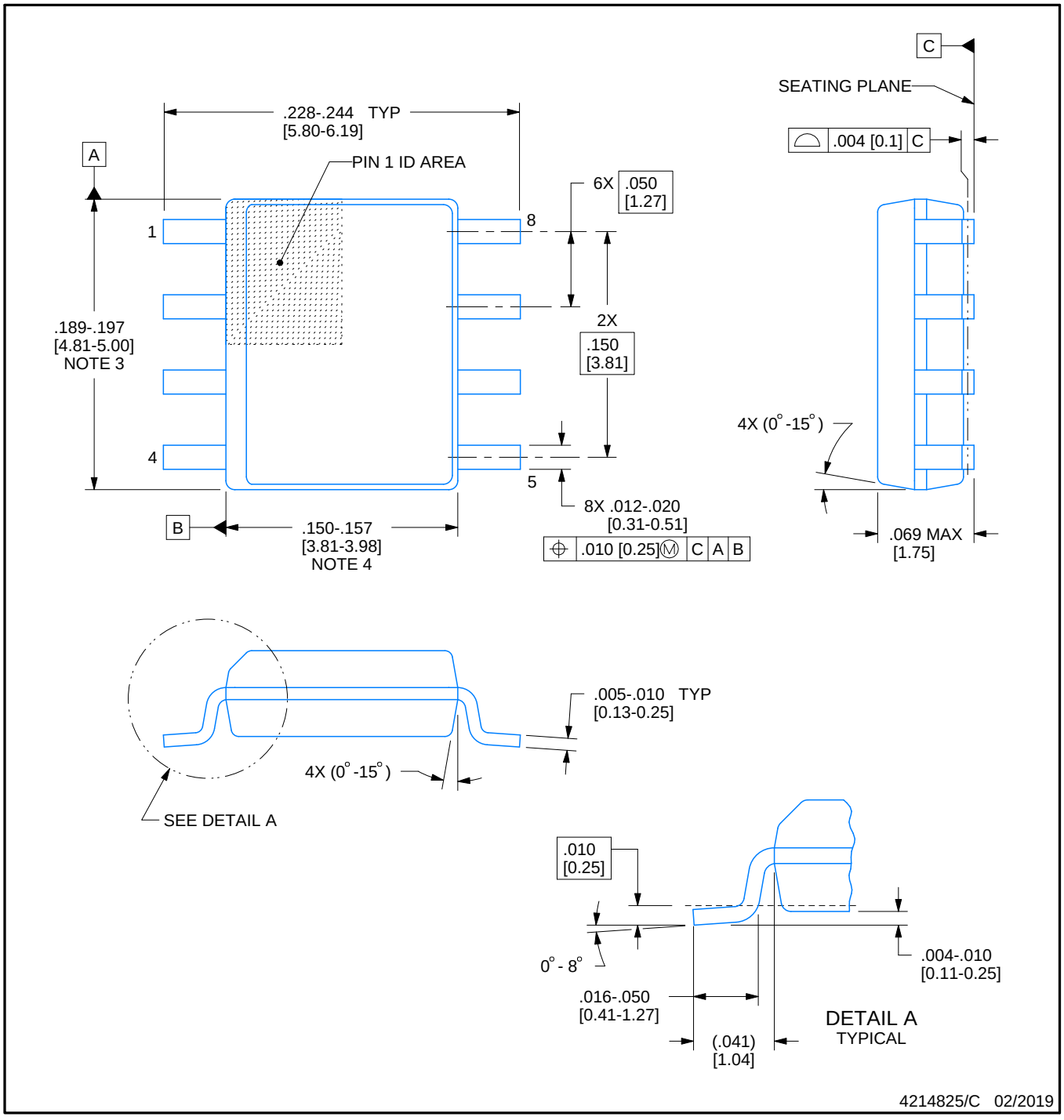


PACKAGE OUTLINE

D0008A

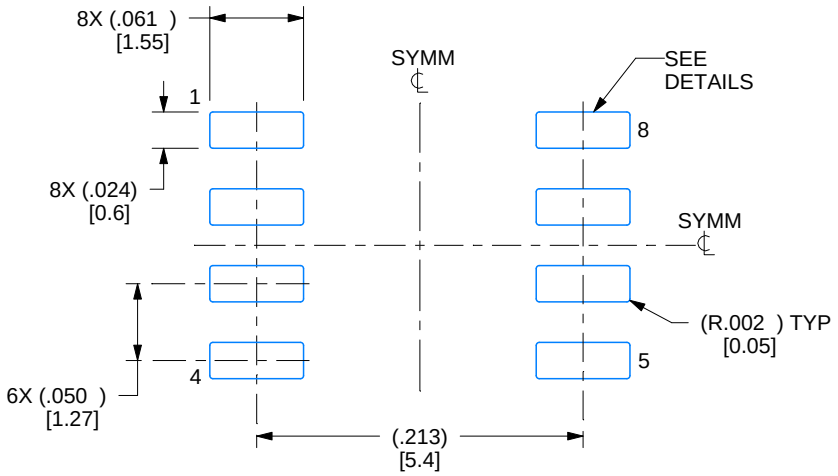
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

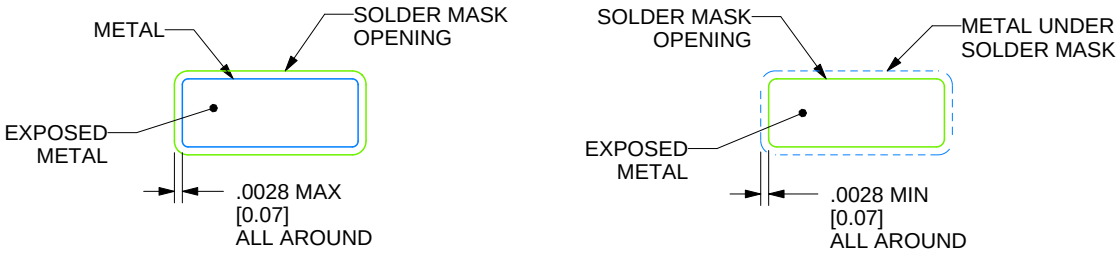


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

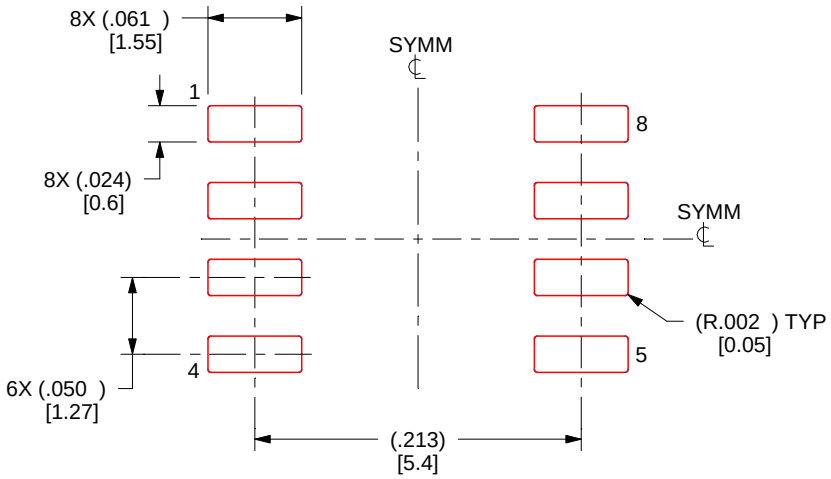
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



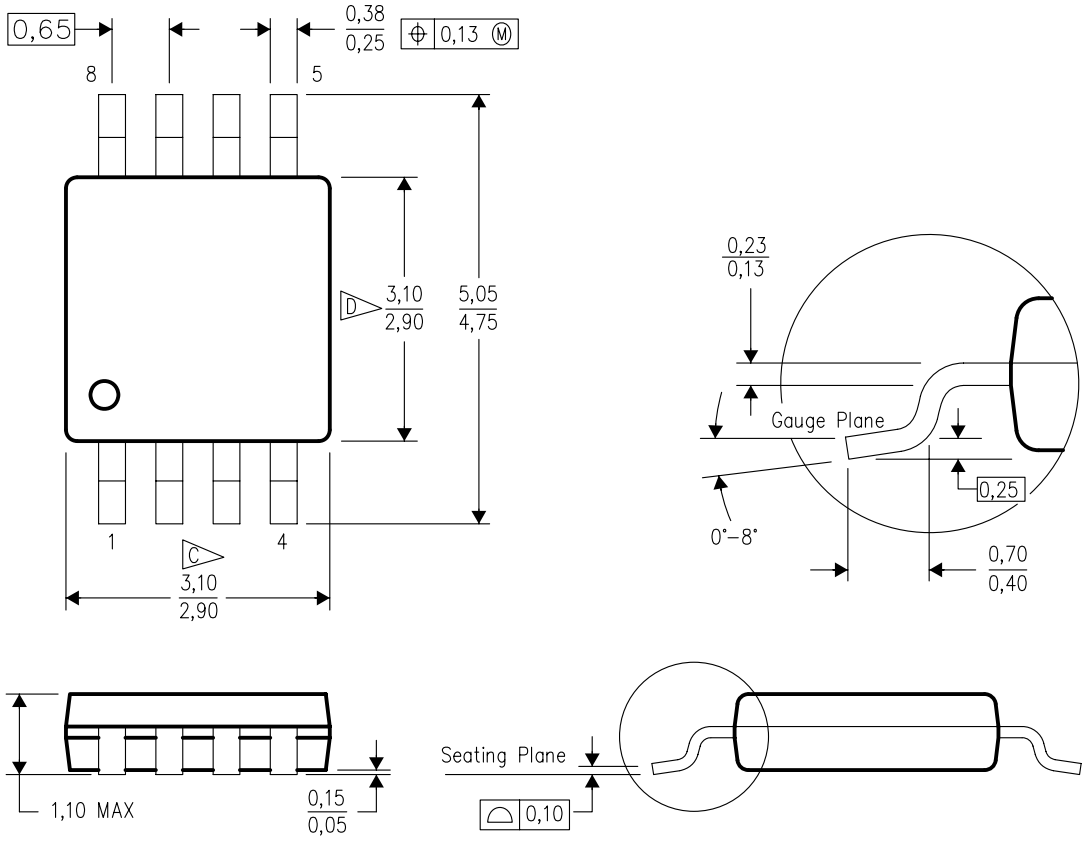
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

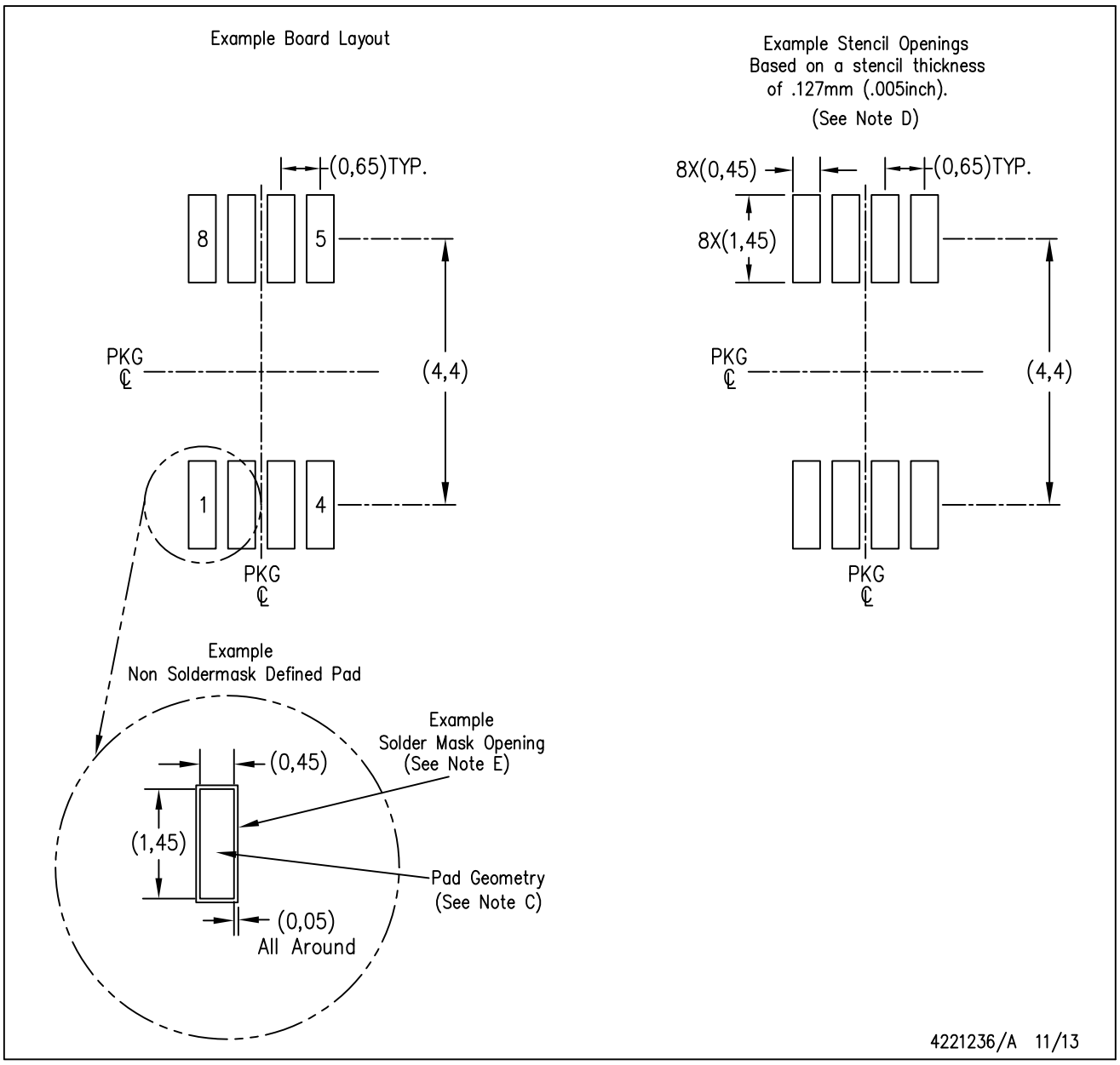
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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