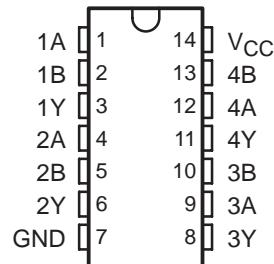


- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree<sup>†</sup>**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**

<sup>†</sup> Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Operates From 1.65 V to 3.6 V**
- **Max  $t_{pd}$  of 3 ns at 3.3 V**
- **$\pm 24$ -mA Output Drive at 3.3 V**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

D OR PW PACKAGE  
(TOP VIEW)



### description/ordering information

The SN74ALVC00 quadruple 2-input positive-NAND gate is designed for 1.65-V to 3.6-V V<sub>CC</sub> operation.

The device performs the Boolean function  $Y = \overline{A} \bullet \overline{B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

### ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE <sup>‡</sup> |               | ORDERABLE PART NUMBER         | TOP-SIDE MARKING |
|----------------|----------------------|---------------|-------------------------------|------------------|
| –40°C to 85°C  | SOIC – D             | Tape and reel | SN74ALVC00IDREP               | ALVC00IEP        |
|                | TSSOP – PW           | Tape and reel | SN74ALVC00IPWREP <sup>§</sup> | ALVC00E          |

<sup>‡</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

<sup>§</sup> Product Preview

FUNCTION TABLE  
(each gate)

| INPUTS |   | OUTPUT |
|--------|---|--------|
| A      | B | Y      |
| H      | H | L      |
| L      | X | H      |
| X      | L | H      |

### logic diagram, each gate (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74ALVC00-EP

## QUADRUPLE 2-INPUT POSITIVE-NAND GATE

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|  |                            |
|--|----------------------------|
| Supply voltage range, $V_{CC}$ .....                                   | -0.5 V to 4.6 V            |
| Input voltage range, $V_I$ (see Note 1) .....                          | -0.5 V to 4.6 V            |
| Output voltage range, $V_O$ (see Notes 1 and 2) .....                  | -0.5 V to $V_{CC}$ + 0.5 V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....                      | -50 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....                     | -50 mA                     |
| Continuous output current, $I_O$ .....                                 | $\pm$ 50 mA                |
| Continuous current through $V_{CC}$ or GND .....                       | $\pm$ 100 mA               |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): D package ..... | 86°C/W                     |
| PW package .....   | 113°C/W                    |

Storage temperature range,  $T_{STG}$  .....

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 4.6 V maximum.  
 3. The package thermal impedance is calculated in accordance with JEDEC 51-7.

### recommended operating conditions (see Note 4)

|                     |                                    | MIN                         | MAX                  | UNIT |
|---------------------|------------------------------------|-----------------------------|----------------------|------|
| $V_{CC}$            | Supply voltage                     | 1.65                        | 3.6                  | V    |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 1.65$ V to 1.95 V | $0.65 \times V_{CC}$ | V    |
|                     |                                    | $V_{CC} = 2.3$ V to 2.7 V   | 1.7                  |      |
|                     |                                    | $V_{CC} = 2.7$ V to 3.6 V   | 2                    |      |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 1.65$ V to 1.95 V | $0.35 \times V_{CC}$ | V    |
|                     |                                    | $V_{CC} = 2.3$ V to 2.7 V   | 0.7                  |      |
|                     |                                    | $V_{CC} = 2.7$ V to 3.6 V   | 0.8                  |      |
| $V_I$               | Input voltage                      | 0                           | 3.6                  | V    |
| $V_O$               | Output voltage                     | 0                           | $V_{CC}$             | V    |
| $I_{OH}$            | High-level output current          | $V_{CC} = 1.65$ V           | -4                   | mA   |
|                     |                                    | $V_{CC} = 2.3$ V            | -12                  |      |
|                     |                                    | $V_{CC} = 2.7$ V            | -12                  |      |
|                     |                                    | $V_{CC} = 3$ V              | -24                  |      |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 1.65$ V           | 4                    | mA   |
|                     |                                    | $V_{CC} = 2.3$ V            | 12                   |      |
|                     |                                    | $V_{CC} = 2.7$ V            | 12                   |      |
|                     |                                    | $V_{CC} = 3$ V              | 24                   |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |                             | 5                    | ns/V |
| $T_A$               | Operating free-air temperature     | -40                         | 85                   | °C   |

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER        | TEST CONDITIONS  | V <sub>CC</sub> | MIN                  | TYP <sup>†</sup> | MAX | UNIT |
|------------------|--|-----------------|----------------------|------------------|-----|------|
| V <sub>OH</sub>  | I <sub>OH</sub> = -100 µA  | 1.65 V to 3.6 V | V <sub>CC</sub> -0.2 |                  |     | V    |
|                  | I <sub>OH</sub> = -4 mA  | 1.65 V          | 1.2                  |                  |     |      |
|                  | I <sub>OH</sub> = -6 mA  | 2.3 V           | 2                    |                  |     |      |
|                  | I <sub>OH</sub> = -12 mA   | 2.3 V           | 1.7                  |                  |     |      |
|                  |  | 2.7 V           | 2.2                  |                  |     |      |
|                  |  | 3 V             | 2.4                  |                  |     |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = -24 mA   | 3 V             | 2                    |                  |     | V    |
|                  | I <sub>OL</sub> = 100 µA   | 1.65 V to 3.6 V | 0.2                  |                  |     |      |
|                  | I <sub>OL</sub> = 4 mA   | 1.65 V          | 0.45                 |                  |     |      |
|                  | I <sub>OL</sub> = 6 mA   | 2.3 V           | 0.4                  |                  |     |      |
|                  | I <sub>OL</sub> = 12 mA  | 2.3 V           | 0.7                  |                  |     |      |
|                  |  | 2.7 V           | 0.4                  |                  |     |      |
| I <sub>I</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.6 V           |                      | ±5               | µA  |      |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V           |                      | 10               | µA  |      |
| ΔI <sub>CC</sub> | One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND | 3 V to 3.6 V    |                      | 750              | µA  |      |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           |                      | 4.5              | pF  |      |

<sup>†</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

| PARAMETER       | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> = 1.8 V<br>± 0.15 V |     | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     |
|-----------------|-----------------|----------------|-------------------------------------|-----|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|
|                 |                 |                | MIN                                 | MAX | MIN                                | MAX | MIN                     | MAX | MIN                                | MAX |
| t <sub>pd</sub> | A or B          | Y              | 1                                   | 4.4 | 1                                  | 2.8 | 3.2                     | 0.5 | 3                                  | ns  |

**operating characteristics, T<sub>A</sub> = 25°C**

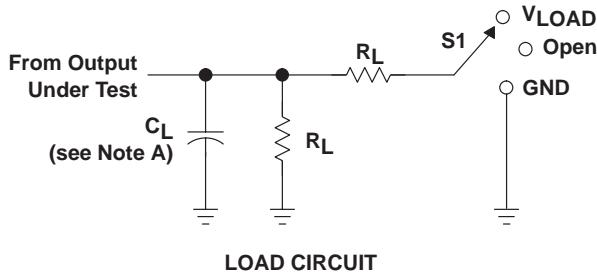
| PARAMETER       | TEST CONDITIONS                        | V <sub>CC</sub> = 1.8 V        |     | V <sub>CC</sub> = 2.5 V |     | V <sub>CC</sub> = 3.3 V |     | UNIT  |
|-----------------|--|--------------------------------|-----|-------------------------|-----|-------------------------|-----|-------|
|                 |  | MIN                            | MAX | MIN                     | MAX | MIN                     | MAX |       |
| C <sub>pd</sub> | Power dissipation capacitance per gate | C <sub>L</sub> = 0, f = 10 MHz |     | 20                      |     | 21                      |     | 23 pF |

# SN74ALVC00-EP

## QUADRUPLE 2-INPUT POSITIVE-NAND GATE

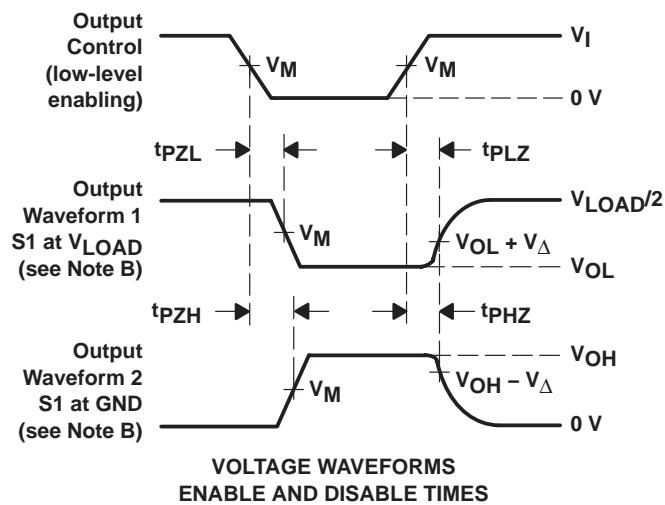
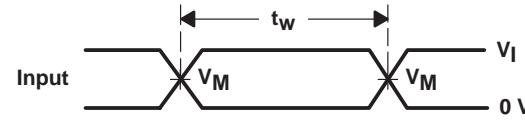
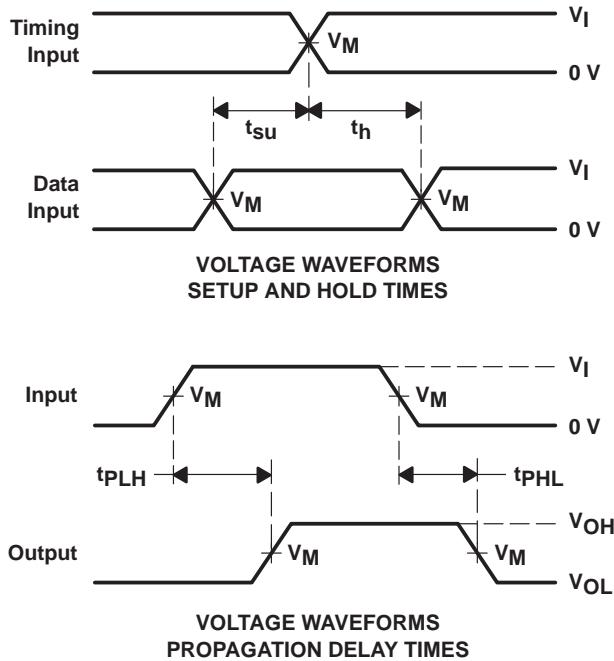
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### PARAMETER MEASUREMENT INFORMATION



| TEST              | S1         |
|-------------------|------------|
| $t_{pd}$          | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$           | INPUT    |               | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_\Delta$ |
|--------------------|----------|---------------|------------|-------------------|-------|--------------|------------|
|                    | $V_I$    | $t_r/t_f$     |            |                   |       |              |            |
| $1.8 V \pm 0.15 V$ | $V_{CC}$ | $\leq 2$ ns   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | $1 k\Omega$  | 0.15 V     |
| $2.5 \pm 0.2 V$    | $V_{CC}$ | $\leq 2$ ns   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | $500 \Omega$ | 0.15 V     |
| 2.7 V              | 2.7 V    | $\leq 2.5$ ns | 1.5 V      | 6 V               | 50 pF | $500 \Omega$ | 0.3 V      |
| $3.3 V \pm 0.3 V$  | 2.7 V    | $\leq 2.5$ ns | 1.5 V      | 6 V               | 50 pF | $500 \Omega$ | 0.3 V      |



NOTES:

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples        |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|----------------|
| SN74ALVC00IDREP  | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | ALVC00IEP               | <b>Samples</b> |
| V62/04685-01XE   | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | ALVC00IEP               | <b>Samples</b> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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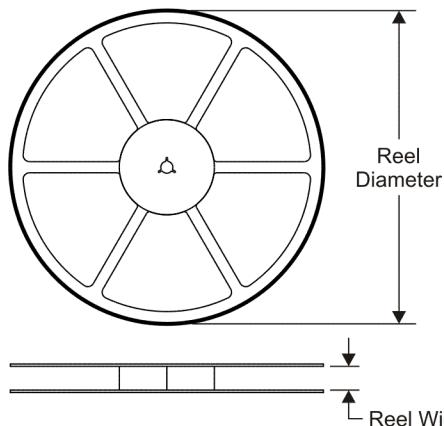
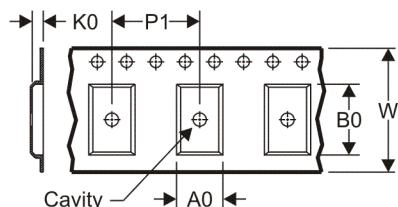
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**OTHER QUALIFIED VERSIONS OF SN74ALVC00-EP :**

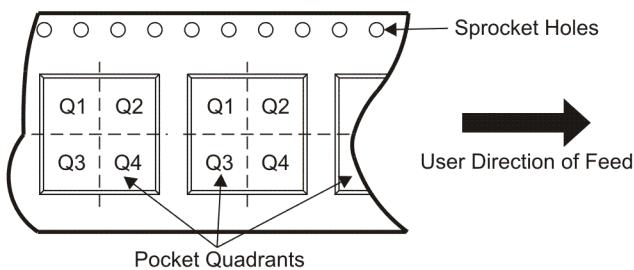
- Catalog: [SN74ALVC00](#)
- Automotive: [SN74ALVC00-Q1](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


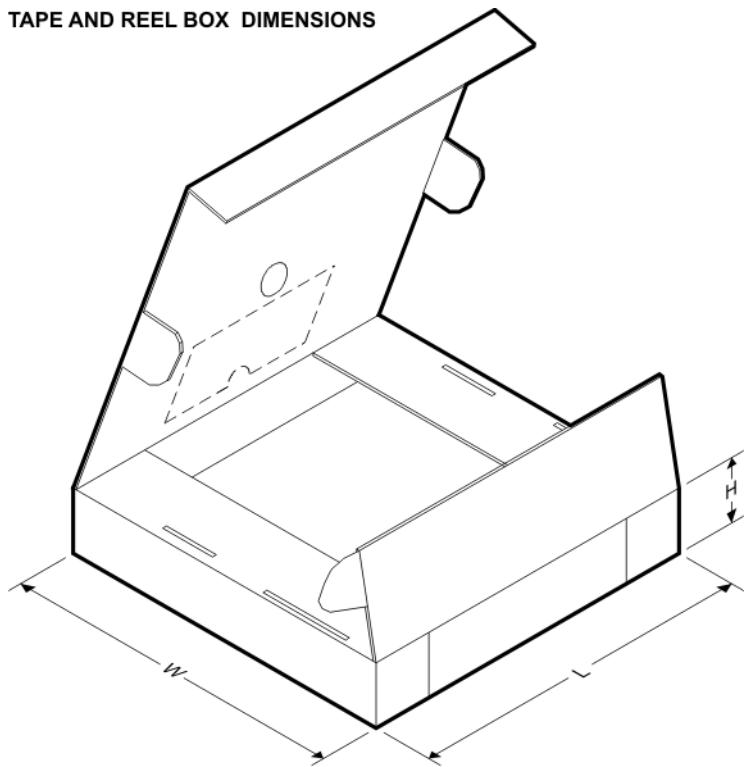
|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALVC00IDREP | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**

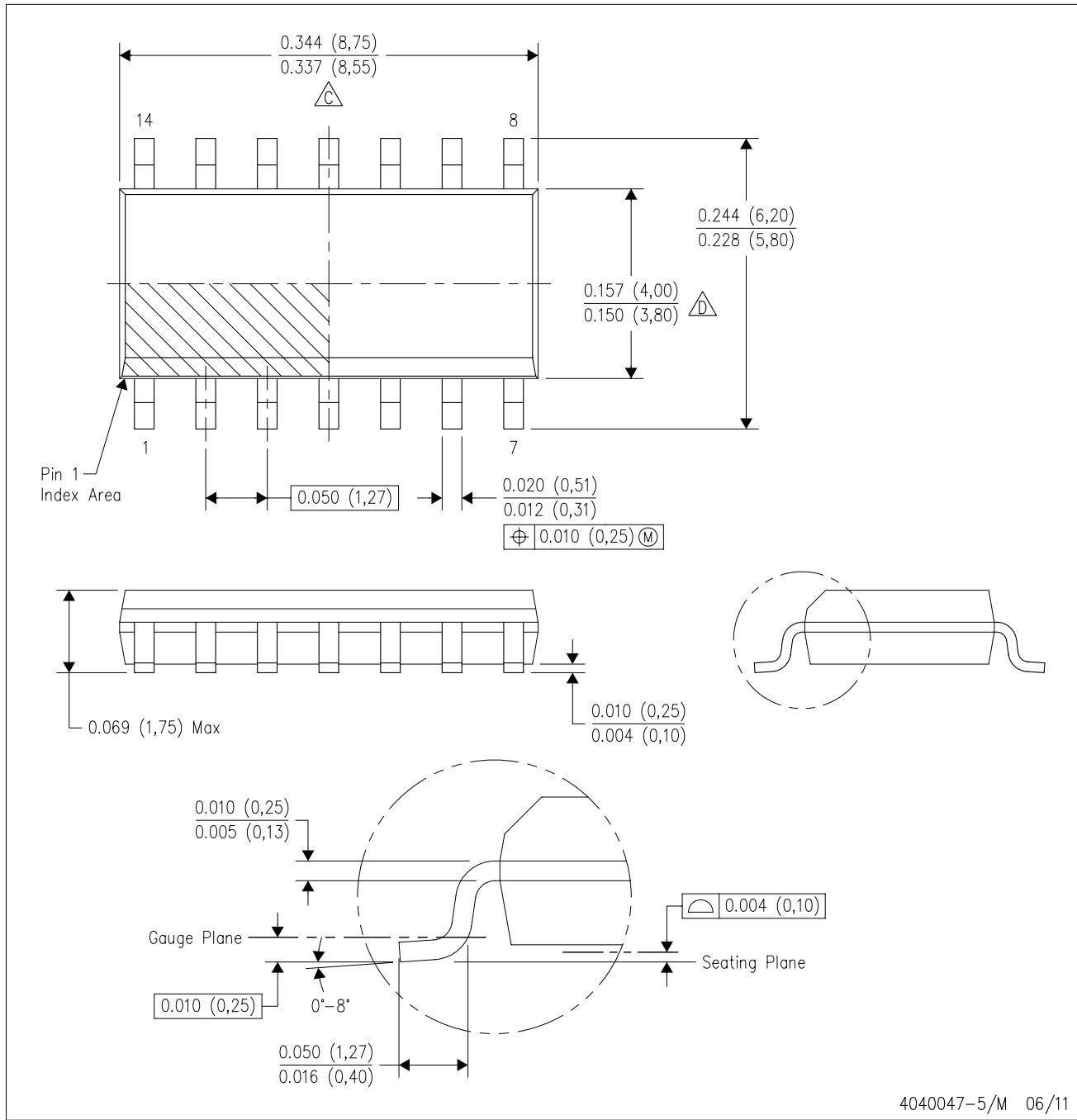


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALVC00IDREP | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

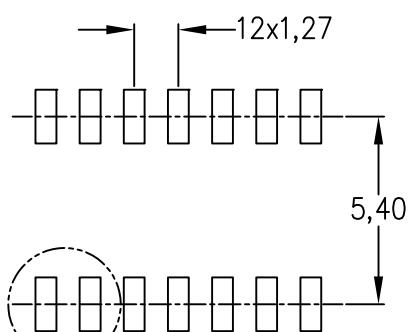
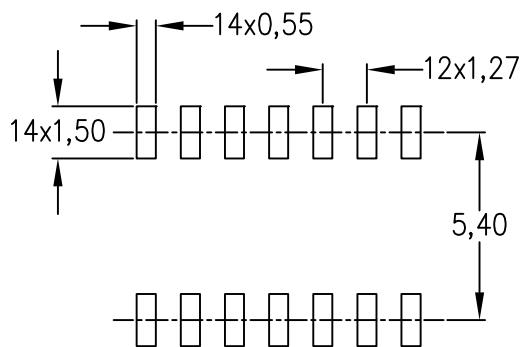
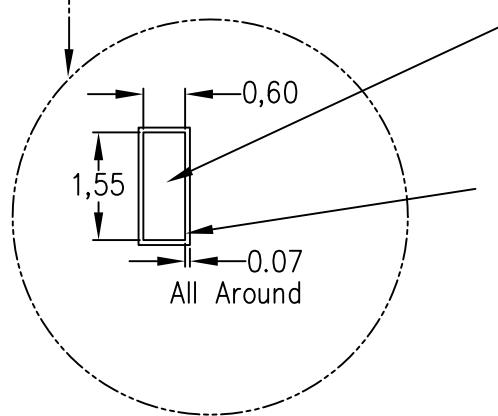
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211283-3/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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