

## P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>e</sup>	Q <sub>g</sub> (Typ.)
- 20	0.080 at V <sub>GS</sub> = - 4.5 V	- 10.5	7.7 nC
	0.102 at V <sub>GS</sub> = - 2.5 V	- 9.3	
	0.128 at V <sub>GS</sub> = - 1.8 V	- 3.5	
	0.198 at V <sub>GS</sub> = - 1.5 V	- 2.5	
	0.600 at V <sub>GS</sub> = - 1.2 V	- 0.5	

### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET

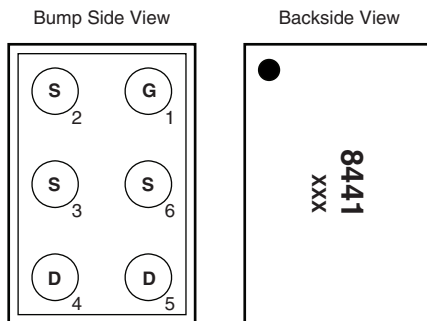
### APPLICATIONS

- Low Threshold Load Switch for Portable Devices
  - Low Power Consumption
  - Increased Battery Life

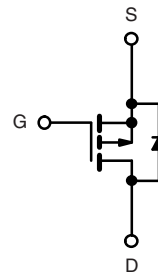


**RoHS**  
COMPLIANT

### MICRO FOOT



**Device Marking:** 8441  
xxx = Date/Lot Traceability Code



**Ordering Information:** Si8441DB-T2-E1 (Lead (Pb)-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	- 20	V
Gate-Source Voltage	V <sub>GS</sub>	± 5	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	- 10.5
		T <sub>C</sub> = 70 °C	- 8.4
		T <sub>A</sub> = 25 °C	- 4.8 <sup>a, b</sup>
		T <sub>A</sub> = 70 °C	- 3.9 <sup>a, b</sup>
Pulsed Drain Current	I <sub>DM</sub>	- 15	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	- 2.3 <sup>a, b</sup>
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	13
		T <sub>C</sub> = 70 °C	8.4
		T <sub>A</sub> = 25 °C	2.77 <sup>a, b</sup>
		T <sub>A</sub> = 70 °C	1.77 <sup>a, b</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Package Reflow Conditions <sup>c</sup>	IR/Convection	260	

**Notes:**

- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Refer to IPC/JEDEC (J-STD-020C), no manual or hand soldering.
- In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.
- Based on T<sub>C</sub> = 25 °C.

**THERMAL RESISTANCE RATINGS**

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, b</sup>	$R_{thJA}$	37	45	°C/W
Maximum Junction-to-Case (Drain)	Steady State $R_{thJC}$	7	9.5	

## Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 85 °C/W.

c. Case is defined as top surface of the package.

**SPECIFICATIONS**  $T_J = 25\text{ °C}$ , unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-20		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		2.2			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.35		-0.7	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 5\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ °C}$			-10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-5			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -1\text{ A}$		0.066	0.080	$\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -1\text{ A}$		0.085	0.102	
		$V_{GS} = -1.8\text{ V}, I_D = -1\text{ A}$		0.105	0.128	
		$V_{GS} = -1.5\text{ V}, I_D = -1\text{ A}$		0.145	0.198	
		$V_{GS} = -1.2\text{ V}, I_D = -0.5\text{ A}$		0.200	0.600	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ A}$		7		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		600		pF
Output Capacitance	$C_{oss}$		130			
Reverse Transfer Capacitance	$C_{rss}$		70			
Total Gate Charge	$Q_g$	$V_{DS} = -10\text{ V}, V_{GS} = -5\text{ V}, I_D = -1\text{ A}$		8.5	13	nC
		$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = 1\text{ A}$		7.7	12	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = 1\text{ A}$		0.85		
Gate-Drain Charge	$Q_{gd}$		1.6			
Gate Resistance	$R_g$	$V_{GS} = -0.1\text{ V}, f = 1\text{ MHz}$		6.2		$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		15	25	ns
Rise Time	$t_r$		30	45		
Turn-Off Delay Time	$t_{d(off)}$		35	55		
Fall Time	$t_f$		10	15		



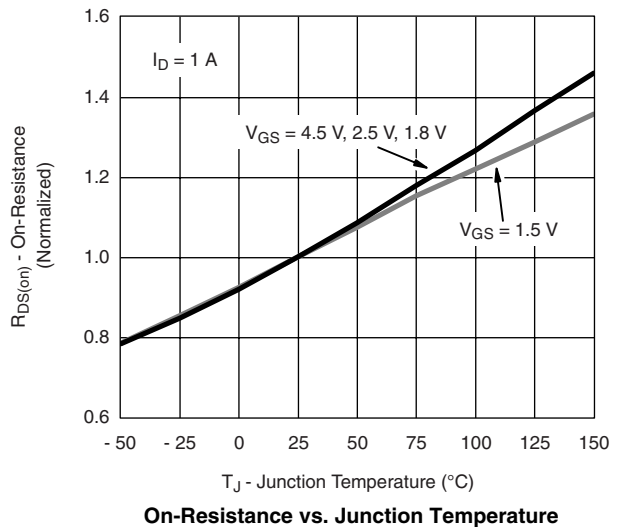
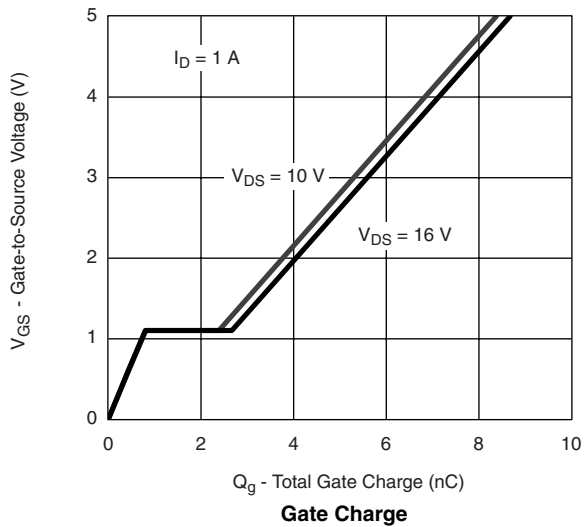
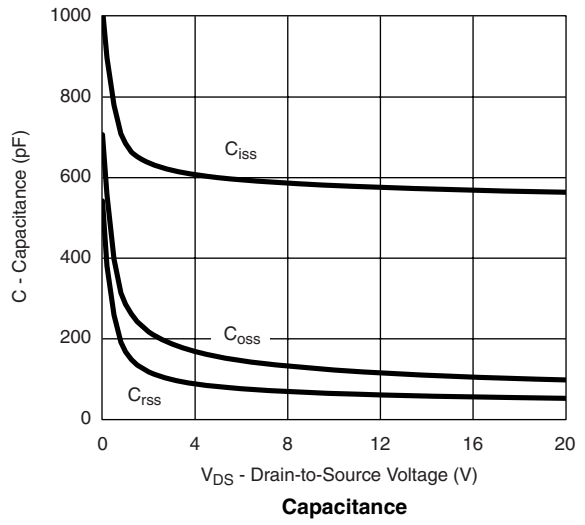
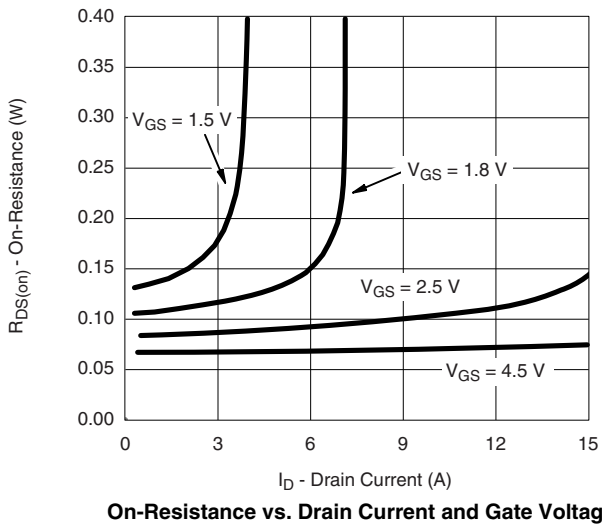
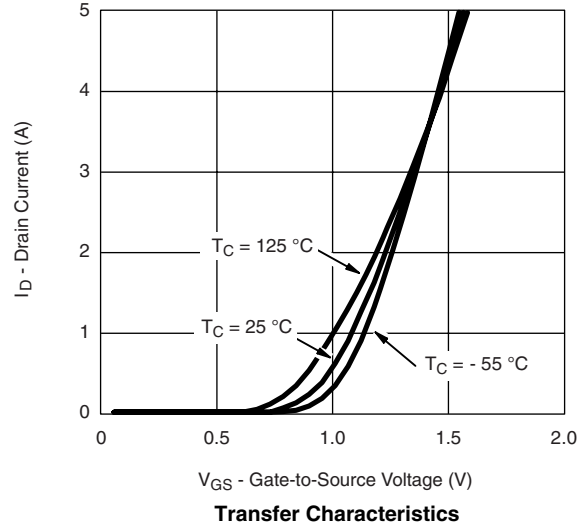
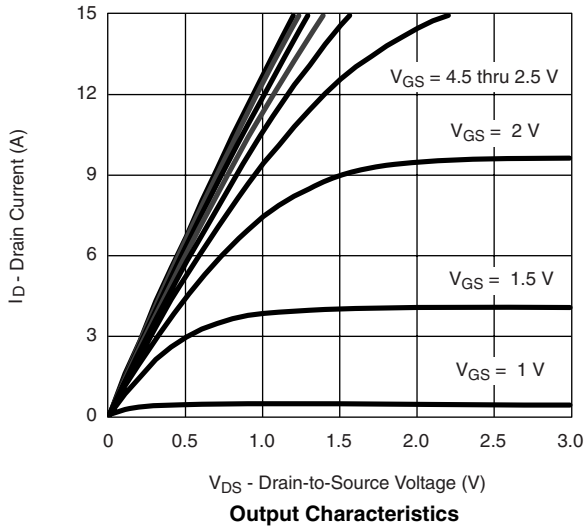
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			- 10.5	A
Pulse Diode Forward Current	$I_{SM}$				- 15	
Body Diode Voltage	$V_{SD}$	$I_S = -1\text{ A}, V_{GS} = 0\text{ V}$		- 0.7	- 1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = -1\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		20	40	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			7	15	nC
Reverse Recovery Fall Time	$t_a$			11		ns
Reverse Recovery Rise Time	$t_b$			9		

Notes:

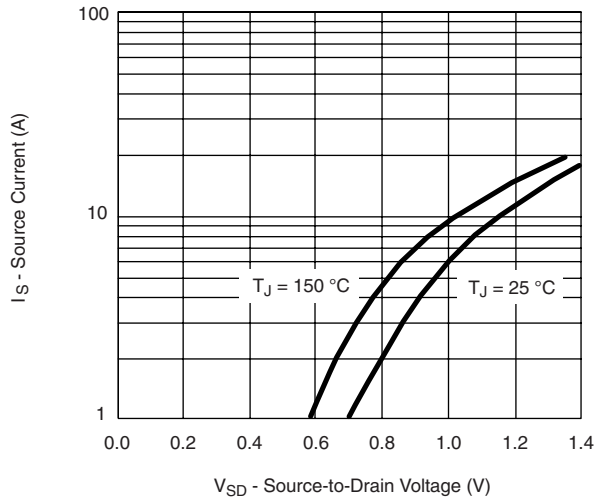
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

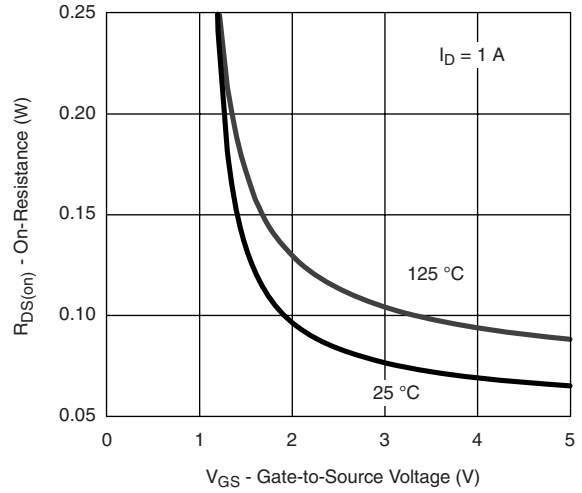
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



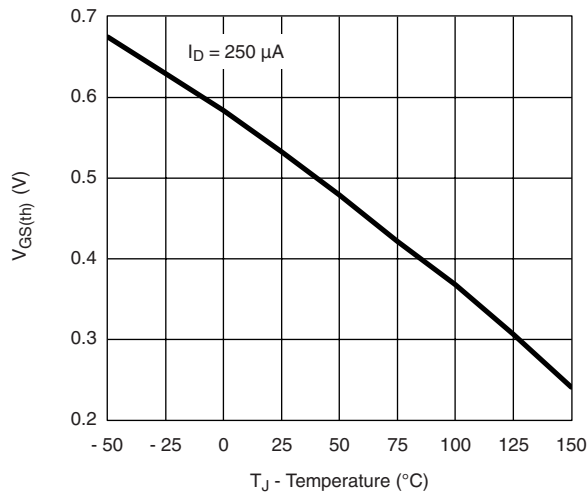
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



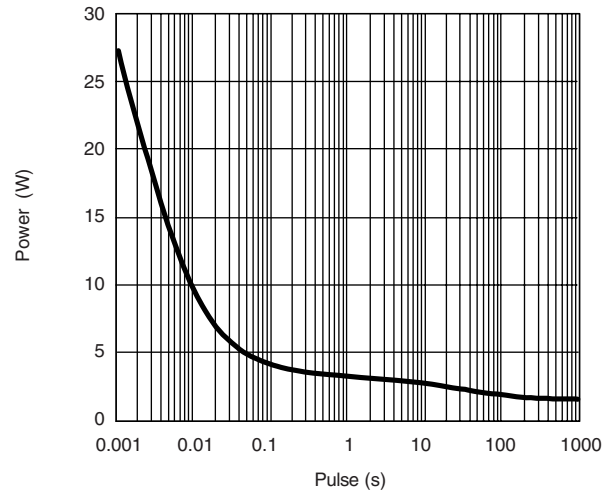
**Source-Drain Diode Forward Voltage**



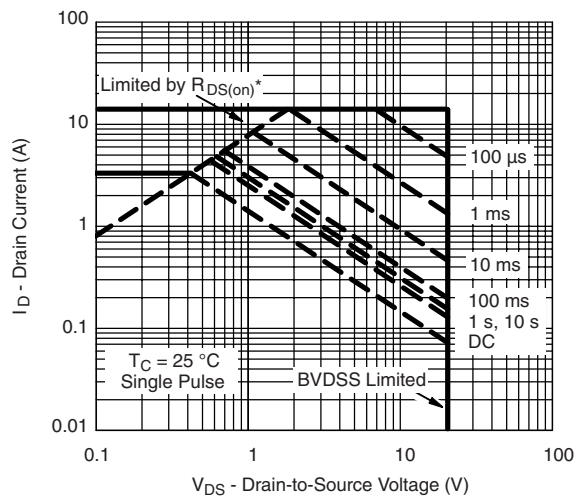
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



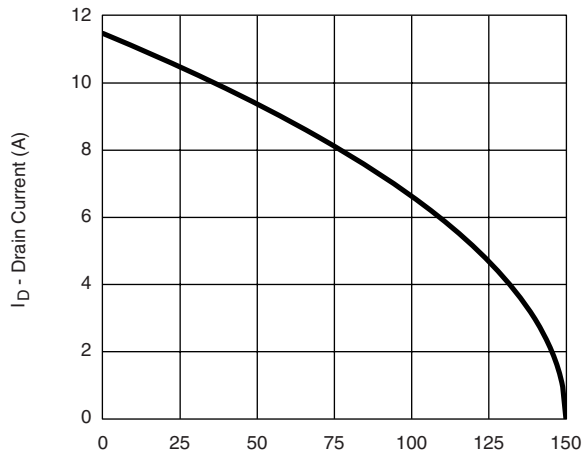
**Single Pulse Power, Junction-to-Ambient**



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

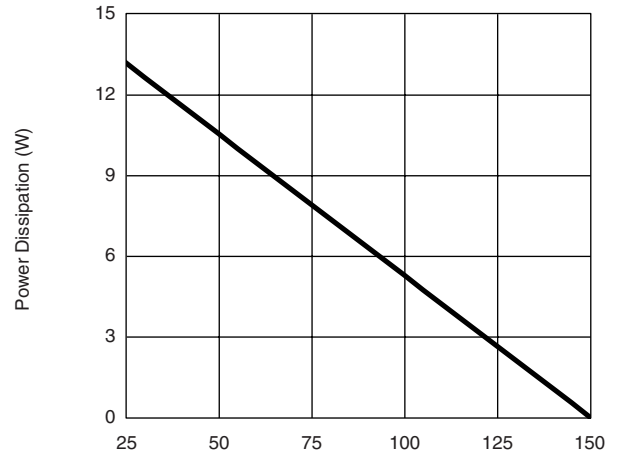
**Safe Operating Area, Junction-to-Ambient**

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



$T_C$  - Case Temperature (°C)

**Current Derating\***

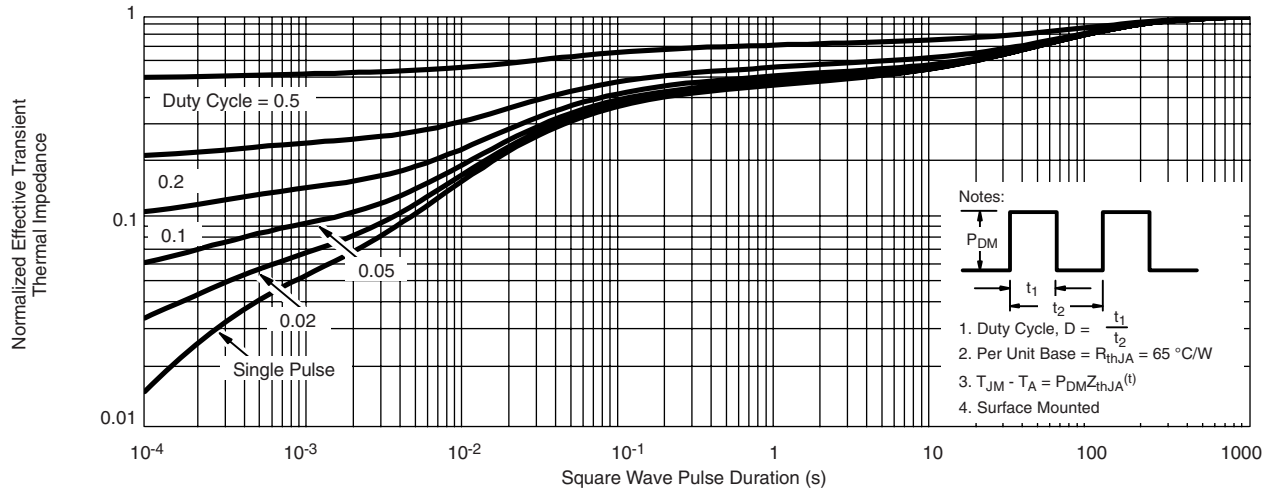


$T_C$  - Case Temperature (°C)

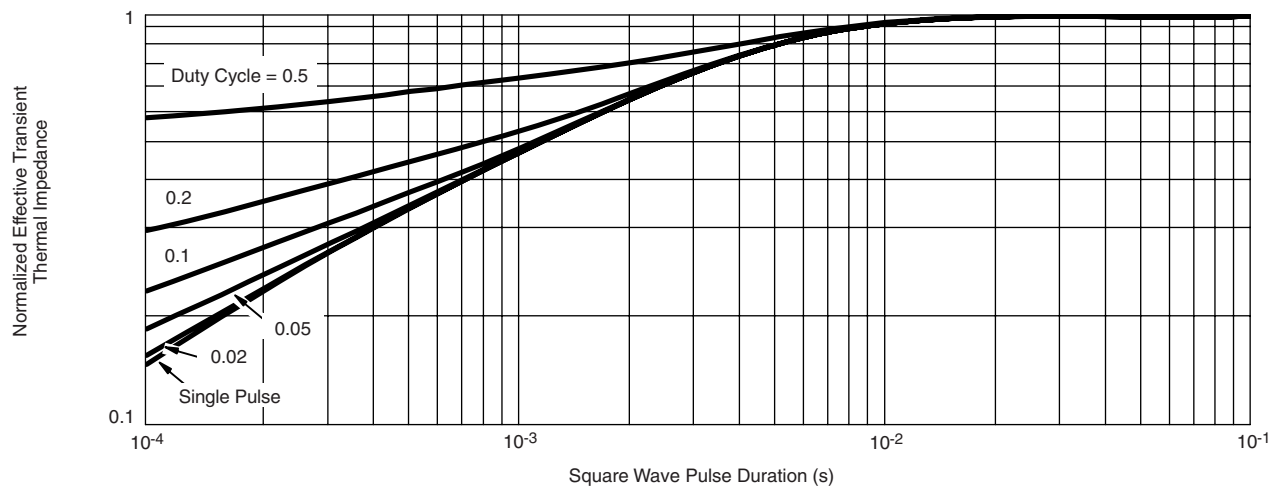
**Power Derating**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



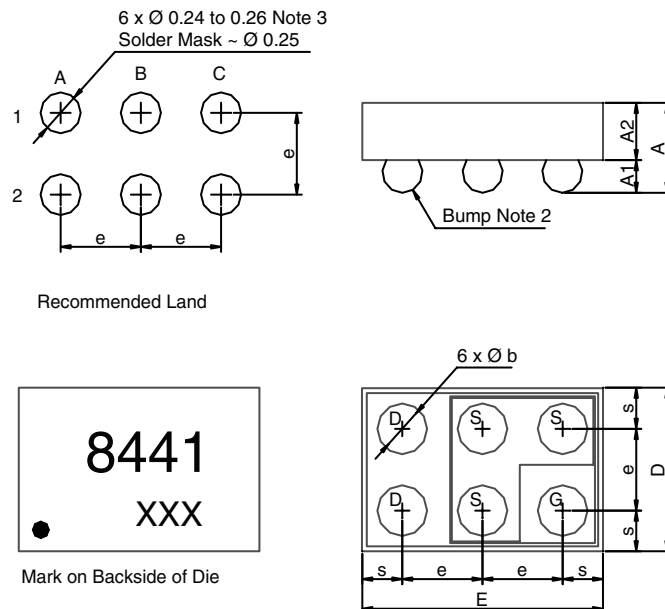
**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

## PACKAGE OUTLINE

### MICRO FOOT: 6-BUMP (2 x 3, 0.5 mm PITCH)



#### Notes (Unless Otherwise Specified):

- All dimensions are in millimeters.
- Six (6) solder bumps are lead (Pb)-free 95.5Sn, 3.8Ag, 0.7Cu with diameter  $\varnothing$  0.30 to 0.32 mm.
- Backside surface is coated with a Ti/Ni/Ag layer.
- Non-solder mask defined copper landing pad.
- is location of Pin 1.

Dim.	Millimeters <sup>a</sup>			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.510	0.575	0.590	0.0201	0.0224	0.0232
A <sub>1</sub>	0.220	0.250	0.280	0.0087	0.0098	0.0110
A <sub>2</sub>	0.290	0.300	0.310	0.0114	0.0118	0.0122
b	0.300	0.310	0.320	0.0118	0.0122	0.0126
e	0.500			0.0197		
s	0.230	0.250	0.270	0.0090	0.0098	0.0106
D	0.920	0.960	1.000	0.0362	0.0378	0.0394
E	1.420	1.460	1.500	0.0559	0.0575	0.0591

#### Notes:

- Use millimeters as the primary measurement.

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