



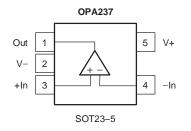
SINGLE-SUPPLY OPERATIONAL AMPLIFIERS MicroAmplifier[™] Series

FEATURES

- MICRO-SIZE, MINIATURE PACKAGES:
 - Single: SOT23-5, SO-8
 - Dual: MSOP-8, SO-8
 - Quad: SSOP-16 (Obsolete)
- LOW OFFSET VOLTAGE: 750μV max
- WIDE SUPPLY RANGE:
 - Single Supply: +2.7V to +36V
 - Dual Supply: ±1.35V to ±18V
- LOW QUIESCENT CURRENT: 350μV max
- WIDE BANDWIDTH: 1.5MHz

APPLICATIONS

- BATTERY-POWERED INSTRUMENTS
- PORTABLE DEVICES
- PCMCIA CARDS
- MEDICAL INSTRUMENTS
- TEST EQUIPMENT



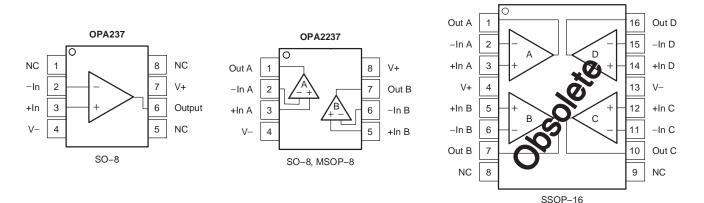
DESCRIPTION

The OPA237 op amp family is one of Texas Instruments' MicroAmplifier[™] series of miniature products. In addition to small size, these devices feature low offset voltage, low quiescent current, low bias current, and a wide supply range. Single, dual, and quad versions have identical specifications for maximum design flexibility. They are ideal for single-supply, battery-operated, and space-limited applications, such as PCMCIA cards and other portable instruments.

OPA237 series op amps can operate from either single or dual supplies. When operated from a single supply, the input common-mode range extends below ground and the output can swing to within 10mV of ground. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

Single, dual, and quad are offered in space-saving surface-mount packages. The single version is available in the ultra-miniature 5-lead SOT23-5 and SO-8 surface-mount. The dual version comes in a miniature MSOP-8 and SO-8 surface-mount. The quad version is obsolete. MSOP-8 has the same lead count as a SO-8 but half the size. The SOT23-5 is even smaller at one-fourth the size of an SO-8. All are specified for -40° C to $+85^{\circ}$ C operation. A macromodel is available for design analysis.

OPA4237



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MicroAmplifier is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, V+ to V	
Input Voltage	. (V–) –0.7V to (V+) +0.7V
Output Short-Circuit(2)	Continuous
Operating Temperature Range	
Storage Temperature Range	–55°C to +125°C
Junction Temperature Range	+150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Short circuit to ground, one amplifier per package.

PACKAGE/ORDERING INFORMATION(1)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT	PACKAGE-LEAD	PACKAGE DRAWING	PACKAGE MARKING	
Single OPA237NA	SOT23-5	DBV	A37A	
OPA237UA	SO-8 D		OPA237UA	
Dual OPA2237EA	MSOP-8	DGK	B37A	
OPA2237UA	SO-8	D	OPA2237UA	
Quad ⁽²⁾ OPA4237UA	SSOP-16	DBQ	OPA4237UA	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Quad version is obsolete.







ELECTRICAL CHARACTERISTICS: $V_S = +5V$

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. At $T_A = +25^{\circ}C$, $V_S = +5V$, $R_L = 10k\Omega$, connected to $V_S/2$, unless otherwise noted.

			A A		
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE Input Offset Voltage vs Temperature ⁽¹⁾ vs Power Supply (PSRR) Channel Separation (dual and quad)	V_{CM} = 2.5V Specified Temperature Range V_{S} = +2.7V to +36V		±250 ± 2 10 0.5	±750 ± 5 30	μV μ V/∘C μV/V μV/V
INPUT BIAS CURRENT Input Bias Current ⁽²⁾ Input Offset Current	V _{CM} = 2.5V V _{CM} = 2.5V		-10 ±0.5	-40 ±10	nA nA
NOISE Input Voltage Noise, f = 0.1 to 10Hz Input Voltage Noise Density, f = 1kHz Current Noise Density, f = 1kHz			1 28 60		μV _{PP} nV/√Hz fA/√Hz
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Ratio	$V_{CM} = -0.2V$ to 3.5V	-0.2 78	86	(V+) –1.5	V dB
INPUT IMPEDANCE Differential Common-Mode			5 • 10 ⁶ 4 5 • 10 ⁹ 2		Ω pF Ω pF
OPEN-LOOP GAIN Open-Loop Voltage Gain	$V_{O} = 0.5V$ to 4V	80	88		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product Slew Rate Settling Time, 0.1% 0.01%	$\label{eq:G} \begin{array}{l} G=1\\ G=-1, 3V Step, C_L=100 p F\\ G=-1, 3V Step, C_L=100 p F \end{array}$		1.4 0.5 11 16		MHz V/μs μs μs
OUTPUT					
Voltage Output, Positive Negative Positive Negative Positive Negative Short-Circuit Current Capacitive Load Drive (stable operation)	$\begin{split} R_L &= 100 k\Omega \text{ to Ground} \\ R_L &= 100 k\Omega \text{ to Ground} \\ R_L &= 100 k\Omega \text{ to } 2.5 V \\ R_L &= 100 k\Omega \text{ to } 2.5 V \\ R_L &= 10 k\Omega \text{ to } 2.5 V \\ R_L &= 10 k\Omega \text{ to } 2.5 V \end{split}$	(V+) -1 0.01 (V+) -1 0.12 (V+) -1 0.5	(V+) -0.75 0.001 (V+) -0.75 0.04 (V+) -0.75 0.35 -10/+4 ical Characterist	ic Curves	V V V V V MA
		Gee Typ		ic Cuives	
POWER SUPPLY Specified Operating Voltage Operating Range Quiescent Current (per amplifier)		+2.7	+5 170	+36 350	V V μA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance, θJA SOT23-5 MSOP-8 SSOP-16 (Obsolete)		-40 -55 -55	200 150 150	+85 +125 +125	°C °C °C W, °C/W °C/W
SO-8			150		°C/W

(1) Specified by wafer-level test to 95% confidence.

(2) Positive conventional current flows into the input terminals.



ELECTRICAL CHARACTERISTICS: $V_S = +2.7V$ Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. At $T_A = +25^{\circ}C$, $V_S = +2.7V$, $R_L = 10k\Omega$, connected to $V_S/2$, unless otherwise noted.

			OPA237UA, NA OPA2237UA, E OPA4237UA			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
OFFSET VOLTAGE Input Offset Voltage vs Temperature ⁽¹⁾ vs Power Supply (PSRR) Channel Separation (dual and quad)	$V_{CM} = 1V$ Specified Temperature Range $V_S = +2.7V \text{ to } +36V$		±250 ± 2 10 0.5	±750 ± 5 30	μV μ V/°C μV/V μV/V	
INPUT BIAS CURRENT Input Bias Current ⁽²⁾ Input Offset Current	$V_{CM} = 1V$ $V_{CM} = 1V$		-10 ±0.5	40 ±10	nA nA	
NOISE Input Voltage Noise, f = 0.1 to 10Hz Input Voltage Noise Density, f = 1kHz Current Noise Density, f = 1kHz			1 28 60		μV _{PP} nV/√Hz fA/√Hz	
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Ratio	$V_{CM} = -0.2V$ to 1.2V	-0.2 75	85	(V+) –1.5	V dB	
INPUT IMPEDANCE Differential Common-Mode			5 • 10 ⁶ 4 5 • 10 ⁹ 2		Ω pF Ω pF	
OPEN-LOOP GAIN Open-Loop Voltage Gain	$V_{O} = 0.5V$ to 1.7V	80	88		dB	
FREQUENCY RESPONSE						
Gain-Bandwidth Product Slew Rate Settling Time, 0.1% 0.01%	$\label{eq:G} \begin{array}{l} G=1\\ G=-1, \mbox{ 1V Step, } C_L=100\mbox{ pF}\\ G=-1, \mbox{ 1V Step, } C_L=100\mbox{ pF} \end{array}$		1.2 0.5 5 8		MHz V/μs μs μs	
OUTPUT Voltage Output, Positive Negative Positive Positive Negative Negative Short-Circuit Current Capacitive Load Drive (stable operation)	$\begin{split} R_L &= 100 k\Omega \text{ to Ground} \\ R_L &= 100 k\Omega \text{ to Ground} \\ R_L &= 100 k\Omega \text{ to } 1.35 \text{V} \\ R_L &= 100 k\Omega \text{ to } 1.35 \text{V} \\ R_L &= 10 k\Omega \text{ to } 1.35 \text{V} \\ R_L &= 10 k\Omega \text{ to } 1.35 \text{V} \end{split}$	(V+) −1 0.01 (V+) −1 0.06 (V+) −1 0.3 See Typi	(V+) -0.75 0.001 (V+) -0.75 0.02 (V+) -0.75 0.2 -5/+3.5 cal Characterist	ic Curves	V V V V V mA	
POWER SUPPLY Specified Operating Voltage Operating Range Quiescent Current (per amplifier)		+2.7	+2.7 160	+36 350	ν ν μΑ	
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance, θ _{JA} SOT23-5		-40 -55 -55	200	+85 +125 +125	°C °C °C	
MSOP-8 SSOP-16 (Obsolete) SO-8			150 150 150		°C/W °C/W °C/W	

Specified by wafer-level test to 95% confidence.
Positive conventional current flows into the input terminals.



ELECTRICAL CHARACTERISTICS: $V_S = \pm 15V$

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. At $T_A = +25^{\circ}C$, $V_S = \pm 15V$, $R_L = 10k\Omega$, connected to $V_S/2$, unless otherwise noted.

			OPA237UA, NA OPA2237UA, EA OPA4237UA					
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS			
OFFSET VOLTAGE Input Offset Voltage vs Temperature ⁽¹⁾ vs Power Supply (PSRR)	$V_{CM} = 0V$ Specified Temperature Range $V_S = \pm 1.35V \text{ to } \pm 18V$		±350 ± 2.5 10	±950 ± 7 30	μV μ V/°C μV/V			
Channel Separation (dual and quad)			0.5		μV/V			
INPUT BIAS CURRENT Input Bias Current ⁽²⁾ Input Offset Current	$V_{CM} = 0V$ $V_{CM} = 0V$		-8.5 ±0.5	-40 ±10	nA nA			
NOISE Input Voltage Noise, f = 0.1 to 10Hz Input Voltage Noise Density, f = 1kHz Current Noise Density, f = 1kHz			1 28 60		µVpp nV/√Hz fA/√Hz			
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Ratio	V _{CM} = -15V to 13.5V	(V–)–0.2 80	90	(V+) –1.5	V dB			
INPUT IMPEDANCE Differential Common-Mode			5 • 10 ⁶ 4 5 • 10 ⁹ 2		Ω pF Ω pF			
OPEN-LOOP GAIN Open-Loop Voltage Gain	$V_{O} = -14V$ to 13.8V	80	88		dB			
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time, 0.1% 0.01%	G = 1 G = -1, 10V Step, C _L = 100pF G = -1, 10V Step, C _L = 100pF		1.5 0.5 18 21		MHz V/μs μs μs			
OUTPUT Voltage Output, Positive Negative Positive Negative Short-Circuit Current Capacitive Load Drive (stable operation)	$R_{L} = 100k\Omega$ $R_{L} = 100k\Omega$ $R_{L} = 10k\Omega$ $R_{L} = 10k\Omega$	(V+) -1.2 (V-) +0.5 (V+) -1.2 (V-) +1 See Typi	(V+) −0.9 (V−) +0.3 (V+) −0.9 (V−) +0.85 −8/+4.5 cal Characterist	ic Curves	V V V W MA			
POWER SUPPLY Specified Operating Range Operating Range Quiescent Current (per amplifier)		±1.35	±15 ±200	±18 ±475	ν ν μΑ			
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance, θ _{JA} SOT23-5		-40 -55 -55	200	+85 +125 +125	⊃° ℃ ℃			
MSOP-8 SSOP-16 (Obsolete) SO-8			150 150 150		°C/W °C/W °C/W			

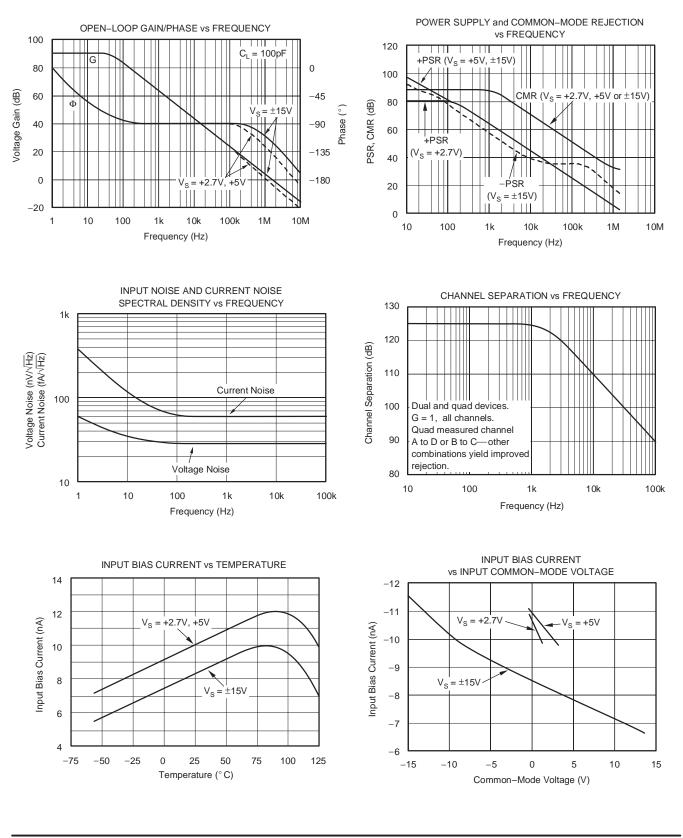
(1) Specified by wafer-level test to 95% confidence.

(2) Positive conventional current flows into the input terminals.



TYPICAL CHARACTERISTICS

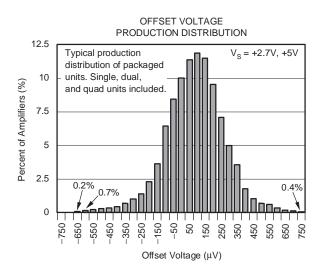
At $T_A = +25^{\circ}C$ and $R_L = 10k\Omega$, unless otherwise noted.





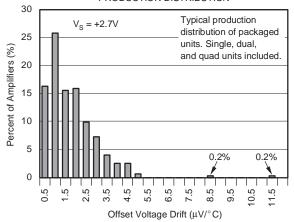
TYPICAL CHARACTERISTICS (Continued)

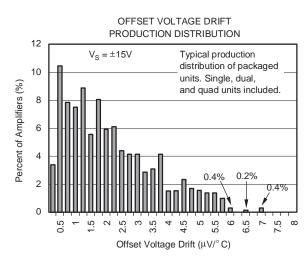
At $T_A = +25^{\circ}C$ and $R_L = 10k\Omega$, unless otherwise noted.



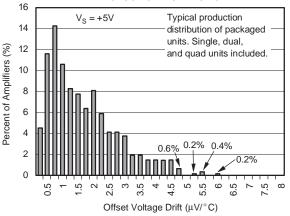
OFFSET VOLTAGE **PRODUCTION DISTRIBUTION** 9 Typical production $V_{S} = \pm 15V$ 8 distribution of packaged units. Single, dual, 7 Percent of Amplifiers (%) and quad units included. 6 5 4 3 2 0.1% 0.1% 1 *** ഫി l n n n 0 650 550 450 350 -50 50 150 250 350 550 650 750 850 950 250 150 950 850 750 Offset Voltage (µV)

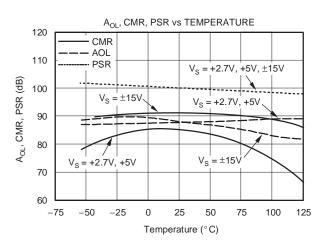
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION





OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

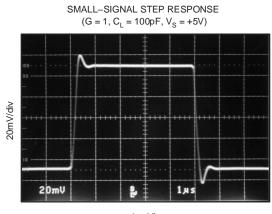




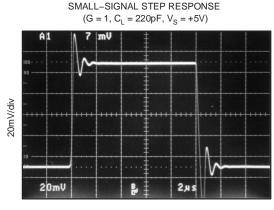


TYPICAL CHARACTERISTICS (Continued)

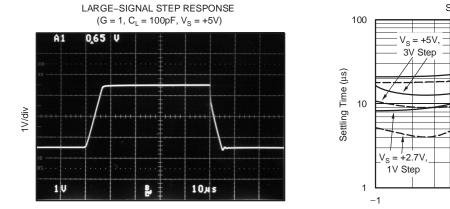
At $T_A = +25^{\circ}C$ and $R_L = 10k\Omega$, unless otherwise noted.



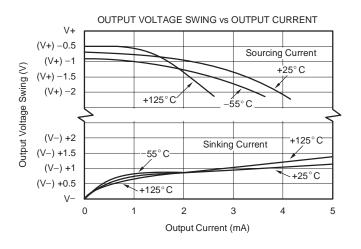
1µs/div

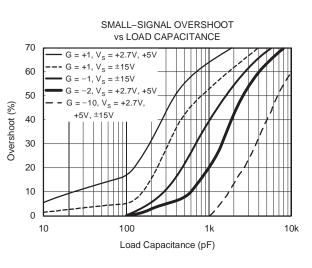


2µs/div



10µs/div



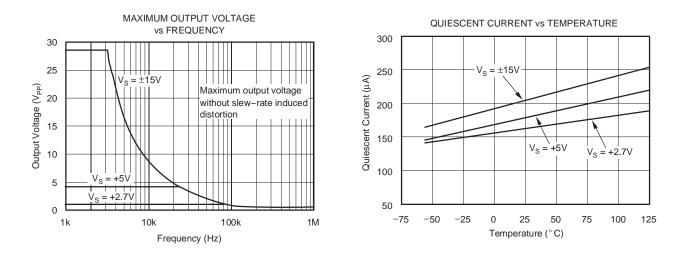


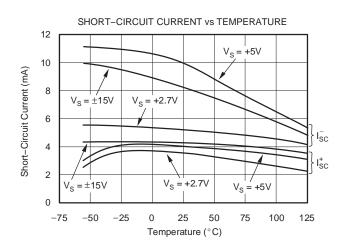
SETTLING TIME vs GAIN



TYPICAL CHARACTERISTICS (Continued)

At $T_A = +25^{\circ}C$ and $R_L = 10k\Omega$, unless otherwise noted.





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APPLICATION INFORMATION

OPA237 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors.

OPERATING VOLTAGE

OPA237 series op amps operate from single (+2.7V to +36V) or dual (\pm 1.35V to \pm 18V) supplies with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in typical performance curves. Specifications are production tested with +2.7V, +5V, and \pm 15V supplies.

OUTPUT CURRENT AND STABILITY

OPA237 series op amps can drive large capacitive loads. However, under certain limited output conditions any op amp may become unstable. Figure 1 shows the region where the OPA237 has a potential for instability. These load conditions are rarely encountered, especially for single supply applications. For example, take the case when a +5V supply with a 10k Ω load to V_S/2 is used. OPA237 series op amps remain stable with capacitive loads up to 4,000pF, if sinking current and up to 10,000pF, if sourcing current. Furthermore, in single-supply applications where the load is connected to ground, the op amp is only sourcing current, and as shown Figure 1, can drive 10,000pF with output currents up to 1.5mA.

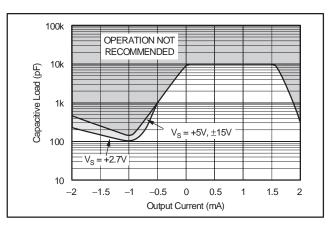


Figure 1. Stability-Capacitive Load vs Output Current

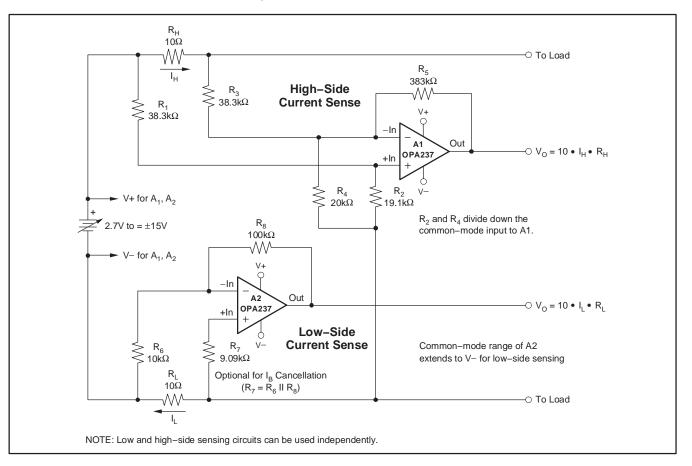


Figure 2. Low and High-Side Battery Current Sensing



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PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
OPA2237EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR		B37A	Samples
OPA2237EA/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B37A	Samples
OPA2237UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR		OPA 2237UA	Samples
OPA2237UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR		OPA 2237UA	Samples
OPA2237UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR		OPA 2237UA	Samples
OPA237NA/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	A37A	Samples
OPA237NA/250E4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	A37A	Samples
OPA237NA/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	A37A	Samples
OPA237NA/3KE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	A37A	Samples
OPA237UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 70	OPA 237UA	Samples
OPA237UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 70	OPA 237UA	Samples
OPA237UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 70	OPA 237UA	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.



PACKAGE OPTION ADDENDUM

6-Feb-2020

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2237EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2237EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2237UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA237NA/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA237NA/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA237UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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PACKAGE MATERIALS INFORMATION

4-Aug-2018



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2237EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2237EA/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2237UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA237NA/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA237NA/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA237UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. Refernce JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



DBV0005A

EXAMPLE BOARD LAYOUT

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



DBV0005A

EXAMPLE STENCIL DESIGN

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

8. Board assembly site may have different recommendations for stencil design.



D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.

- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



D0008A

EXAMPLE BOARD LAYOUT

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



D0008A

EXAMPLE STENCIL DESIGN

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.



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