TPS22932B Low Input Voltage, Ultralow rON Load Switch With Configurable Enable Logic and Controlled Slew-Rate

1 Features

- Input Voltage: 1.1 V to 3.6 V
- Ultralow ON-Resistance
  - r_{ON} = 55 mΩ at V_{IN} = 3.6 V
  - r_{ON} = 65 mΩ at V_{IN} = 2.5 V
  - r_{ON} = 75 mΩ at V_{IN} = 1.8 V
  - r_{ON} = 115 mΩ at V_{IN} = 1.2 V
- 500-mA Maximum Continuous Switch Current
- Quiescent Current < 1 µA
- Shutdown Current < 1 µA
- Low Control Threshold Allows Use of 1.2-V, 1.8-V, 2.5-V, and 3.3-V Logic
- Configurable Enable Logic
- Controlled Slew Rate to Avoid Inrush Currents: 165 µs at 1.8 V
- Six-Terminal Wafer Chip Scale Package (DSBGA)
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- PDAs
- Cell Phones
- GPS Devices
- MP3 Players
- Digital Cameras
- Peripheral Ports
- Portable Instrumentation

3 Description

The TPS22932B device is a low r_{ON} load switch with controlled turnon. The device contains a P-channel MOSFET that can operate over an input voltage range of 1.1 V to 3.6 V.

The switch is controlled by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, and noninverter. All inputs can be connected to V_{IN} or GND. The control pins can be connected to low-voltage GPIOs allowing the switch to be controlled by either 1.2-V, 1.8-V, 2.5-V, or 3.3-V logic signals while keeping extremely low quiescent current.

A 120-Ω on-chip load resistor is available for output quick discharge when the switch is turned off. The rise time (slew rate) of the device is internally controlled to avoid inrush current: the rise time of TPS22932B is 165 µs.

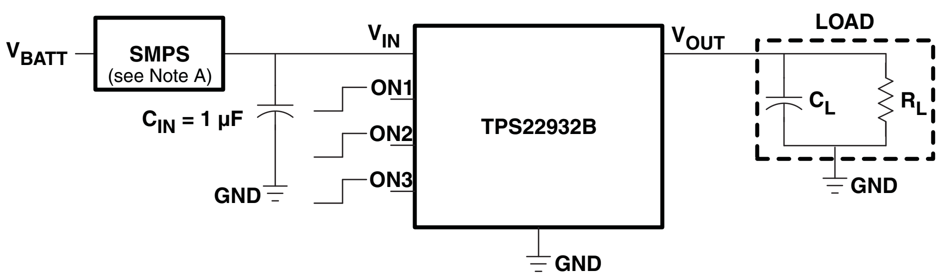
TPS22932B is available in a space-saving 6-pin DSBGA (YFP with 0.4-mm pitch). The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22932B	DSBGA (6)	0.80 mm × 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



A. Switched-mode power supply

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2013) to Revision C — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Moved Operating free-air temperature values in *Absolute Maximum Ratings* to the *Recommended Operating Conditions* 4

Changes from Revision A (November 2009) to Revision B — **Page**

- Aligned package description throughout data sheet. ... 1

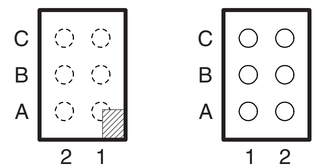
5 Device Comparison Table

DEVICE	r_{ON} at 1.8 V (TYP)	SLEW RATE (TYP at 3.3 V)	QUICK OUTPUT DISCHARGE [(1)]	MAX OUTPUT CURRENT	ENABLE
TPS22932B	75 mΩ	165 µs	Yes	500 mA	Active High

(1) This feature discharges the output of the switch to ground through a 120-Ω resistor, preventing the output from floating.

6 Pin Configuration and Functions

YFP Package
6-Pin DSBGA
Top View



Laser Marking View **Bump View**

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	V_{OUT}	O	Switch output
A2	V_{IN}	I	Switch input, bypass this input with a ceramic capacitor to ground
B1	GND	—	Ground
B2	ON1	I	Switch control input, active high - Do not leave floating
C2	ON2		
C1	ON3		

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	4	V
V_{OUT}	Output voltage		V_{IN} + 0.3	V
I_{MAX}	Maximum continuous switch current		500	mA
T_{lead}	Maximum lead temperature (10-s soldering time)		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
I_{OUT}	Output current		500	mA
V_{IN}	Input voltage	1.1	3.6	V
V_{OUT}	Output voltage		V_{IN}	
C_{IN}	Input capacitor	1 (1)		µF
T_A	Operating free-air temperature	–40	85	°C

(1) See *Application Information*.

7.4 Thermal Information

THERMAL METRIC (1)		TPS22932B YFP (DSBGA) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 1.1 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP (1)	MAX	UNIT
I_{IN}	Quiescent current	I_{OUT} = 0	V_{IN} = 1.1 V	Full		140	275	nA
			V_{IN} = 1.8 V			280	500	
			V_{IN} = 3.6 V			860	920	
$I_{IN(OFF)}$	OFF-state supply current	V_{ON} = GND, OUT = Open	V_{IN} = 1.1 V	Full		80	225	nA
			V_{IN} = 1.8 V			125	300	
			V_{IN} = 3.6 V			340	650	
$I_{IN(LEAKAGE)}$	OFF-state switch current	V_{ON} = GND, V_{OUT} = 0	V_{IN} = 1.1 V	Full		80	225	nA
			V_{IN} = 1.8 V			125	300	
			V_{IN} = 3.6 V			340	650	
r_{ON}	ON-state resistance	I_{OUT} = –200 mA	V_{IN} = 3.6 V	25°C		55	70	mΩ
				Full			85	
			V_{IN} = 2.5 V	25°C		65	80	
				Full			100	
			V_{IN} = 1.8 V	25°C		75	90	
				Full			110	
			V_{IN} = 1.2 V	25°C		115	130	
				Full			155	
			V_{IN} = 1.1 V	25°C		135	150	
				Full			170	
r_{PD}	Output pulldown resistance	V_{IN} = 3.3 V, V_{ON} = 0, I_{OUT} = 30 mA		25°C		75	120	Ω
I_{ON}	ON-state input leakage current	V_{ON} = 1.1 V to 3.6 V or GND		Full			1	µA
Control Inputs (ON1, ON2, ON3)								

(1) Typical values are at the specified V_{IN} and T_A = 25°C.

Electrical Characteristics (continued)

V_{IN} = 1.1 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP[(1)]	MAX	UNIT
	Input leakage current	V_{IN} = 1.1 V to 3.6 V or GND	Full			1	µA
V_{ON}	Control input voltage		Full			3.6	V
V_{T+}	Positive-going input voltage threshold	V_{IN} = 1.1 V to 1.8 V	Full	0.5		0.8	V
		V_{IN} = 1.8 V to 3.6 V		0.6		0.9	
$V_{T–}$	Negative-going input voltage threshold	V_{IN} = 1.1 V to 1.8 V	Full	0.2		0.6	V
		V_{IN} = 1.8 V to 3.6 V		0.3		0.7	
ΔV_T	Hysteresis (V_{T+} – $V_{T–}$)	V_{IN} = 1.1 V to 3.6 V	Full	0.2		0.6	V

7.6 Switching Characteristics, 1.2 V

V_{IN} = 1.2 V, R_{L_CHIP} = 120 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω	C_L = 0.1 µF		350		µs
			C_L = 1 µF		390		
			C_L = 3 µF		450		
t_{OFF}	Turnoff time	R_L = 500 Ω	C_L = 0.1 µF		30		µs
			C_L = 1 µF		70		
			C_L = 3 µF		160		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		240		µs
			C_L = 1 µF		240		
			C_L = 3 µF		260		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		20		µs
			C_L = 1 µF		150		
			C_L = 3 µF		450		

7.7 Switching Characteristics, 1.5 V

V_{IN} = 1.5 V, R_{L_CHIP} = 120 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω	C_L = 0.1 µF		290		µs
			C_L = 1 µF		320		
			C_L = 3 µF		350		
t_{OFF}	Turnoff time	R_L = 500 Ω	C_L = 0.1 µF		30		µs
			C_L = 1 µF		70		
			C_L = 3 µF		150		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		205		µs
			C_L = 1 µF		205		
			C_L = 3 µF		220		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		18		µs
			C_L = 1 µF		145		
			C_L = 3 µF		445		

7.8 Switching Characteristics, 1.8 V

V_{IN} = 1.8 V, R_{L_CHIP} = 120 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω	C_L = 0.1 µF		215		µs
			C_L = 1 µF		240		
			C_L = 3 µF		260		
t_{OFF}	Turnoff time	R_L = 500 Ω	C_L = 0.1 µF		24		µs
			C_L = 1 µF		60		
			C_L = 3 µF		142		
t_r	V_{OUT} rise time	R_L = 500	C_L = 0.1 µF		165		µs
			C_L = 1 µF		165		
			C_L = 3 µF		175		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		18		µs
			C_L = 1 µF		145		
			C_L = 3 µF		440		

7.9 Switching Characteristics, 2.5 V

V_{IN} = 2.5 V, R_{L_CHIP} = 120 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω	C_L = 0.1 µF		185		µs
			C_L = 1 µF		205		
			C_L = 3 µF		225		
t_{OFF}	Turnoff time	R_L = 500 Ω	C_L = 0.1 µF		2		µs
			C_L = 1 µF		60		
			C_L = 3 µF		140		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		145		µs
			C_L = 1 µF		150		
			C_L = 3 µF		160		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		18		µs
			C_L = 1 µF		147		
			C_L = 3 µF		445		

7.10 Switching Characteristics, 3 V

V_{IN} = 3 V, R_{L_CHIP} = 120 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω	C_L = 0.1 µF		170		µs
			C_L = 1 µF		190		
			C_L = 3 µF		210		
t_{OFF}	Turnoff time	R_L = 500 Ω	C_L = 0.1 µF		2		µs
			C_L = 1 µF		60		
			C_L = 3 µF		140		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		140		µs
			C_L = 1 µF		140		
			C_L = 3 µF		150		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		17		µs
			C_L = 1 µF		148		
			C_L = 3 µF		450		

7.11 Switching Characteristics, 3.3 V

V_{IN} = 3.3 V, R_{L_CHIP} = 120 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω	C_L = 0.1 µF		160		µs
			C_L = 1 µF		175		
			C_L = 3 µF		195		
t_{OFF}	Turnoff time	R_L = 500 Ω	C_L = 0.1 µF		20		µs
			C_L = 1 µF		55		
			C_L = 3 µF		135		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		135		µs
			C_L = 1 µF		135		
			C_L = 3 µF		145		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		17		µs
			C_L = 1 µF		148		
			C_L = 3 µF		450		

7.12 Typical Characteristics

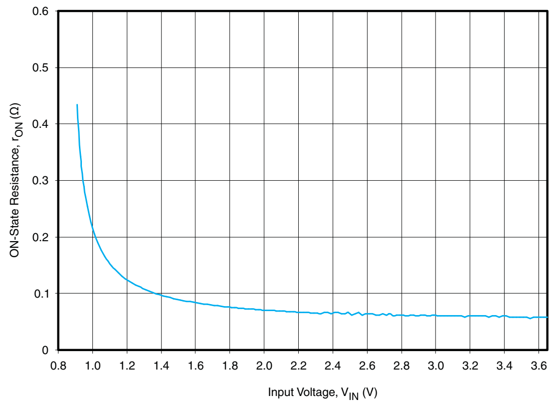


Figure 1. r_{ON} vs V_{IN}

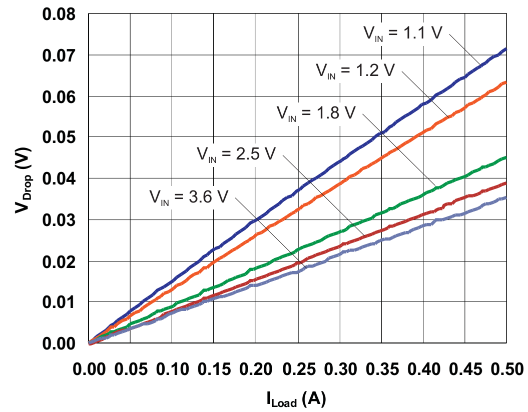
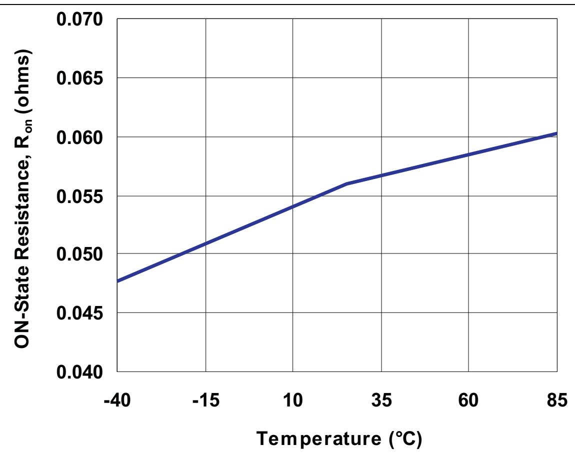
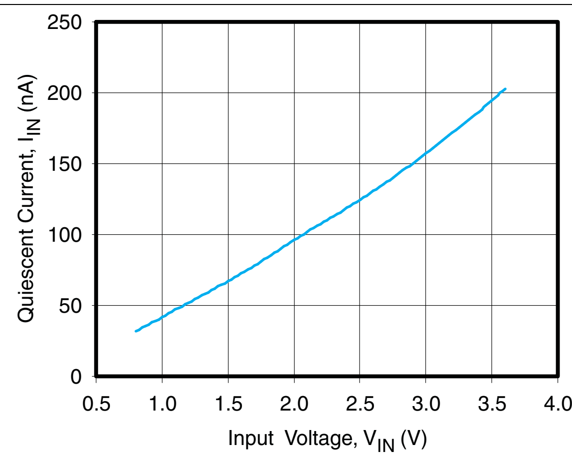


Figure 2. Voltage Drop vs Load Current



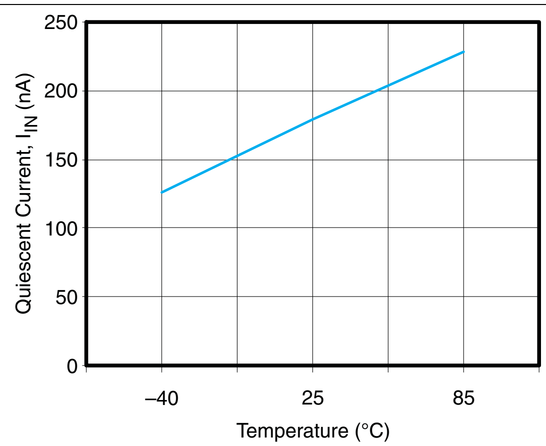
V_{IN} = 3.3 V

Figure 3. r_{ON} vs T_A



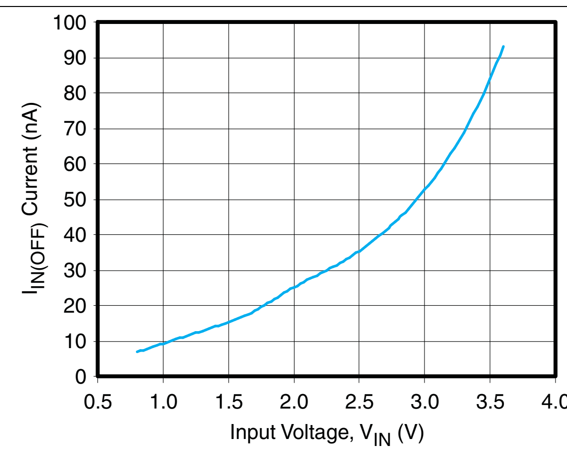
ON2 = V_{IN}, ON1–ON3 = 0 V, I_{out} = 0

Figure 4. Quiescent Current vs V_{IN}



V_{IN} = 3.3 V, ON2 = V_{IN}, ON1–ON3 = 0 V, I_{out} = 0

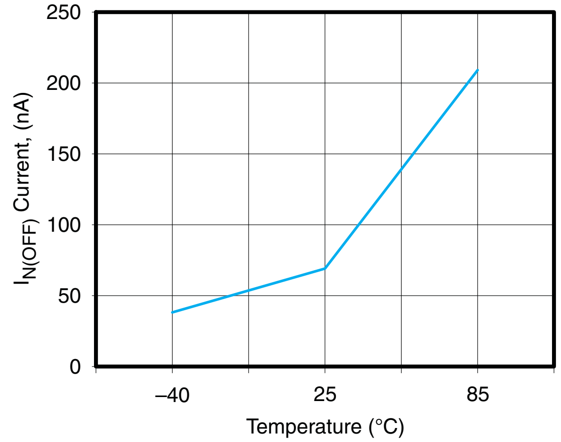
Figure 5. Quiescent Current vs T_A



ON1–ON2–ON3 = 0 V

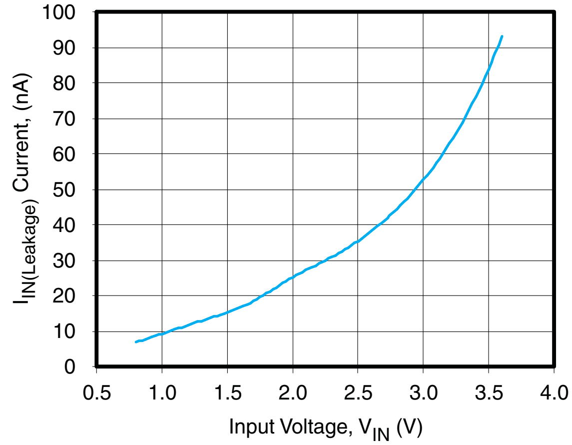
Figure 6. $I_{IN(OFF)}$ vs V_{IN}

Typical Characteristics (continued)



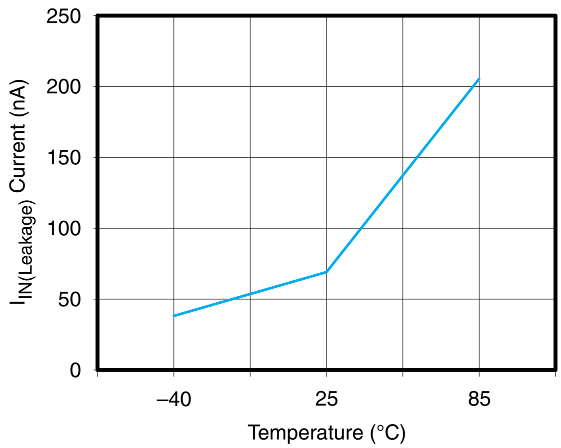
V_{IN} = 3.3 V, ON1–ON2–ON3 = 0 V

Figure 7. $I_{IN(OFF)}$ vs Temperature



ON1–ON2–ON3 = 0 V, V_{out} = 0

Figure 8. $I_{IN(Leakage)}$ vs V_{IN}



V_{IN} = 3.3 V, ON1–ON2–ON3 = 0 V

Figure 9. $I_{IN(Leakage)}$ vs Temperature

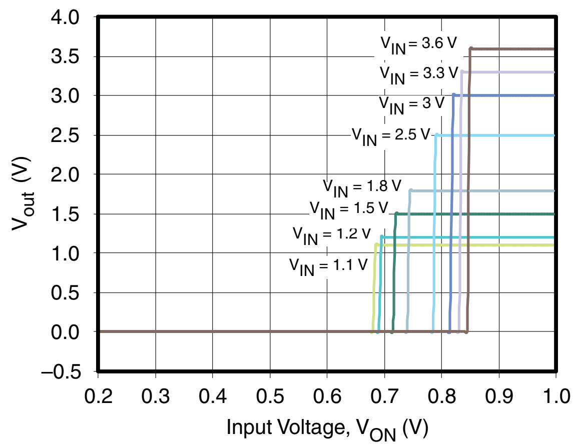
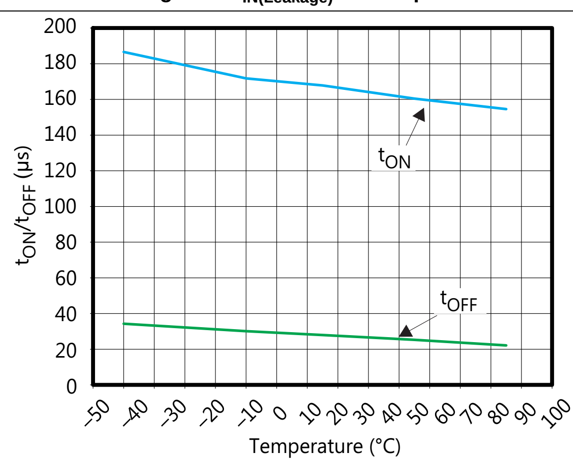
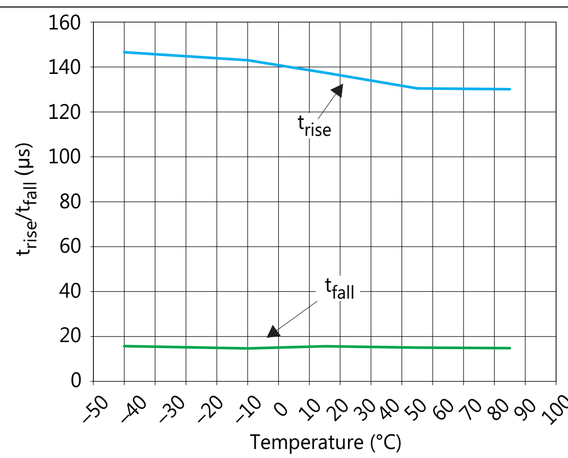


Figure 10. ON-Input Threshold



C_L = 0.1 µF, R_L = 500 Ω, V_{IN} = 3.3 V

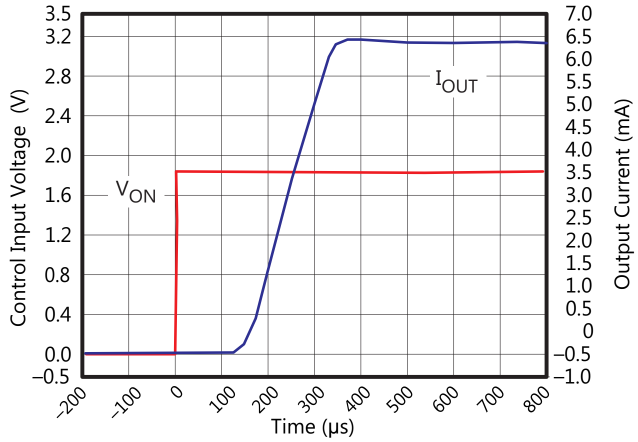
Figure 11. t_{ON}/t_{OFF} vs Temperature



C_L = 0.1 µF, R_L = 500 Ω, V_{IN} = 3.3 V

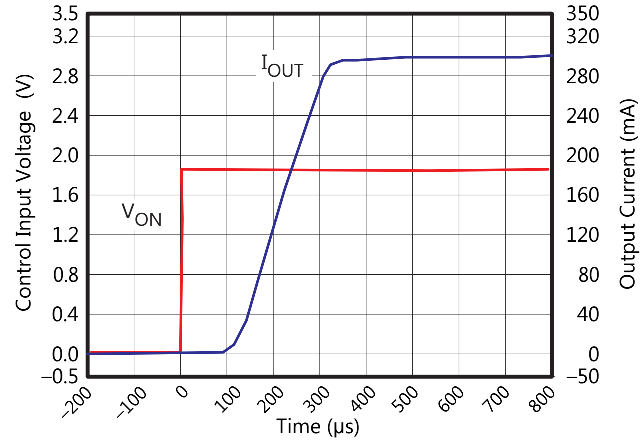
Figure 12. t_{rise}/t_{fall} vs Temperature

Typical Characteristics (continued)



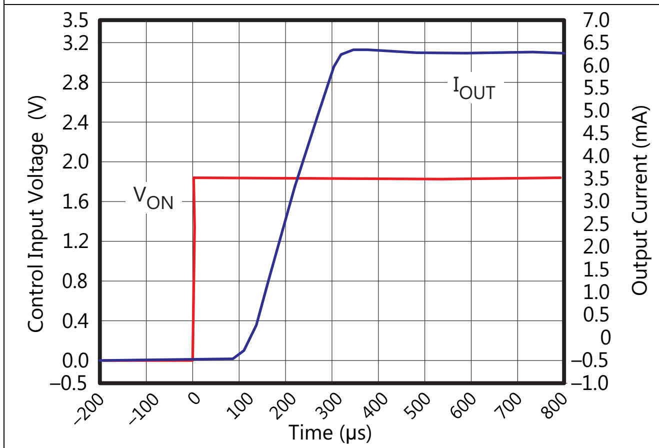
C_L = 3 µF, R_L = 500 Ω, V_{IN} = 3.3 V

Figure 13. t_{ON} Response



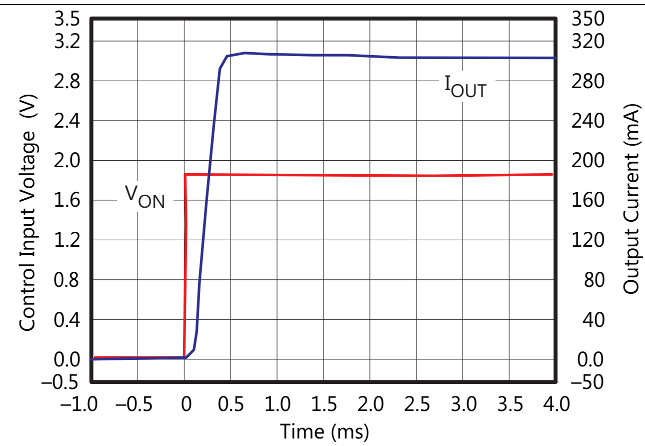
C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 3.3 V

Figure 14. t_{ON} Response



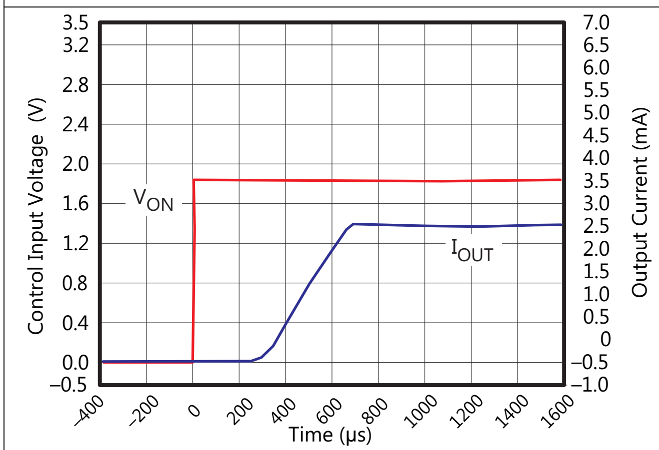
C_L = 3 µF, R_L = 500 Ω, V_{IN} = 3.3 V

Figure 15. t_{ON} Response



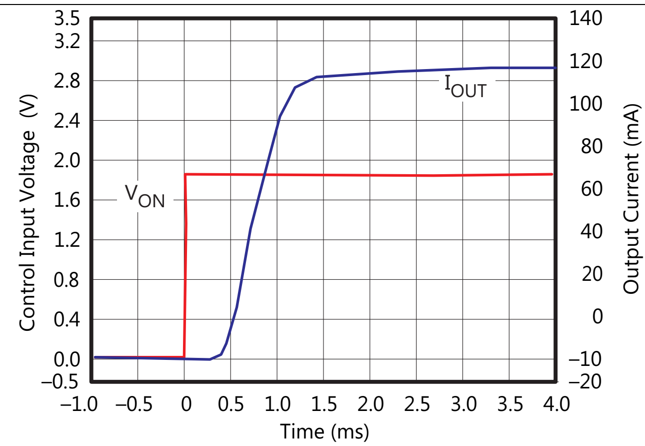
C_L = 3 µF, R_L = 10 Ω, V_{IN} = 3.3 V

Figure 16. t_{ON} Response



C_L = 0.1 µF, R_L = 500 Ω, V_{IN} = 1.2 V

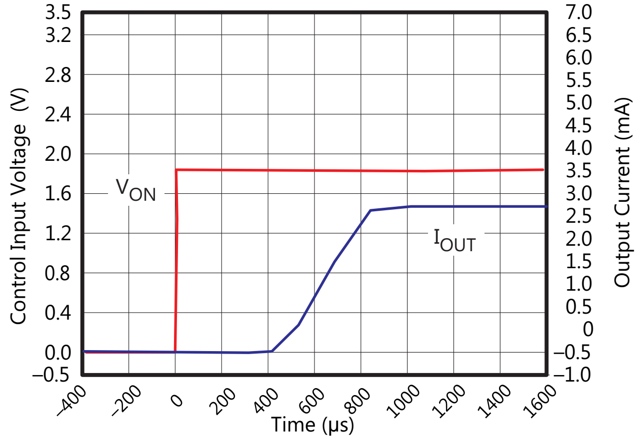
Figure 17. t_{ON} Response



C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 1.2 V

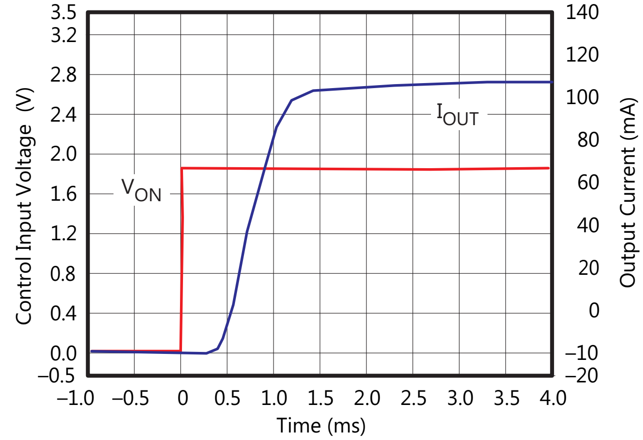
Figure 18. t_{ON} Response

Typical Characteristics (continued)



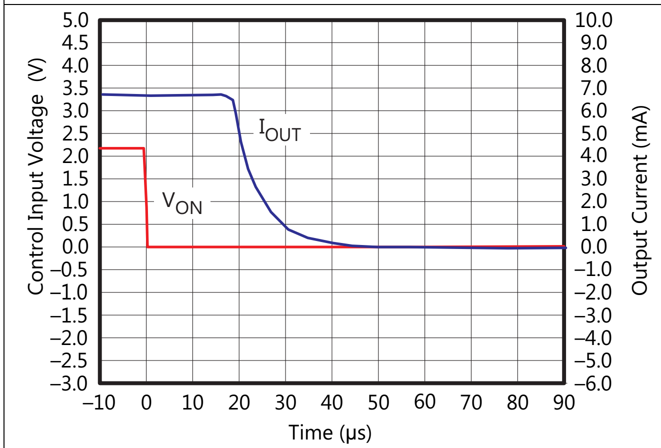
C_L = 3 µF, R_L = 500 Ω, V_{IN} = 1.2 V

Figure 19. t_{ON} Response



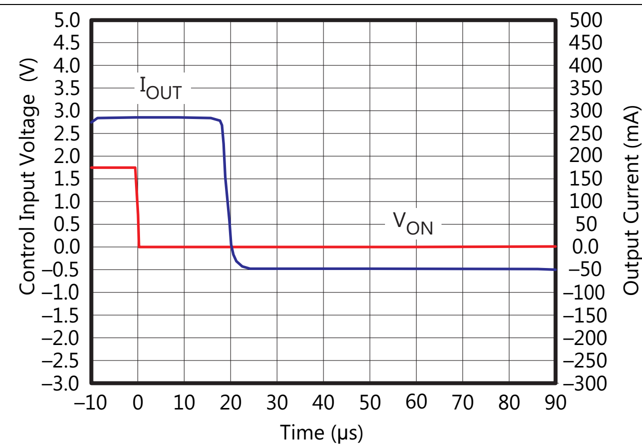
C_L = 3 µF, R_L = 10 Ω, V_{IN} = 1.2 V

Figure 20. t_{ON} Response



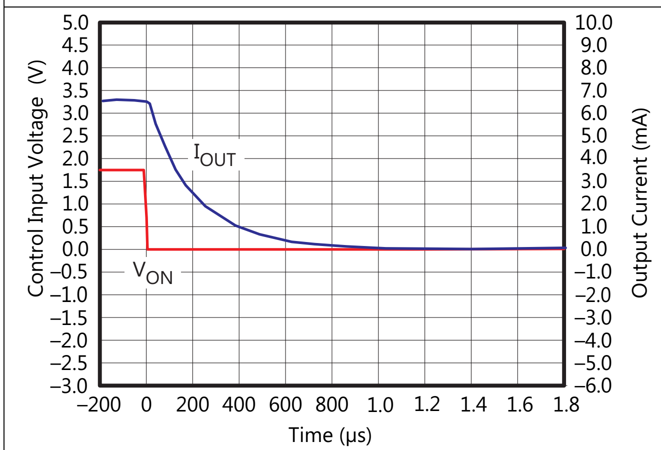
C_L = 0.1 µF, R_L = 500 Ω, V_{IN} = 3.3 V

Figure 21. t_{OFF} Response



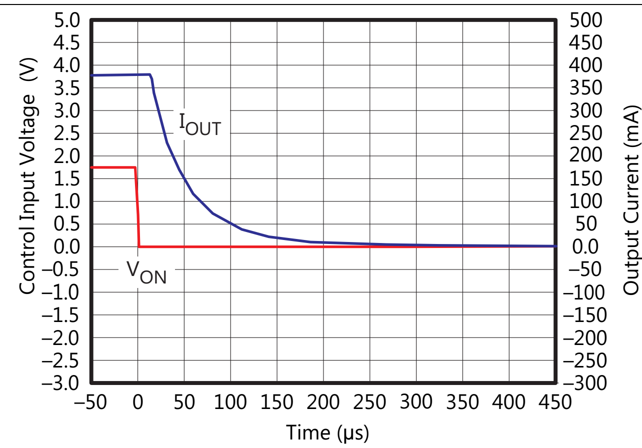
C_L = 0.1 µF, R_L = 11 Ω, V_{IN} = 3.3 V

Figure 22. t_{OFF} Response



C_L = 3 µF, R_L = 500 Ω, V_{IN} = 3.3 V

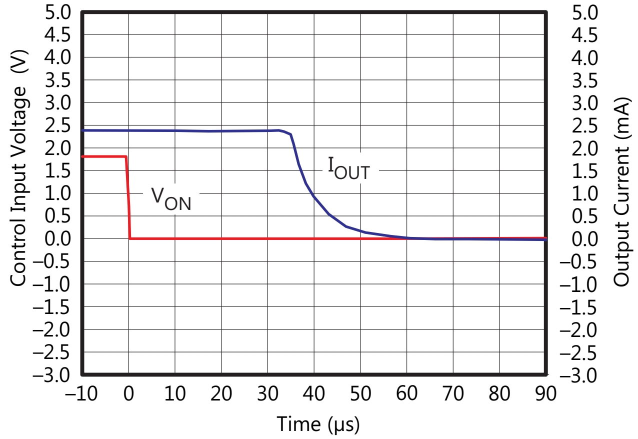
Figure 23. t_{OFF} Response



C_L = 3 µF, R_L = 11 Ω, V_{IN} = 3.3 V

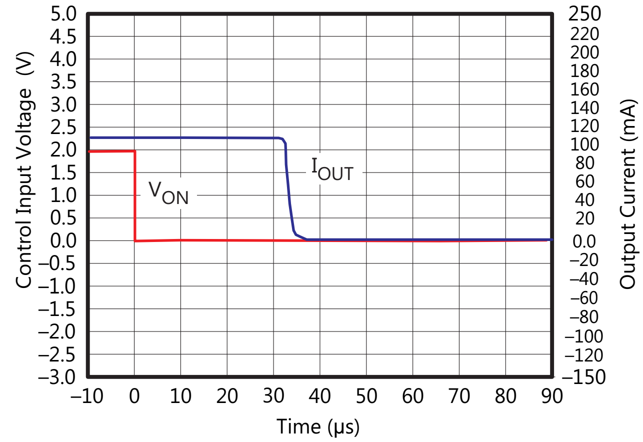
Figure 24. t_{OFF} Response

Typical Characteristics (continued)



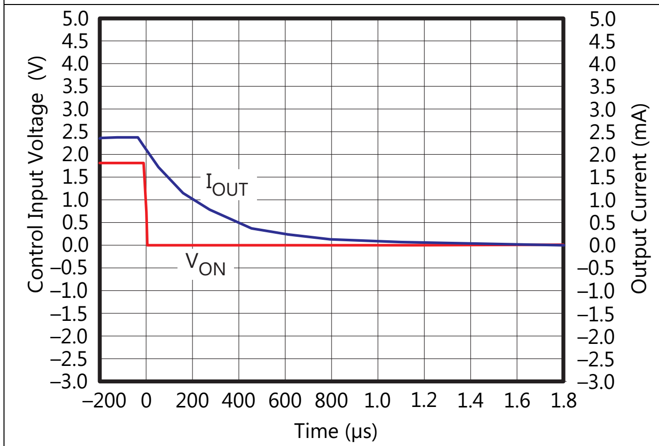
C_L = 0.1 µF, R_L = 500 Ω, V_{IN} = 1.2 V

Figure 25. t_{OFF} Response



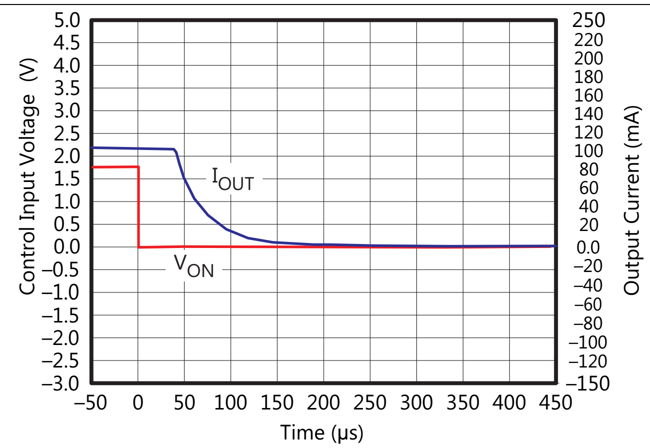
C_L = 0.1 µF, R_L = 11 Ω, V_{IN} = 1.2 V

Figure 26. t_{OFF} Response



C_L = 3 µF, R_L = 500 Ω, V_{IN} = 1.2 V

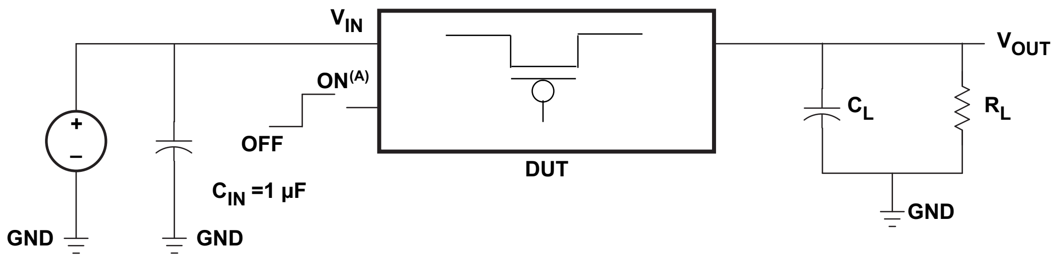
Figure 27. t_{OFF} Response



C_L = 3 µF, R_L = 11 Ω, V_{IN} = 1.2 V

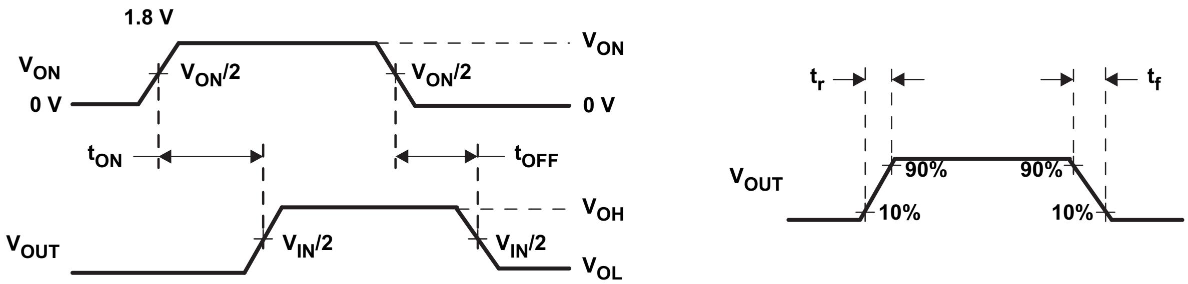
Figure 28. t_{OFF} Response

8 Parameter Measurement information



A. t_{rise} and t_{fall} of the control signal is 100 ns.

Figure 29. Test Circuit



A. t_{rise} and t_{fall} of the control signal is 100 ns.

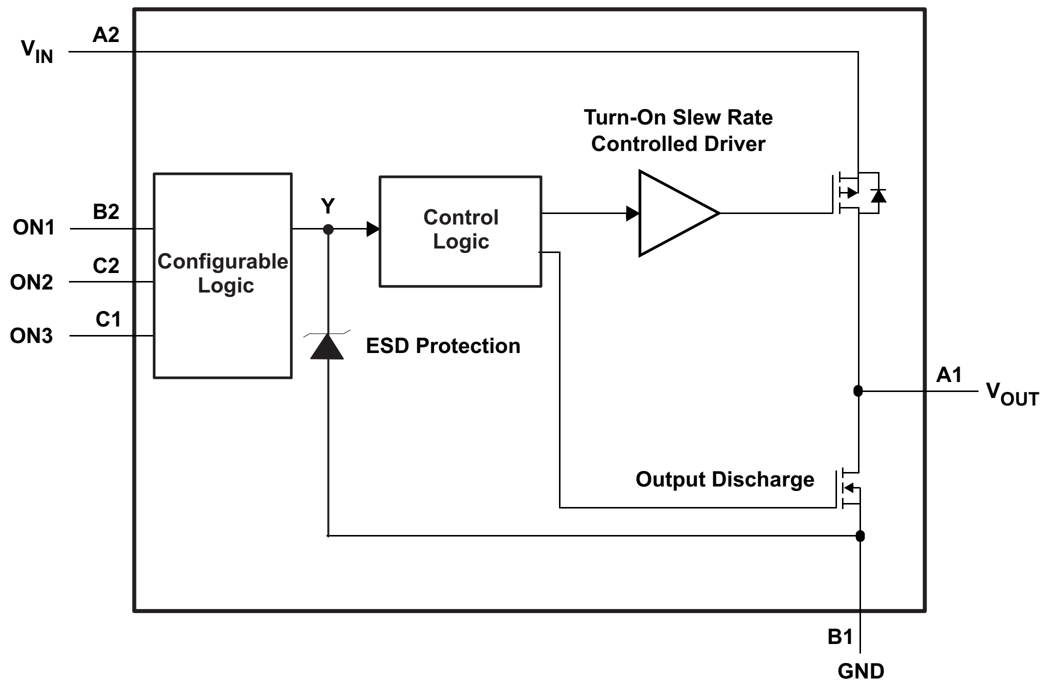
Figure 30. t_{ON}/t_{OFF} Waveforms

9 Detailed Description

9.1 Overview

TPS22932B is a single-channel, low r_{ON} load switch with controlled turnon. The device contains a low r_{ON} P-channel MOSFET that can operate over an input voltage range of 1.1 V to 3.6 V. The switch is controlled by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, and noninverter. All inputs can be connected to VIN or GND. The control pins can be connected to low-voltage GPIOs allowing it to be controlled by either 1.2-V, 1.8-V, 2.5-V, or 3.3-V logic signals while keeping extremely low quiescent current. A 120-Ω on-chip load resistor is available for output quick discharge when the switch is turned off. The rise time (slew rate) of the device is internally controlled to avoid inrush current.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Configurable Logic Function

The switch is controlled by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, and noninverter. All inputs can be connected to VIN or GND. The control pins can be connected to low-voltage GPIOs allowing it to be controlled by either 1.2-V, 1.8-V, 2.5-V, or 3.3-V logic signals while keeping extremely low quiescent current.

9.3.2 Quick Output Discharge

The TPS22932B includes the Quick Output Discharge (QOD) feature. When the switch is disabled, a discharge resistance with a typical value of 120 Ω is connected between the output and ground. This resistance pulls down the output and prevents it from floating when the device is disabled.

9.4 Device Functional Modes

9.4.1 Logic Configurations

Table 1. Configurable Logic Function Table

INPUTS			SWITCH CONTROL
ON3	ON2	ON1	Y
L	L	L	OFF
L	L	H	OFF
L	H	L	ON
L	H	H	ON
H	L	L	OFF
H	L	H	ON
H	H	L	OFF
H	H	H	ON

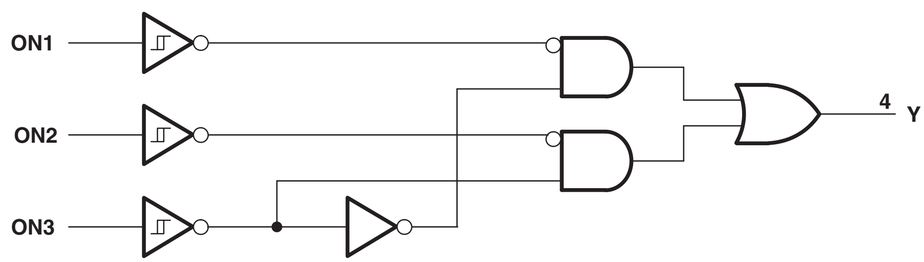


Figure 31. Logic Diagram (Positive Logic)

Table 2. Function Selection Table

LOGIC FUNCTION	FIGURE NO.
2-to-1 data selector	Figure 32
2-input AND gate	Figure 33
2-input OR gate with one inverted input	Figure 34
2-input NAND gate with one inverted input	Figure 34
2-input AND gate with one inverted input	Figure 35
2-input NOR gate with one inverted input	Figure 35
2-input OR gate	Figure 36
Inverter	Figure 37
Noninverted buffer	Figure 38

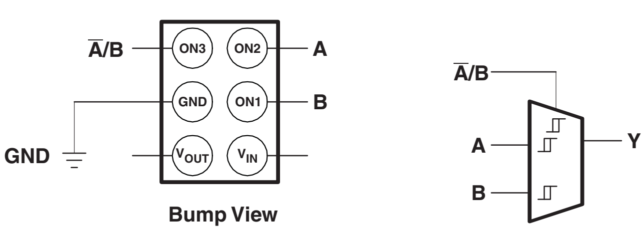


Figure 32. 2-to-1 Data Selector

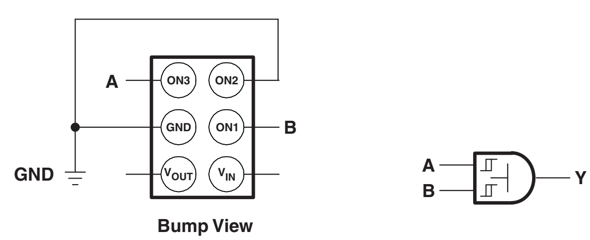


Figure 33. 2-Input AND Gate

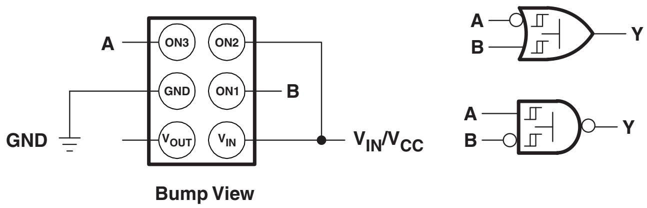


Figure 34. 2-Input OR Gate With One Inverted Input, 2-Input NAND Gate With One Inverted Input

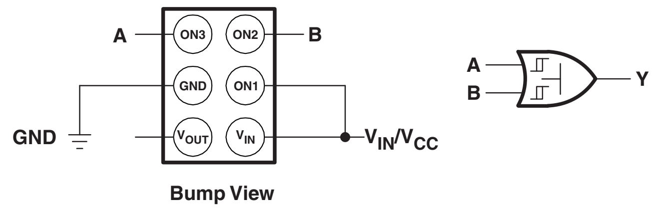


Figure 36. 2-Input OR Gate

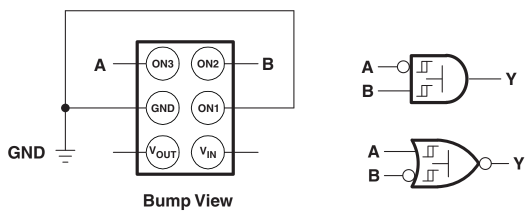


Figure 35. 2-Input AND Gate With One Inverted Input, 2-Input NOR Gate With One Inverted Input

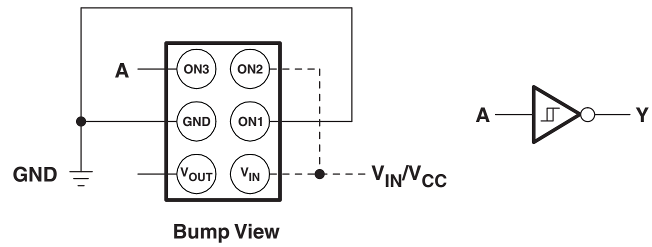


Figure 37. Inverter

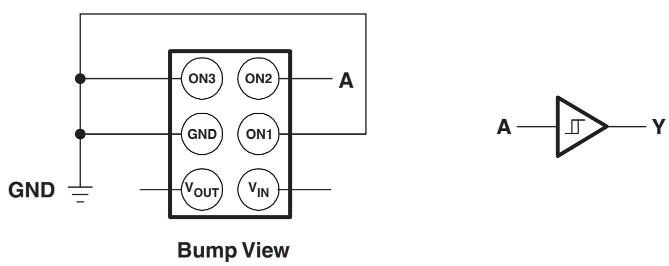


Figure 38. Noninverted Buffer

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 ON and OFF Control

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state so long as there is no fault. ON is active HI and has a low threshold making it capable of interfacing with low voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, or 3.3-V GPIOs.

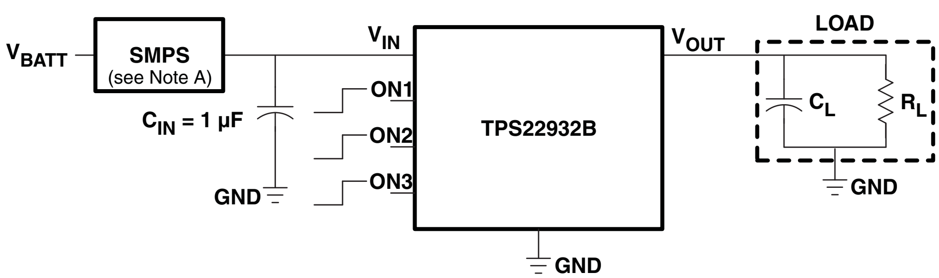
10.1.2 Input Capacitor

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor must be placed between V_{IN} and GND . A 1-µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during higher current application. When switching a heavy load, TI recommends to have an input capacitor about 10 or more times higher than the output capacitor to avoid any supply drop.

10.1.3 Output Capacitor

Due to the integral body diode in the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}.

10.2 Typical Application



A. Switched-mode power supply

Figure 39. Typical Application

10.2.1 Design Requirements

For this example, follow the design parameters listed in Table 3.

Table 3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
V_{IN}	3.3 V
C_L	4.7 µF
Maximum Acceptable Inrush Current	150 mA

10.2.2 Detailed Design Procedure

10.2.2.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the r_{ON} of the device and the load current. The r_{ON} of the device depends upon the VIN condition of the device. Refer to the r_{ON} specification of the device in the *Electrical Characteristics* table of this data sheet. When the r_{ON} of the device is determined based upon the VIN conditions, use Equation 1 to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times r_{ON}$$

where

- ΔV = Voltage drop from VIN to VOUT
- I_{LOAD} = Load current
- r_{ON} = ON-resistance of the device for a specific V_{IN}
- An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated. (1)

10.2.2.2 Managing Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0-V to V_{IN}. This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

$$\text{Inrush Current} = C \times \frac{dv}{dt}$$

where

- C = Output capacitance
- $\frac{dv}{dt} = \text{Output slew rate}$ (2)

The TPS22932B offers a very slow controlled rise time for minimizing inrush current. This device can be selected based upon the maximum acceptable slew rate which can be calculated using the design requirements and the inrush current equation. An output capacitance of 4.7 µF will be used because the amount of inrush increases with output capacitance:

$$150\ \text{mA} = 4.7\ \mu\text{F} \times \frac{dv}{dt} \quad (3)$$

$$\frac{dv}{dt} = 31.9\ \text{V/ms} \quad (4)$$

To ensure an inrush current of less than 150 mA, a device with a slew rate less than 31.9 V/ms must be used.

The TPS22932B has a typical rise time of 145 µs at 3.3 V. This results in a slew rate of 22.8 V/ms which meets the requirement.

10.2.3 Application Curve

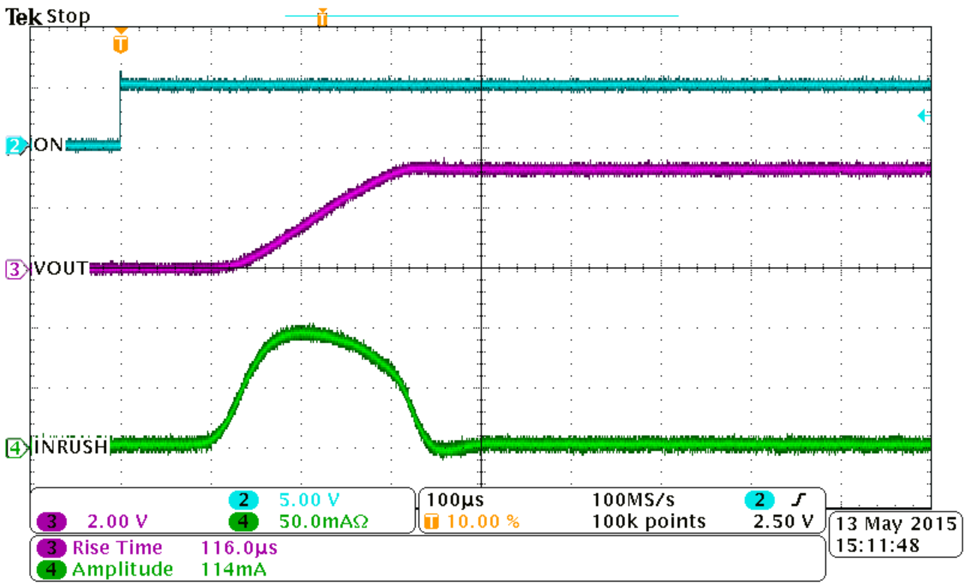


Figure 40. TPS22932B Inrush Current With 4.7-µF Output Capacitor

11 Power Supply Recommendations

The device is designed to operate with a V_{IN} range of 1.1 V to 3.6 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient.

12 Layout

12.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for V_{IN}, V_{OUT}, and GND will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

12.2 Layout Example

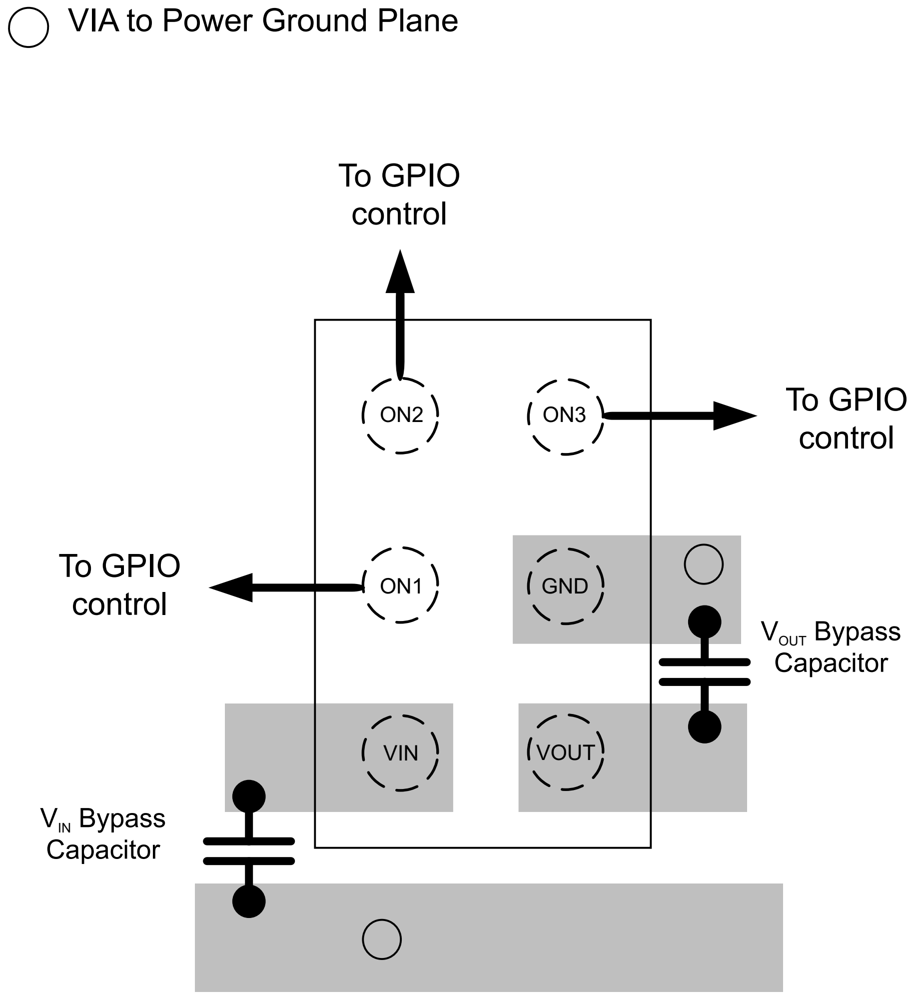


Figure 41. Layout Example

13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22932BYFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(483 ~ 485)	Samples
TPS22932BYFPT	ACTIVE	DSBGA	YFP	6	250	TBD	Call TI	Call TI	-40 to 85	483	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

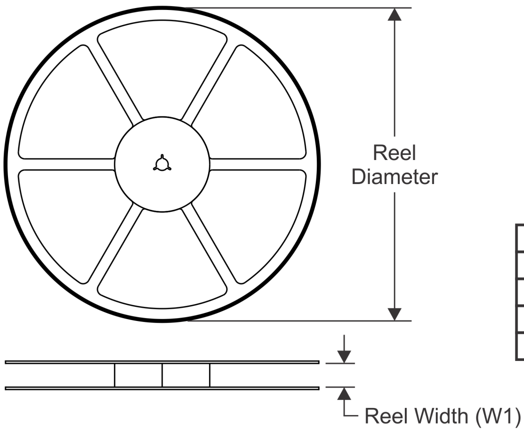
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

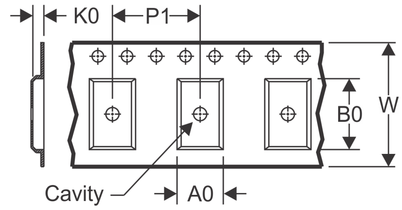
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

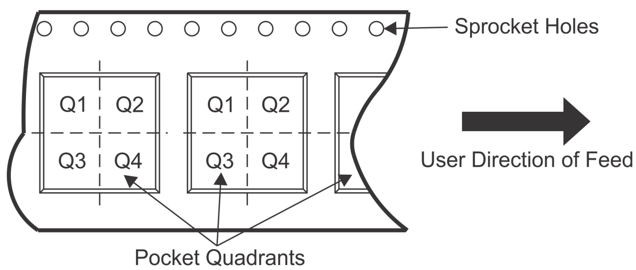


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

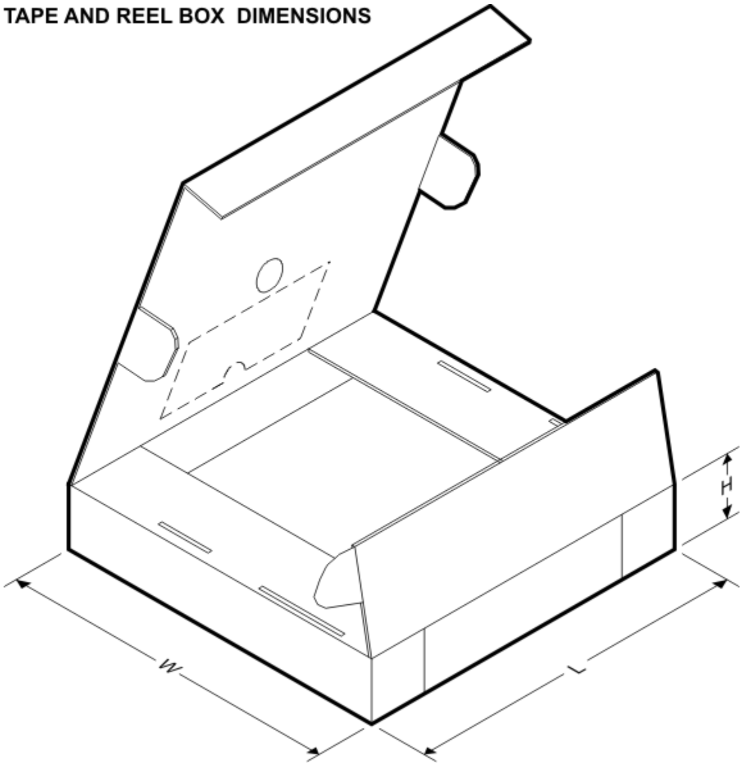
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22932BYFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



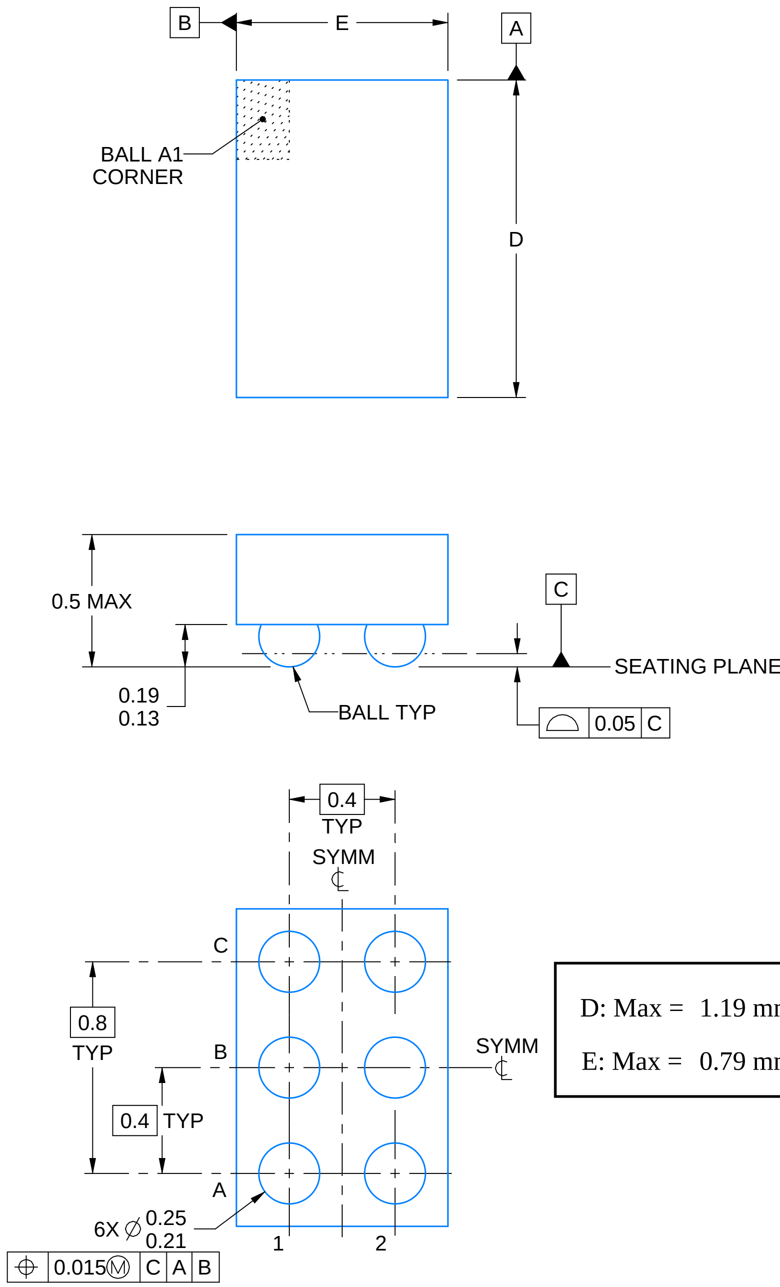
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22932BYFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



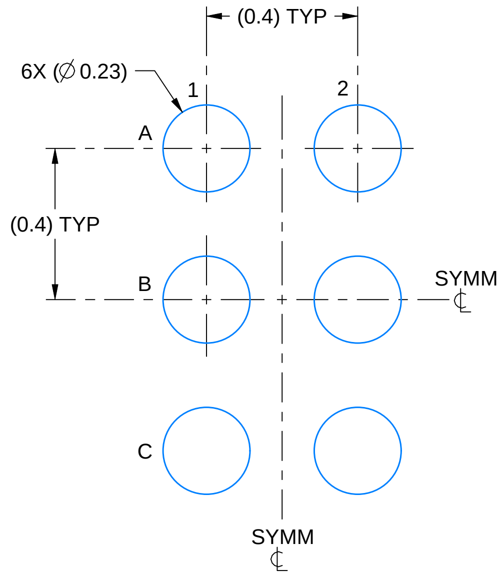
D: Max = 1.19 mm, Min = 1.13 mm

E: Max = 0.79 mm, Min = 0.73 mm

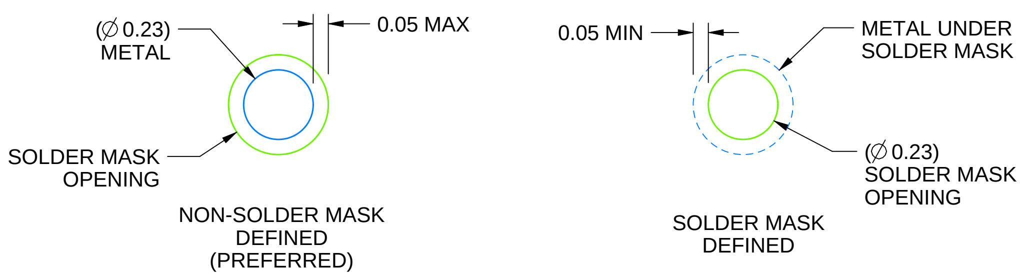
4223410/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:50X

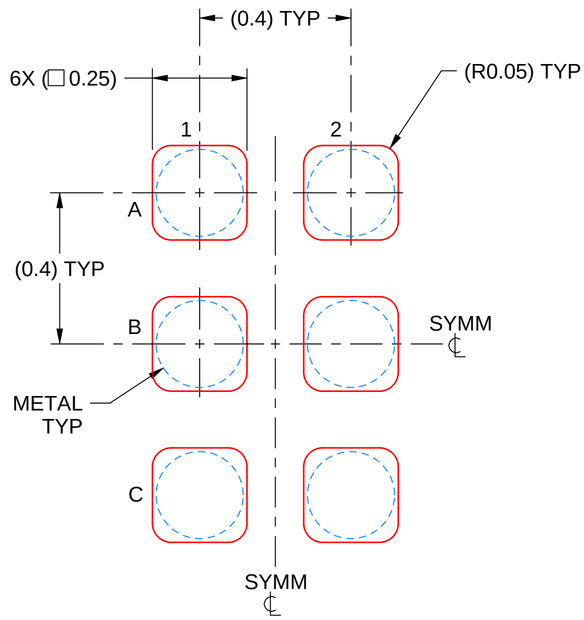


SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE AND DISCLAIMER

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265