N-Channel 25-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)[a, e]	Q_g (Typ)
25	0.0062 at V_{GS} = 10 V	78	20.5 nC
	0.010 at V_{GS} = 4.5 V	62	

FEATURES

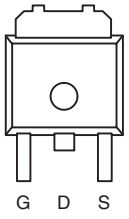
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- RoHS Compliant

RoHS COMPLIANT

APPLICATIONS

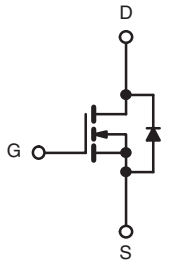
- DC/DC Conversion, Low-Side
  - Desktop PC

TO-252



Drain Connected to Tab

Top View



N-Channel MOSFET

Ordering Information: SUD50N025-06P-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	25	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)	T_C = 25 °C	I_D	78[a, e]	A
	T_C = 70 °C		65[a, e]	
	T_A = 25 °C		32[b, c]	
	T_A = 70 °C		25[b, c]	
Pulsed Drain Current		I_{DM}	100	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	43	
	T_A = 25 °C		7.1[b, c]	
Avalanche Current Pulse	L = 0.1 mH	I_{AS}	35	
Single Pulse Avalanche Energy		E_{AS}	61.25	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	65[a]	W
	T_C = 70 °C		45[a]	
	T_A = 25 °C		10.7[b, c]	
	T_A = 70 °C		7.5[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, d]	t ≤ 10 sec	R_{thJA}	11	14	°C/W
Maximum Junction-to-Case	Steady State	R_{thJC}	1.9	2.3	

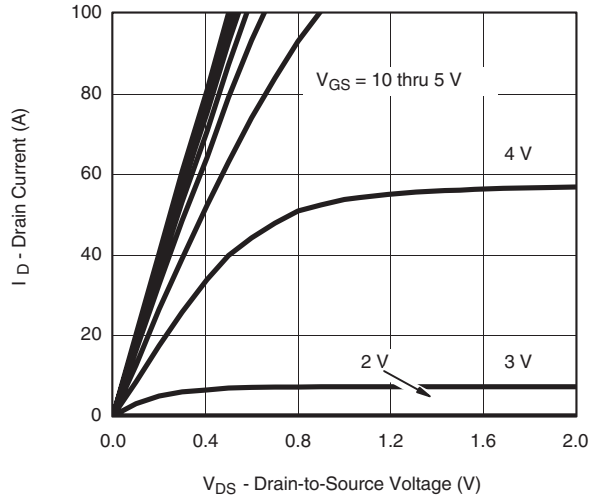
Notes:
a. Based on T_C = 25 °C.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 sec.
d. Maximum under Steady State conditions is 90 °C/W.
e. Calculated based on maximum junction temperature. Package limitation current is 50 A.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	25			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		20		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.4		2.4	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25 V, V_{GS} = 0 V			1	µA
		V_{DS} = 25 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	50			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		0.0051	0.0062	Ω
		V_{GS} = 4.5 V, I_D = 15 A		0.0081	0.010	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 15 A		55		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 12 V, V_{GS} = 0 V, f = 1 MHz		2490		pF
Output Capacitance	C_{oss}			530		
Reverse Transfer Capacitance	C_{rss}			280		
Total Gate Charge	Q_g	V_{DS} = 12 V, V_{GS} = 10 V, I_D = 50 A		44	66	nC
		V_{DS} = 12 V, V_{GS} = 4.5 V, I_D = 50 A		20.5	31	
Gate-Source Charge	Q_{gs}			7.5		
Gate-Drain Charge	Q_{gd}			7.0		
Gate Resistance	R_g	f = 1 MHz	0.55	1.1	1.65	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 12 V, R_L = 0.24 Ω $I_D \cong$ 50 A, V_{GEN} = 4.5 V, R_g = 1 Ω		19	28	ns
Rise Time	t_r			12	18	
Turn-Off Delay Time	$t_{d(off)}$			18	27	
Fall Time	t_f			7	11	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 12 V, R_L = 0.24 Ω $I_D \cong$ 50 A, V_{GEN} = 10 V, R_g = 1 Ω		9	14	
Rise Time	t_r			11	16.5	
Turn-Off Delay Time	$t_{d(off)}$			24	36	
Fall Time	t_f			8	12	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			43	A
Pulse Diode Forward Current[a]	I_{SM}				100	
Body Diode Voltage	V_{SD}	I_S = 30 A		0.9	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 20 A, di/dt = 100 A/µs, T_J = 25 °C		30	45	ns
Body Diode Reverse Recovery Charge	Q_{rr}			20	30	nC
Reverse Recovery Fall Time	t_a			13.5		ns
Reverse Recovery Rise Time	t_b			16.5		

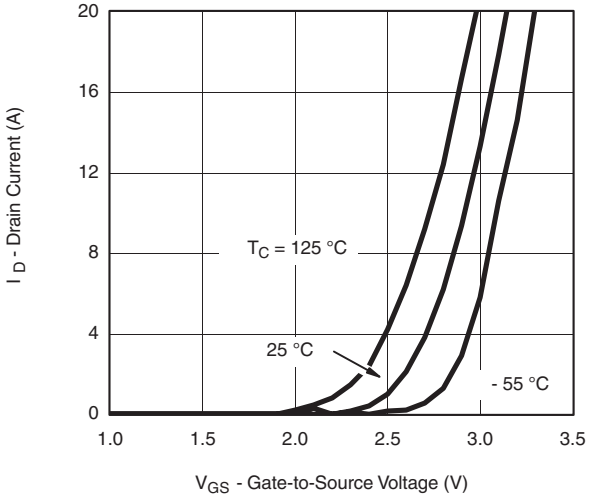
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

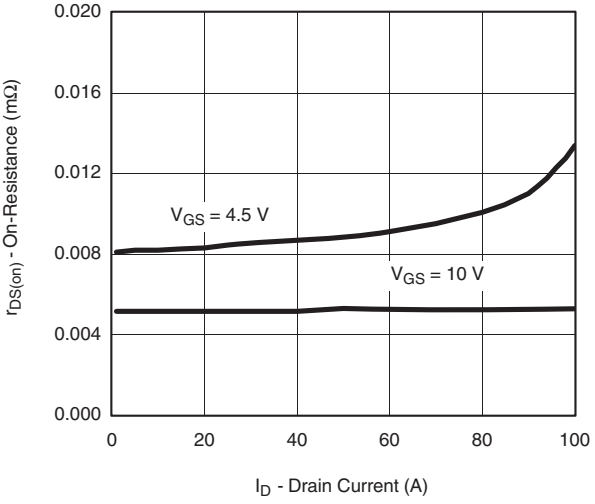
TYPICAL CHARACTERISTICS 25 °C unless noted



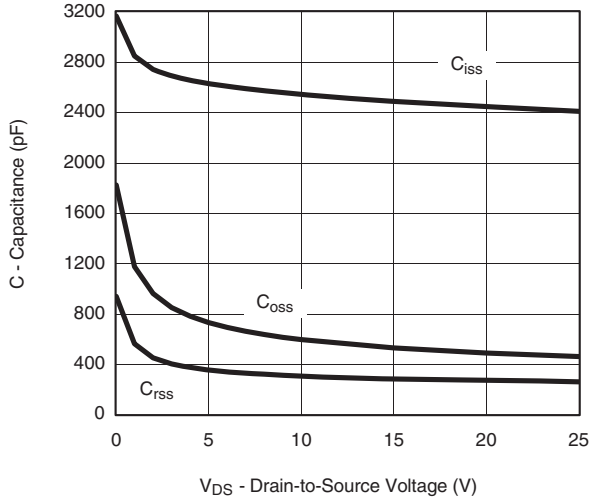
Output Characteristics



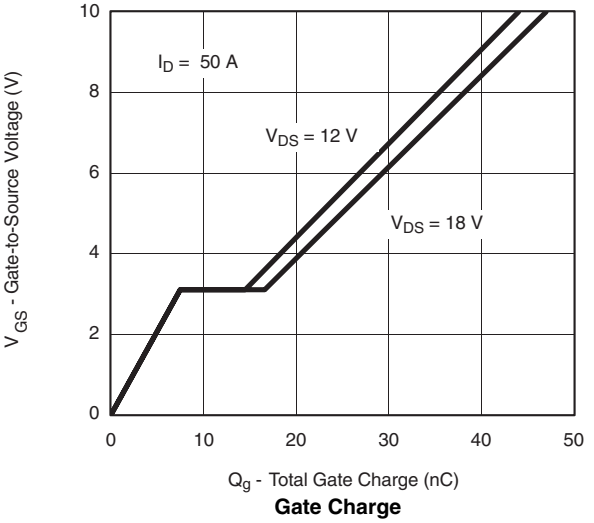
Transfer Characteristics



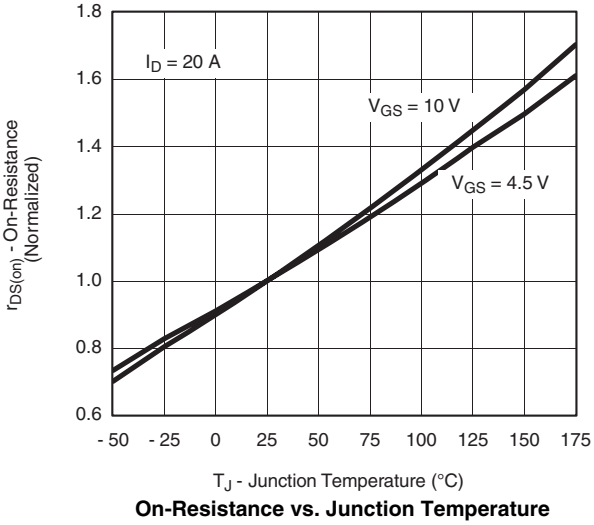
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

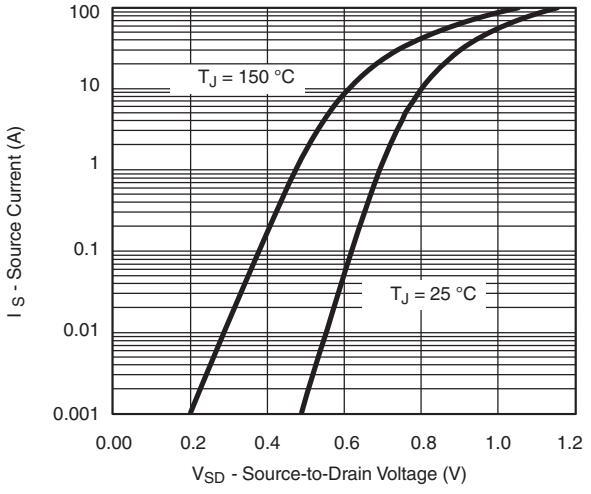


Gate Charge

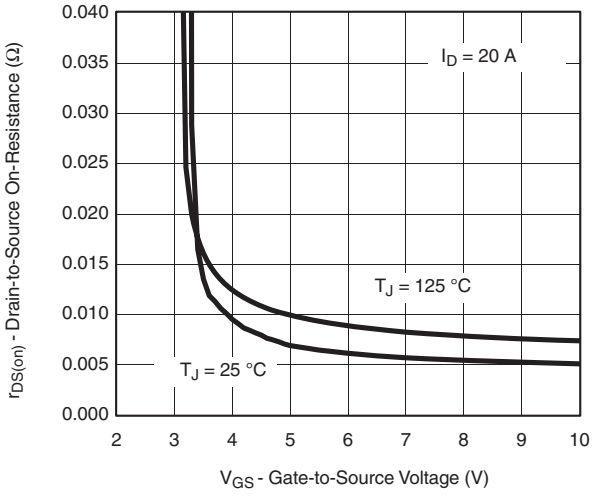


On-Resistance vs. Junction Temperature

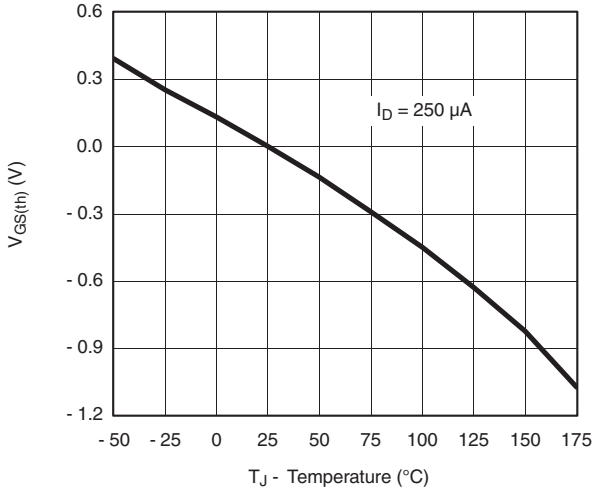
TYPICAL CHARACTERISTICS 25 °C unless noted



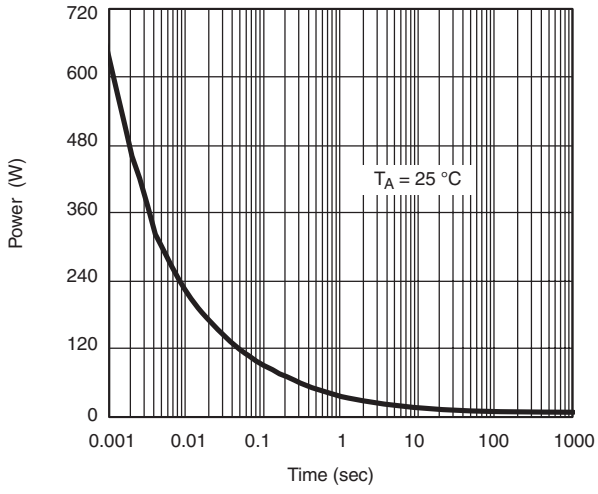
Source-Drain Diode Forward Voltage



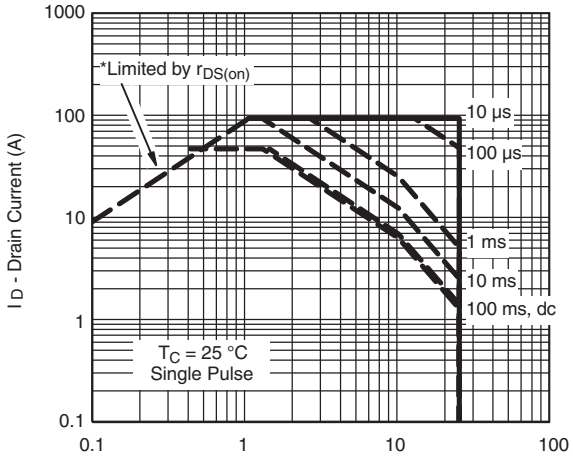
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



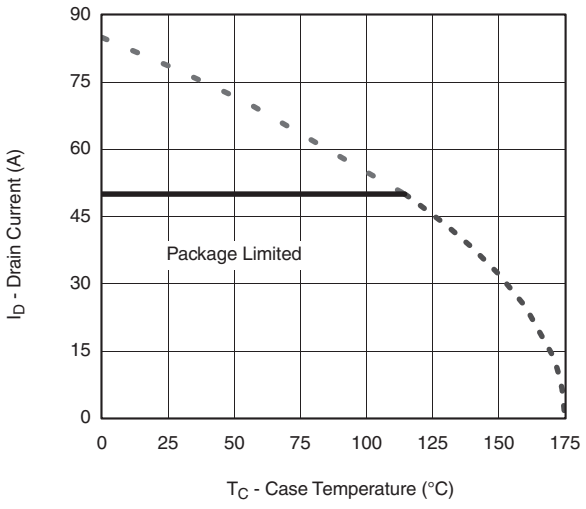
Single Pulse Power, Junction-to-Ambient



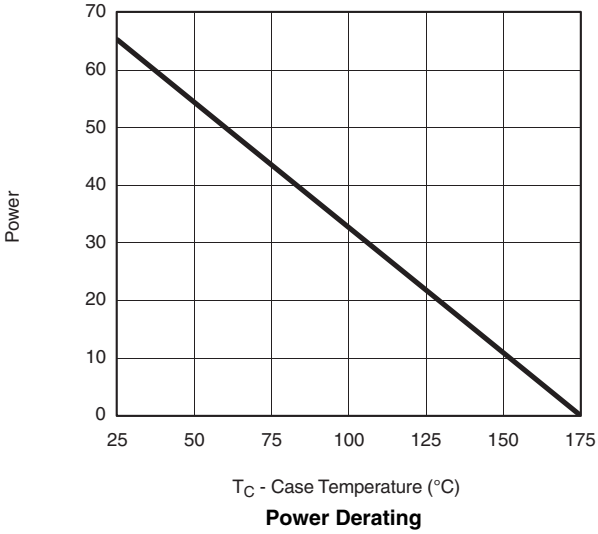
*V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

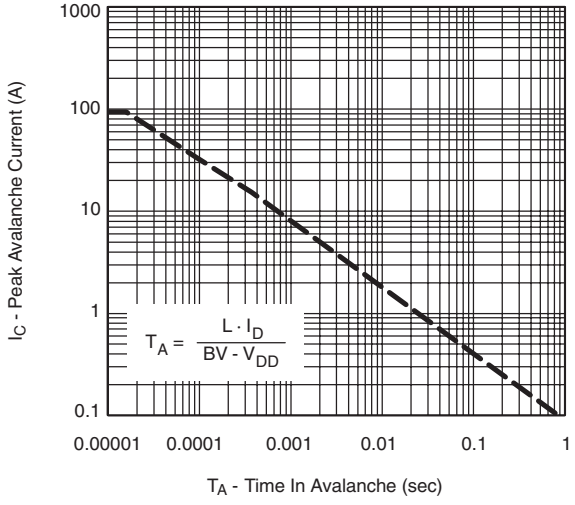
TYPICAL CHARACTERISTICS 25 °C unless noted



Current Derating*



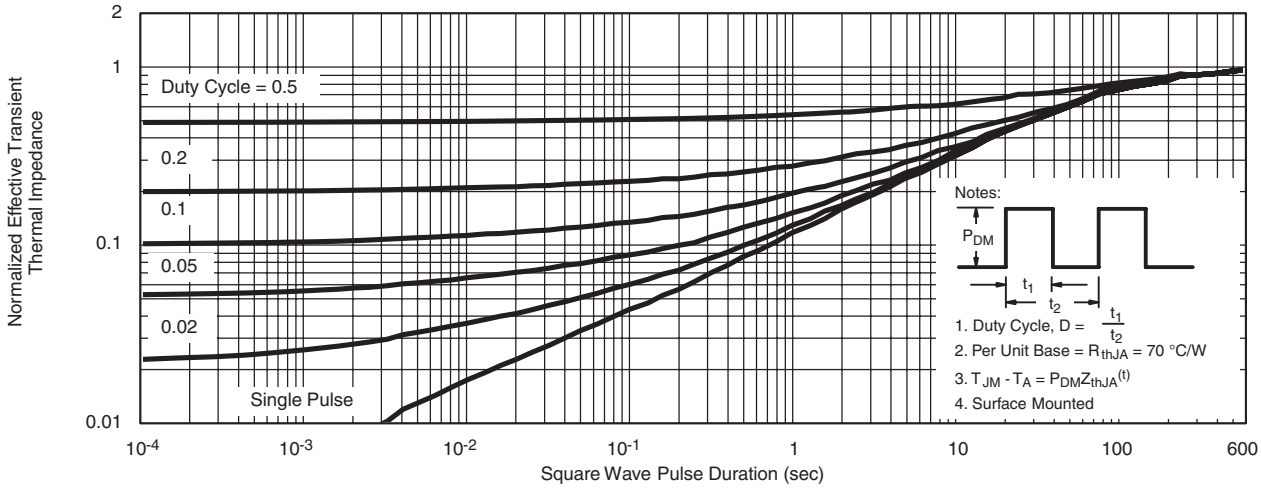
Power Derating



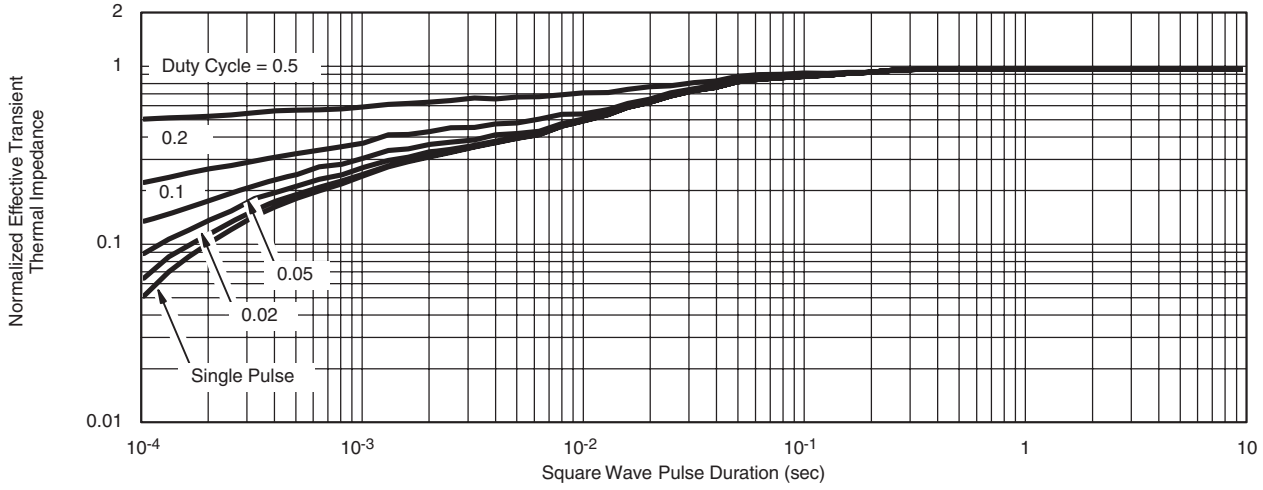
Single Pulse Avalanche Capability

*The power dissipation P_D is based on $T_{J(max)}$ = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C unless noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

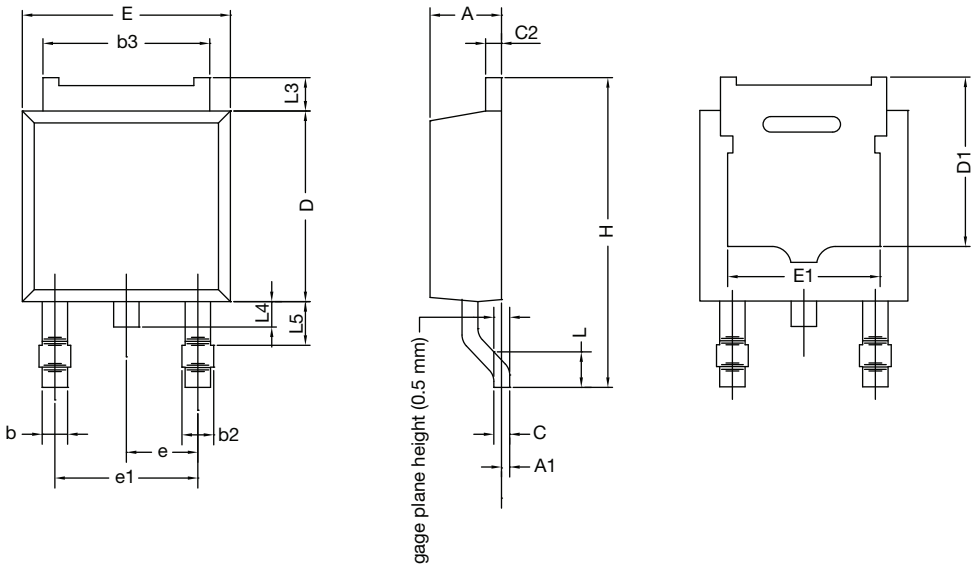


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?73349.

TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y

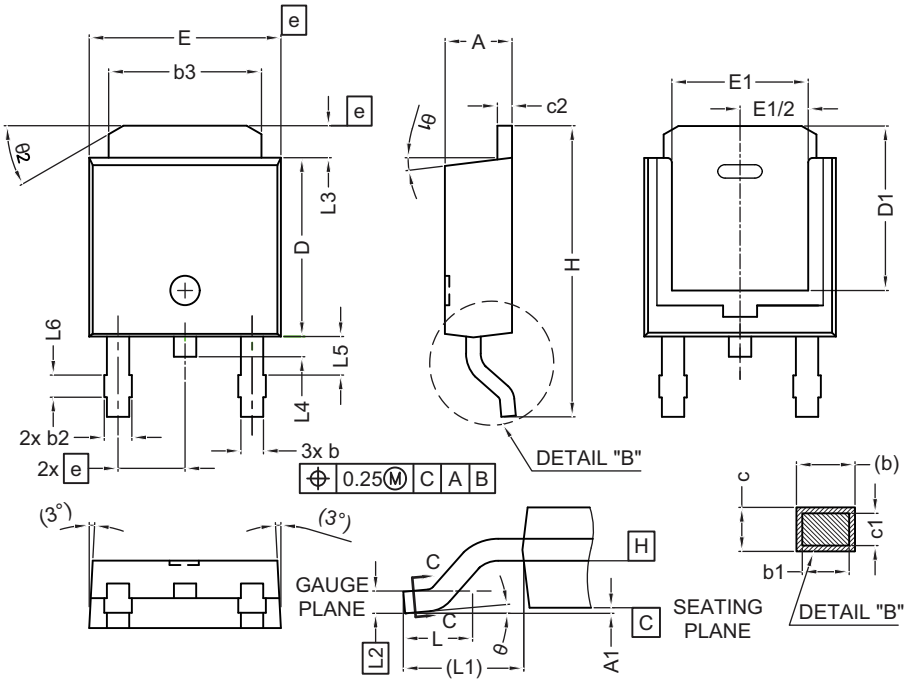


	MILLIMETERS	
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only

VERSION 2: FACILITY CODE = N



	MILLIMETERS	
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

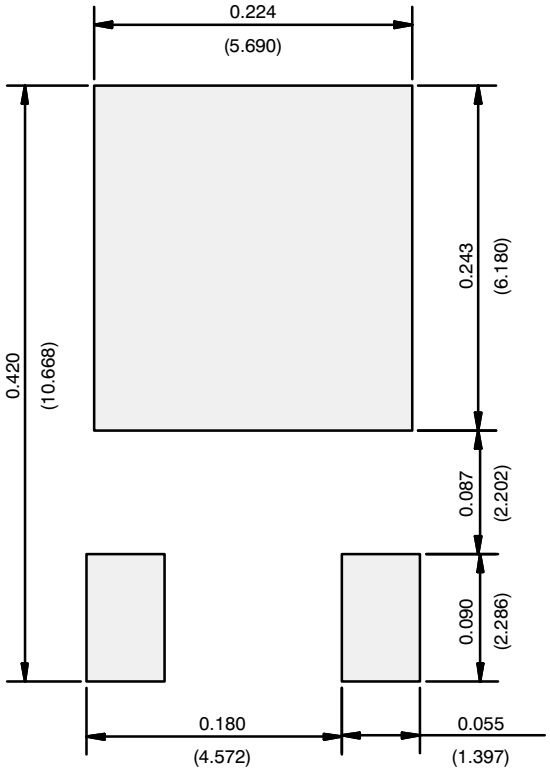
	MILLIMETERS	
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E19-0649-Rev. Q, 16-Dec-2019
DWG: 5347

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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