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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

August 2011

NC7SZ74
TinyLogic® UHS D-Type, Flip-Flop with Preset and Clear

Features

- Ultra-High Speed: t_{PD} 2.6ns (Typical) into 50pF at 5V V_{CC}
- High Output Drive: ±24mA at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Power Down High-Impedance Inputs/Outputs
- Over-Voltage Tolerance Inputs Facilitate 5V to 3V Translation
- Proprietary Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Package
- Space-Saving US8 Surface Mount Package

Description

The NC7SZ74 is a single, D-type, CMOS flip-flop with preset and clear from Fairchild's ultra high-speed series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive, while maintaining low static power dissipation over a very broad V_{CC} operating range of 1.65V to 5.5V V_{CC}. The inputs and outputs are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V, independent of V_{CC} operating voltage.

The signal level applied to the D input is transferred to the Q output during the positive-going transition of the CLK pulse.

Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SZ74K8X	SZ74	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide-	3000 Units on Tape & Reel
NC7SZ74L8X	N9	8-Lead MicroPak, 1.6 mm Wide	5000 Units on Tape & Reel

Connection Diagrams

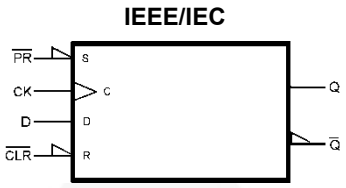


Figure 1. Logic Symbol

Pin Configurations

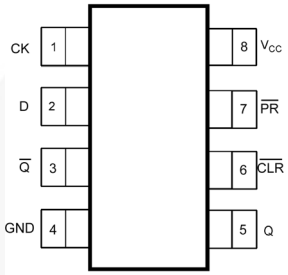


Figure 2. US8 (Top View)

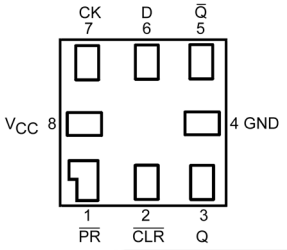


Figure 3. MicroPak™ (Top Through View)

Pin Definitions

Pin # US8	Pin # MicroPak	Name	Description
1	7	CK	Clock Pulse Input
2	6	D	Data Input
3	5	/Q	Flip-Flop Output
4	4	GND	Ground
5	3	Q	Flip-Flop Output
6	2	/CLR	Direct Clear Input
7	1	/PR	Direct Preset Input
8	8	V_{CC}	Supply Voltage

Function Table

Inputs				Output		Function
/CLR	/PR	D	CK	Q	/Q	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	
H	H	L	↑	L	H	
H	H	H	↑	H	L	
H	H	X	↓	Q_n	$/Q_n$	No Change

H = HIGH Logic Level Qn = No change in data X = Immaterial ↓= Falling Edge

L = LOW Logic Level Z = High Impedance ↑ = Rising Edge

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	7.0	V
V_{IN}	DC Input Voltage		-0.5	7.0	V
V_{OUT}	DC Output Voltage		-0.5	7.0	V
I_{IK}	DC Input Diode Current	V_{IN} < 0V		-50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0V		-50	mA
I_{OUT}	DC Output Source/Sink Current			±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current			±50	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)			+260	°C
P_D	Power Dissipation at +85°C			250	mW
ESD	Human Body Model, JEDEC:JESD22-A114			5000	V
	Charge Device Model: JEDEC:JESD22-C101			2000	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.50	5.50	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage	Active State	0	V_{CC}	V
		3-State	0	5.5	
t_r, t_f	Input Rise and Fall Times	V_{CC}=1.8V, 2.5V ± 0.2V	0	20	ns/V
		V_{CC}=3.3V ± 0.3V	0	10	
		V_{CC}=5.0V ± 0.5V	0	5	
T_A	Operating Temperature		-40	+85	°C
θ_{JA}	Thermal Resistance	US8		250	°C/W
		MicroPak™-8		280	

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=+25°C			T_A=-40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Control Input Voltage	1.65 to 1.95		$0.75V_{CC}$			$0.75V_{CC}$		V
		2.30 to 5.50		$0.70V_{CC}$			$0.70V_{CC}$		
V_{IL}	LOW Level Control Input Voltage	1.65 to 1.95				$0.25V_{CC}$		$0.25V_{CC}$	V
		2.30 to 5.50				$0.30V_{CC}$		$0.30V_{CC}$	
V_{OH}	HIGH Level Output Voltage	1.65	$V_{IN}=V_{IH}$, I_{OH}=-100µA	1.55	1.65		1.55		V
		2.30		2.20	2.30		2.20		
		3.00		2.90	3.00		2.90		
		4.50		4.40	4.50		4.40		
		1.65	I_{OH}=-4mA	1.29	1.52		1.29		
		2.30	I_{OH}=-8mA	1.90	2.15		1.90		
		3.00	I_{OH}=-16mA	2.40	2.80		2.40		
		3.00	I_{OH}=-24mA	2.30	2.68		2.30		
		4.50	I_{OH}=-32mA	3.80	4.20		3.80		
V_{OL}	LOW Level Control Output Voltage	1.65	$V_{IN}=V_{IH}$, I_{OL}=100µA			0.10		0.10	V
		2.30				0.10		0.10	
		3.00				0.10		0.10	
		4.50				0.10		0.10	
		1.65	I_{OL}=4mA		0.80	0.24		0.24	
		2.30	I_{OL}=8mA		0.10	0.30		0.30	
		3.00	I_{OL}=16mA		0.15	0.40		0.40	
		3.00	I_{OL}=24mA		0.22	0.55		0.55	
		4.50	I_{OL}=32mA		0.22	0.55		0.55	
I_{IN}	Input Leakage Current	0 to 5.5	$0 \le V_{IN} \le 5.5V$			±0.1		±1.0	µA
I_{OFF}	Power Off Leakage Current	0	V_{IN} or V_{OUT}=5.5V			1		10	µA
I_{CC}	Quiescent Supply Current	1.65 to 5.50	V_{IN}=5.5V, GND			1		10	µA

AC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=+25°C			T_A=-40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
f_{MAX}	Maximum Clock Frequency	1.80 ± 0.15	C_L=15pF R_D=1MΩ S_1=Open	75			75			Figure 4 Figure 8
		2.50 ± 0.20		150			150			
		3.30 ± 0.30		200			200			
		5.00 ± 0.50		250			250			
		3.30 ± 0.50	C_L=50pF R_D=500Ω, S_1=Open	175			175			
		5.00 ± 0.50		200			200			
t_{PLH}, t_{PHL}	Propagation Delay CK to Q, /Q	1.80 ± 0.15	C_L=15pF, R_D=1MΩ S_1=Open	2.5	6.5	12.5	2.5	13.0	ns	Figure 4 Figure 6
		2.50 ± 0.20		1.5	3.8	7.5	1.5	8.0		
		3.30 ± 0.30		1.0	2.8	6.5	1.0	7.0		
		5.00 ± 0.50		0.8	2.2	4.5	0.8	5.0		
		3.30 ± 0.30	C_L=50pF R_D=500Ω, S_1=Open	1.0	3.4	7.0	1.0	7.5		
		5.00 ± 0.50		1.0	2.6	5.0	1.0	5.5		
t_{PLH}, t_{PHL}	Propagation Delay /CLR, /PR to Q, /Q	1.80 ± 0.15	C_L=15pF, R_L=1MΩ S_1=Open	2.5	6.5	14.0	2.5	14.5	ns	Figure 4 Figure 6
		2.50 ± 0.20		1.5	3.8	9.0	1.5	9.5		
		3.30 ± 0.30		1.0	2.8	6.5	1.0	7.0		
		5.00 ± 0.50		0.8	2.2	5.0	0.8	5.5		
		3.30 ± 0.30	C_L=50pF, R_D=500Ω, S_1=Open	1.0	3.4	7.0	1.0	7.5		
		5.00± 0.50		1.0	2.6	5.0	1.0	5.5		
t_S	Setup Time CK to D	1.80 ± 0.15	C_L=15pF, R_L=1MΩ S_1=Open	6.5			6.5		ns	Figure 4 Figure 7
		2.50 ± 0.20		3.5			3.5			
		3.30 ± 0.30		2.0			2.0			
		5.00 ± 0.50		1.5			1.5			
		3.30 ± 0.30	C_L=50pF, R_D=500Ω, S_1=Open	2.0			2.0			
		5.00± 0.50		1.5			1.5			
t_H	Hold Time, CK to D	1.80 ± 0.15	C_L=15pF, R_L=1MΩ S_1=Open	0.5			0.5		ns	Figure 4 Figure 7
		2.50 ± 0.20		0.5			0.5			
		3.30 ± 0.30		0.5			0.5			
		5.00 ± 0.50		0.5			0.5			
		3.30 ± 0.30	C_L=50pF, R_D=500Ω, S_1=Open	0.5			0.5			
		5.00± 0.50		0.5			0.5			
t_W	Pulse Width, CK, /PR, /CLR	1.80 ± 0.15	C_L=15pF, R_L=1MΩ S_1=Open	6.0			6.0		ns	Figure 4 Figure 8
		2.50 ± 0.20		4.0			4.0			
		3.30 ± 0.30		3.0			3.0			
		5.00 ± 0.50		2.0			2.0			
		3.30 ± 0.30	C_L=50pF, R_D=500Ω, S_1=Open	3.0			3.0			
		5.00± 0.50		2.0			2.0			
t_{REC}	Recover Time /CLR, /PR to CK	1.80 ± 0.15	C_L=15pF, R_L=1MΩ S_1=Open	8.0			8.0		ns	Figure 4 Figure 7
		2.50 ± 0.20		4.5			4.5			
		3.30 ± 0.30		3.0			3.0			
		5.00 ± 0.50		3.0			3.0			
		3.30 ± 0.30	C_L=50pF, R_D=500Ω, S_1=Open	3.0			3.0			
		5.00 ± 0.50		3.0			3.0			

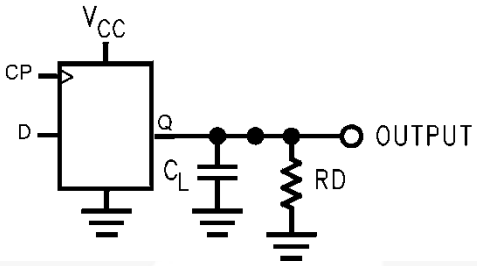
Continued on the following page…

AC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=+25°C			T_A=-40 to +85°C		Units	Figure
				Min.	Typ.	Min.	Typ.	Min.		
C_{IN}	Input Capacitance	0			3				pF	
C_{OUT}	Output Capacitance	0			4				pF	
C_{PD}	Power Dissipation Capacitance[2]	3.30			10				pF	
		5.00			12					

Note:

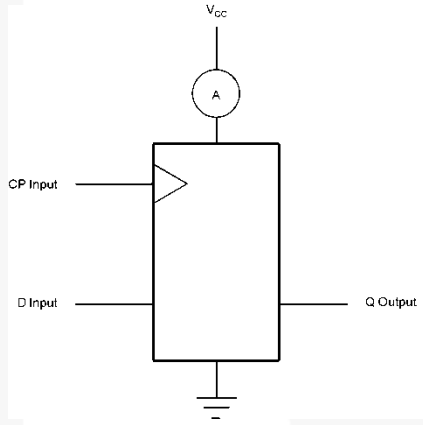
2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD}=(C_{PD})(V_{CC})(f_{IN})+(I_{CC}static)$.



Note:

3. C_L includes load and stray capacitance. Input PRR=1.0MHz t_w=500ns.

Figure 4. AC Test Circuit



Notes:

4. CP input=AC Waveforms t_r=t_f=2.5ns.
5. CP input PRR=10MHz; Duty Cycle=50%.
6. D input PRR=5MHz; Duty Cycle=50%.

Figure 5. I_{CCD} Test Circuit

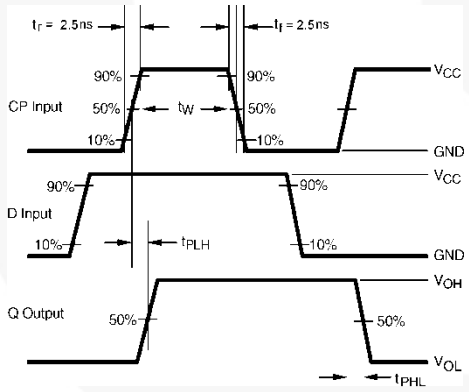


Figure 6. AC Waveforms

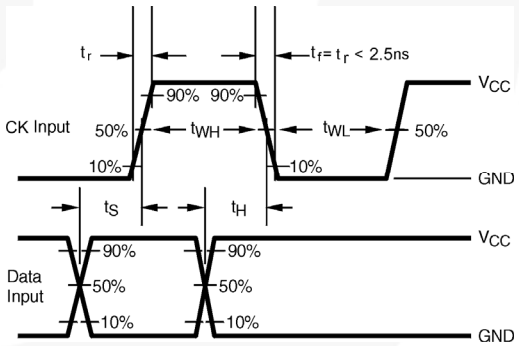


Figure 7. AC Waveforms

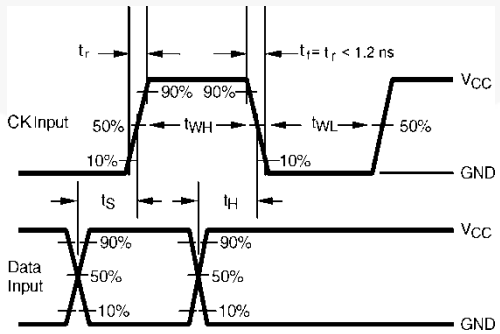


Figure 8. AC Waveforms

Physical Dimensions

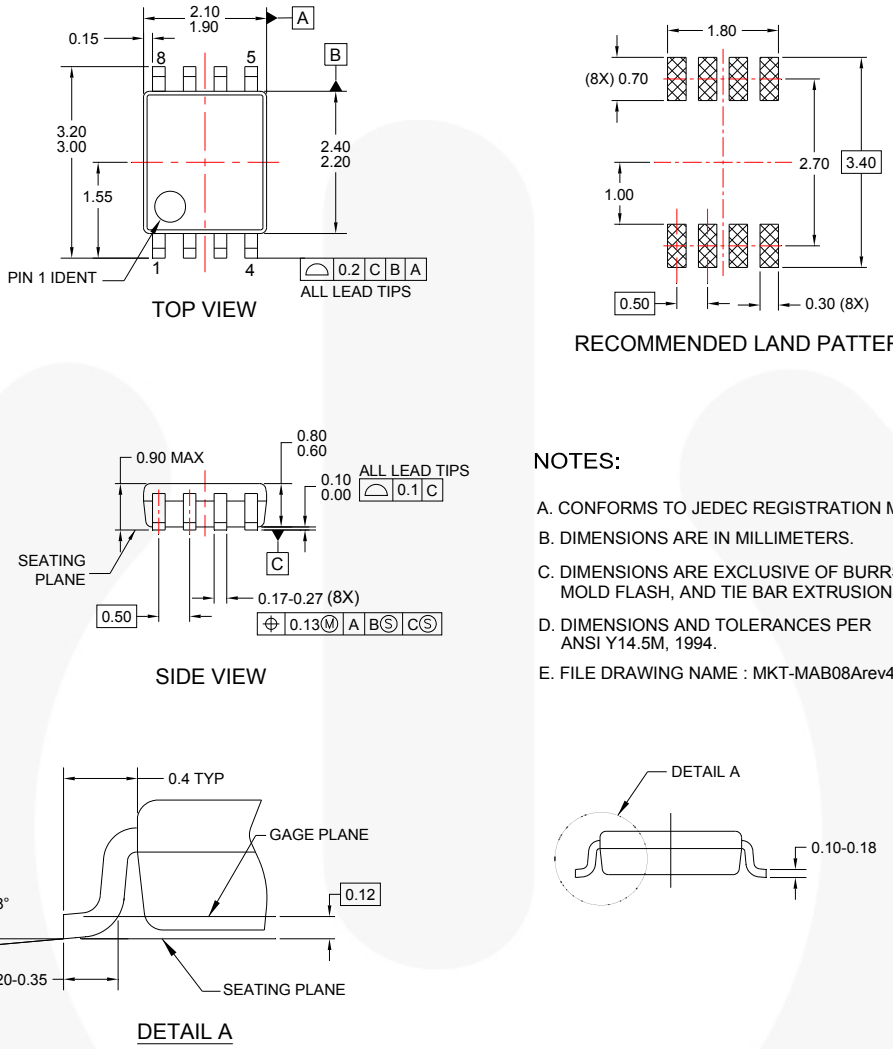


Figure 9. 8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide

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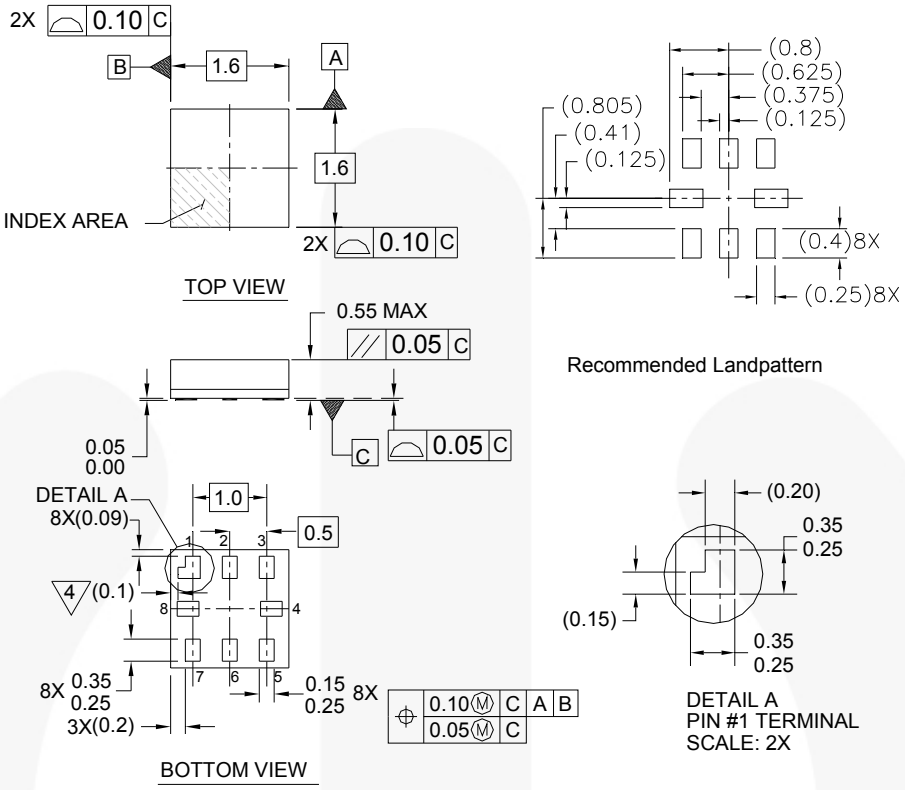
Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/analog/pdf/sc70-5_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
K8X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET
5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

Figure 10.8-Lead, MicroPak™, 1.6mm Wide

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L8X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I56

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