SP4T SWITCH WITH IMPEDANCE DETECTION MICRO-USB SWITCH TO SUPPORT USB, UART, AUDIO, AND VIDEO

Check for Samples: TSU6712

FEATURES

- **Detection is Compatible to CEA-936A (4-Wire Protocol, UART Interface)**
- **USB Path Supports USB 2.0 High Speed**
- **Support Control Signals (USB, UART JIG) Used in Manufacturing (JIG, BOOT)**
- **Interrupt for Attach and Detach Accessory**
- **Compatible Accessories**
  - **USB Cable, UART Cable, TV Out Cable**
  - **Mono, Stereo Headset**
  - **Remote Controller for DMB**
  - **Charging + TV Out**
  - **Charging + Stereo Headset**
- **ESD Performance Tested Per JESD 22**
  - **1500-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **ESD Performance DP/DM/ID/VBUS to GND**
  - **±6-kV Contact Discharge (IEC 61000-4-2)**

APPLICATIONS

- **Cell Phones & Smart Phones**
- **Tablet PCs**
- **Digital Cameras & Camcorders**
- **GPS Navigation Systems**
- **Micro USB interface with USB/UART/Audio/Video**

RVC PACKAGE
(TOP VIEW)

	1	2	3	4	5
A	INTB	VDDIO	ISET	OUT	VBUS
B	D +	SDA	S_L	MIC	DM
C	D -	SCL	V_L	S_R	DP
D	VBAT	IDBP	V_R	VIDEO	ID
E	RxD	TxD	BOOT	JIG	GND

DESCRIPTION

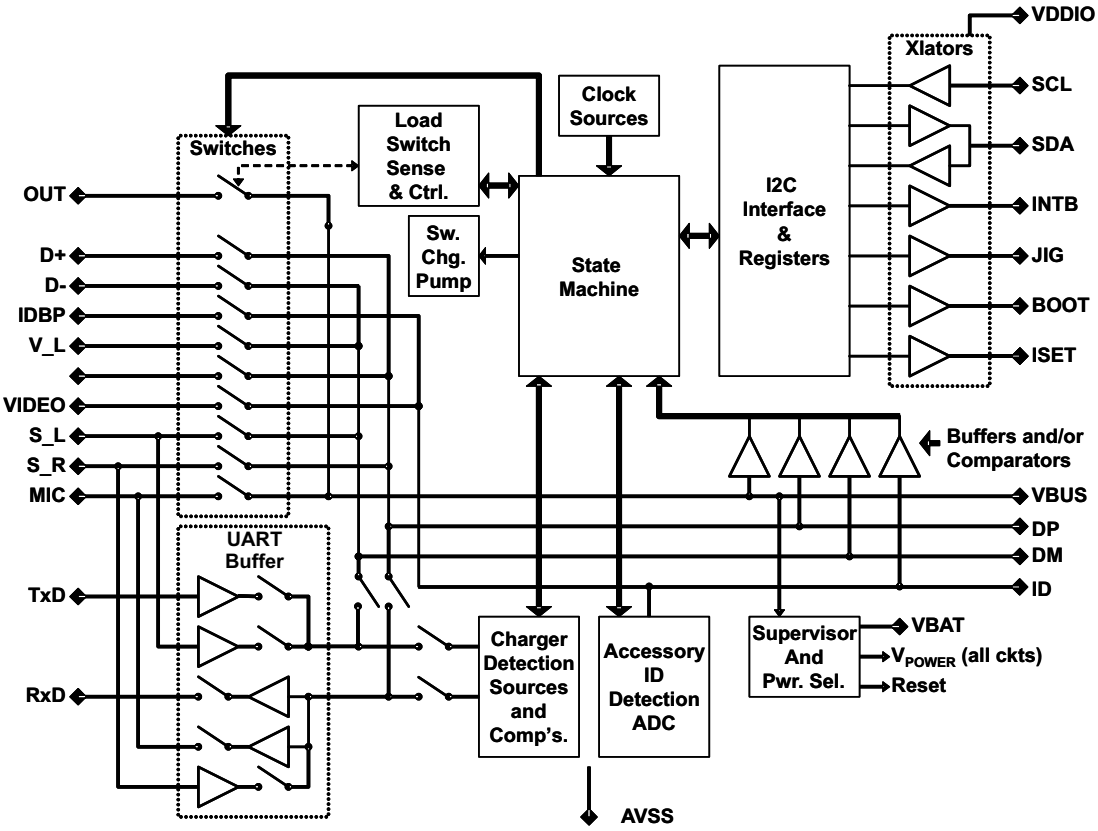
The TSU6712 is a multiple SP4T switch with impedance detection. The switch features impedance detection, which supports the detection of various accessories that are attached through DP and DM. The detection is based on the impedance values of the accessories as defined in Table 1. The TSU6712 is fully controlled using I^2C and enables USB data, stereo and mono audio, video, microphone, and UART data to use a common connector port.

Power for this device is supplied through VBAT of the system or through VBUS when attached. The switch can be controlled through I^2C. JIG and BOOT pins are used when a USB, UART JIG cable is used to test during development and manufacturing.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com

APPLICATION BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
Ball NO.	NAME		
D1	VBAT	–	3.0 – 4.4V Battery supply voltage
A2	VDDIO	–	1.8 ~ 3.3V Logic Supply
A5	VBUS	I	USB connector VBUS
A4	OUT	O	Phone charger output
E5	GND	–	Ground
B1	D +	I/O	USB data +
C1	D -	I/O	USB data -
D2	IDBP	I/O	USB ID data
E1	RxD	I/O	UART receive data
E2	TxD	I/O	UART transmit data
D3	V_R	I/O	TV-out right sound
C3	V_L	I/O	TV-out left sound
D4	VIDEO	I/O	TV-out encoded video
B4	MIC	I/O	Microphone signal
C4	S_R	I/O	Stereo headset right sound
B3	S_L	I/O	Mono or stereo headset left sound
C2	SCL	I	I2C clock
B2	SDA	I/O	I2C data
C5	DP	I/O	Common I/O port
B5	DM	I/O	Common I/O port
D5	ID	I/O	Common I/O port
A1	INTB	O	Processor interrupt signal when peripheral is plugged/unplugged. Push-pull output
A3	ISET	O	Fast-mode charger output. Open-drain output
E4	JIG	O	GPIO factory output. Open-drain output
E3	BOOT	O	GPIO factory output. Push-pull output

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{BUS}	Supply voltage from USB connector		–0.5	28	V
V_{BAT}	Supply voltage from battery		-0.5	6	
V_{DDIO}	Logic supply voltage		-0.5	4.6	V
OUT	Phone charger output		-0.5	7	V
V_{AUDIO}	Switch I/O voltage range	Audio Switch	-1.5	V_{BAT}+0.5	V
V_{MICIO}		Mic Switch	-0.5	V_{BAT}+0.5	
$V_{VIDEOIO}$		Video Switch	-1	V_{BAT}+0.5	
V_{UARTIO}		UART Buffer	-0.5	4.6	
V_{USBIO}		USB Switch	-0.5	V_{BAT}+0.5	
V_{LOGIC}	Voltage applied to logic output (SCL, SDA, INTB, ISET, BOOT, JIG)		-0.5	4.6	V
I_{BUS}	Peak input current on V_{BUS} pin			2	A
I_{OUT}	Peak output current on OUT pin			2	A
I_K	Analog port diode current		-50	50	mA
I_{SW-DC}	ON-state continuous switch current		-60	60	mA
$I_{SW-PEAK}$	ON-state peak switch current		-150	150	mA
I_{IK}	Digital logic input clamp current	V_L < 0		-50	mA
I_{LOGIC_O}	Continuous current through logic output		-50	50	mA
I_{GND}	Continuous current through GND			100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

THERMAL IMPEDANCE RATINGS

				UNIT
θ_{JA}	Package thermal impedance	YFP package	98.8	°C/W

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

Condition	Min	Max	Units
V_{BUS}	4.0	6.5	V
V_{BAT}	3.0	4.4	V
V_{DDIO}	1.8	3.3	V
USB_I/O	0	3.6	V
UART_I/O	0	2.7	V
Video_I/O	-0.5	2	V
Audio_I/O	-0.8	0.8	V
MIC_I/O	0	2.3	V
Temperature	-40	85	˚C

DIGITAL SIGNALS – I²C INTERFACE AND GPIO

over operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS	MIN	MAX	UNIT
V_{DDIO}	Logic and I/O supply voltage		1.65	3.6	V
V_{IH}	High-level input voltage		V_{DDIO} × 0.7	V_{DDIO}	V
V_{IL}	Low-level input voltage		0	V_{DDIO} × 0.3	V
V_{OH}	High-level output voltage	I_{OH} = -3 mA	V_{DDIO} × 0.7		V
V_{OL}	Low-level output voltage	I_{OL} = 3 mA	0	0.4	V
f_{SCL}	SCL frequency			400	kHz

UART BUFFER

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
From Phone Transmitter to Accessory					
V_{IH}	High-level input voltage (TxD)	V_{DDIO} = 2.8 V	1.15	V_{DDIO}	V
V_{IL}	Low-level input voltage (TxD)	V_{DDIO} = 2.8 V	0	0.49	V
V_{OH}	High-level output voltage (DP, DM)	I_{OH} = –4 mA , V_{BAT} = 3.0 V	2.4	V_{BAT}	V
V_{OL}	Low-level output voltage (DP, DM)	I_{OL} = 4 mA , V_{BAT} = 3.0 V	0	0.55	V
From Accessory to Phone Receiver					
V_{IH}	High-level input voltage (DP, DM)	V_{BAT} = 3.0 V	2.0	V_{BAT}	V
V_{IL}	Low-level input voltage (DP, DM)	V_{BAT} = 3.0 V	0	0.8	V
V_{OH}	High-level output voltage (RxD)	I_{OH} = –4 mA , V_{DDIO} = 2.8 V	1.16	V_{DDIO}	V
V_{OL}	Low-level output voltage (RxD)	I_{OL} = 4 mA , V_{DDIO} = 2.8 V	0	0.33	V

JIG AND ISET FAST-MODE CHARGER OUTPUT (OPEN-DRAIN OUTPUT)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = 10 mA, V_{BAT} = 3.0 V		0.5	V

INTB AND BOOT (PUSH-PULL OUTPUT)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA , V_{DDIO} = 2.8 V	2.2	V_{DDIO}	V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA , V_{DDIO} = 2.8 V	0	0.33	V

OVP ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
In							
Undervoltage lockout, input power detected threshold rising		V_{UVLO+}	V_{BUS} increasing from 0V to 5V, No load on OUT pin	2.65	2.8	3	V
Undervoltage lockout, input power detected threshold falling		$V_{UVLO–}$	V_{BUS} decreasing from 5V to 0V, No load on OUT pin	2.25	2.44	2.7	V
Hysteresis on UVLO		$V_{HYS-UVLO}$	Δ of V_{UVLO+} and $V_{UVLO–}$	150	260	550	mV
Input to Output Characteristics							
V_{BUS} switch resistance		$R_{DS-VBUSSWITCH}$	V_{BUS} = 5 V, I_{OUT} = 100 mA		120	200	mΩ
Turn-ON time		t_{ON}	R_L = 36 Ω, C_L = 400 pF		16		ms
Turn-OFF time		t_{OFF}	R_L = 36 Ω, C_L = 400 pF		50		µs
Input Overvoltage Protection (OVP)							
Input overvoltage protection threshold	V_{BUS}	V_{OVP}	V_{BUS} increasing from 6 V to 8 V	6.8	7	7.2	V
Maximum OV delay	V_{BUS}	$t_{PD(OVP)}$			0.25	1	µs
Hysteresis on OVP	V_{BUS}	$V_{HYS-UVLO}$	V_{BUS} decreasing from 8 V to 6 V	25	100	300	mV
Recovery time from input overvoltage condition	V_{BUS}	$t_{ON(OVP)}$	Time measured from V_{BUS} 8 V ≥ 6 V, 1-µs fall-time		8		ms

TOTAL SWITCH CURRENT CONSUMPTION

over operating free-air temperature range (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBAT Standby Current Consumption	$I_{BAT(Standby)}$	V_{BUS} = 0 V			30	µA
VBAT Operating Current Consumption	$I_{BAT(Operating)}$	V_{BUS} = 0 V			150	µA
VBUS Operating Current Consumption	I_{VBUS}	No load on OUT pin, V_{BUS} = 5 V	150		600	µA

AUDIO SWITCH ELECTRICAL CHARACTERISTICS(1)

V_{BAT} = 3 V to 4.4 V, V_{DDIO} = 2.8 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Switch							
Analog signal range		V_{AUDIO}		–0.8		0.8	V
ON-state resistance	S_L or S_R , DM or DP	r_{ON}	V_I = ±0.8 V, I_O = –20 mA, V_{BAT} = 3.F0 V		2	5.5	Ω
ON-state resistance match between channels	S_L or S_R , DM or DP	Δr_{ON}	V_I = 0.8 V, I_I = –20mA, V_{BAT} = 3.0 V		0.05	0.5	Ω
ON-state resistance flatness	S_L or S_R , DM or DP	$r_{ON(flat)}$	V_I = ±0.8 V, I_O = –20 mA, V_{BAT} = 3.0 V		0.05	0.2	Ω
V_I or V_O OFF leakage current		$I_{IO(OFF)}$	(V_I = 0 V, V_O = 0.8 V) or (V_I = 0.8 V, V_O = –0.8 V), V_{BAT} = 4.4 V, Switch OFF		200	500	nA
V_O ON leakage current		$I_{IO(ON)}$	V_I = OPEN, V_O = –0.8 V or 0.8 V, V_{BAT} = 4.4 V, Switch ON		10	300	nA
Dynamic							
Turn-ON time	From receipt of I^2C stop bit	t_{ON}	V_I or V_O = V_{BAT}, R_L = 50 Ω, C_L = 35 pF		120		µs
Turn-OFF time	From receipt of I^2C stop bit	t_{OFF}	V_I or V_O = V_{BAT}, R_L = 50 Ω, C_L = 35 pF		4.5		µs
V_I OFF capacitance		$C_{I(OFF)}$	DC bias = 0 V or 1.6 V, f = 10 MHz, Switch OFF		5.5		pF
V_O OFF capacitance		$C_{O(OFF)}$	DC bias = 0 V or 1.6 V, f = 10 MHz, Switch OFF		10		pF
V_I, V_O ON capacitance		$C_{I(ON)}$, $C_{O(ON)}$	DC bias = 0 V or 1.6 V f = 10 MHz, Switch ON		13		pF
Bandwidth		BW	R_L = 50 Ω, Switch ON		450		MHz
OFF Isolation		O_{ISO}	f = 20 kHz, R_L = 50 Ω, Switch OFF		–100		dB
Crosstalk		X_{TALK}	f = 20 kHz, R_L = 50 Ω		–85		dB
Total harmonic distortion		THD	R_L = 16 Ω, C_L = 20 pF, f = 20 Hz to 20 kHz, 1.6-V_{pp} output		0.05		%

(1) V_I is equal to the asserted voltage on S_R and S_L pins. V_O is equal to the asserted voltage on DP and DM pins. I_I is equal to the current on the S_R and S_L pins. I_O is equal to the current on the DP and DM pins.

MIC SWITCH ELECTRICAL CHARACTERISTICS (1)

V_{BAT} = 3 V to 4.4 V, V_{DDIO} = 2.8 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Switch							
Analog signal range		V_{MICIO}		0		2.3	V
ON-state resistance	MIC, V_{BUS}	r_{ON}	V_I = 2.3 V, I_O = –2 mA, V_{BAT} = 3 V		40	70	Ω
V_I or V_O OFF leakage current		$I_{IO(OFF)}$	V_I = 0.3 V, V_O = 2.3 V or V_I = 2.3 V, V_O = 0.3 V, V_{BAT} = 4.4 V, Switch OFF		5	500	nA
MIC pulldown resistance		$R_{PD\ (ON)}$	V_I = OPEN, V_O = 1.35 V, V_{BAT} = 4.4 V, Switch ON		1.5		kΩ
Dynamic							
Turn-ON time	From receipt of I^2C ACK bit	t_{ON}	V_I or V_O = V_{BAT}, R_L = 50 Ω, C_L = 35 pF		120		µs
Turn-OFF time	From receipt of I^2C ACK bit	t_{OFF}	V_I or V_O = V_{BAT}, R_L = 50 Ω, C_L = 35 pF		11		µs
V_I OFF capacitance		$C_{I(OFF)}$	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF		140		pF
V_O OFF capacitance		$C_{O(OFF)}$	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF		10.5		pF
V_I, V_O ON capacitance		$C_{I(ON)}$, $C_{O(ON)}$	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch ON		140		pF
Bandwidth		BW	R_L = 50 Ω, Switch ON		40		MHz
OFF Isolation		O_{ISO}	f = 20 kHz, R_L = 50 Ω, Switch OFF		–95		dB
Crosstalk		X_{TALK}	f = 20 kHz, R_L = 50 Ω, to audio output		–85		dB
Total harmonic distortion		THD	RL = 600 Ω, CL = 20 pF, f = 20 Hz–20 kHz , V_{in}=0.1 V_{pp} centered at V_{BAT}/2		0.46	0.65	%

(1) V_I is equal to the asserted voltage on V_{BUS} pin. V_O is equal to the asserted voltage on MIC pin. I_I is equal to the current on the V_{BUS} pin. I_O is equal to the current on the MIC pin.

VIDEO SWITCH ELECTRICAL CHARACTERISTICS(1)

V_{BAT} = 3.0 V to 4.4 V, V_{DDIO} = 2.8 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Switch							
Analog signal range		$V_{VIDEOIO}$		–0.5		2	V
ON-state resistance	V_L, V_R, or VIDEO DM, DP, or ID	r_{ON}	V_I = 0.5 V to 2 V, I_O = –20 mA, V_{BAT} = 3.0 V		12	18	Ω
ON-state resistance match between channels	V_L, V_R DM, DP	Δr_{ON}	V_I = 1.0 V, I_I = –2.0 mA, V_{BAT} = 3.0 V		0.5	2	Ω
ON-state resistance flatness	V_L, V_R DM, DP	$r_{ON(flat)}$	V_I = 0.5 V to 2.0 V, I_O = –20 mA, V_{BAT} = 3.0 V		0.5	2	Ω
V_I or V_O OFF leakage current		$I_{IO(OFF)}$	V_I = 0.3 V, V_O = 2.0 V or V_I = 2 V, V_O = 0.3 V, V_{BAT} = 4.4 V, Switch OFF		60	360	nA
V_O ON leakage current		$I_{IO(ON)}$	V_I = OPEN, V_O = 0.3 V or 2.0 V, V_{BAT} = 4.4 V, Switch ON		60	360	nA
Dynamic							
Turn-ON time	From receipt of I^2C ACK bit	t_{ON}	V_I or V_O = V_{BAT}, R_L = 50 Ω, C_L = 35 pF		70		µs
Turn-OFF time	From receipt of I^2C ACK bit	t_{OFF}	V_I or V_O = V_{BAT}, R_L = 50 Ω, C_L = 35 pF		26		µs
V_I OFF capacitance		$C_{I(OFF)}$	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF		3		pF
V_O OFF capacitance		$C_{O(OFF)}$	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF		10		pF
V_I, V_O ON capacitance		$C_{I(ON)}$, $C_{O(ON)}$	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch ON		12		pF
Bandwidth		BW	R_L = 50 Ω, Switch ON		450		MHz
OFF Isolation		O_{ISO}	f = 10 MHz, $R_{L(VIDEO)}$ = 50 Ω, Switch OFF		–58		dB
Crosstalk		X_{TALK}	f = 10 MHz, $R_{L(VIDEO)}$ = 50 Ω, Switch ON		–60		dB
Total harmonic distortion	V_L or V_R	THD	R_L = 600 Ω, C_L = 20 pF, f = 20 Hz~20 kHz , 2.3V_{pp} output		0.05		%

(1) V_O is equal to the asserted voltage on DP, DM, and ID pins. V_I is equal to the asserted voltage on D+, D–, and IDBP pins. I_O is equal to the current on the DP, DM, and ID pins. I_I is equal to the current on the D+, D–, and IDBP pins.

USB SWITCH ELECTRICAL CHARACTERISTICS(1)

V_{BAT} = 3 V to 4.4 V, V_{DDIO} = 2.8 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Switch							
Analog signal range		V_{USBIO}		0		V_{BAT}	V
ON-state resistance	D–, D+, or IDBP DM, DP, or ID	r_{ON}	V_I = 0 V to 3.6 V, I_O = –2 mA, V_{BAT} = 3 V		8	15	Ω
ON-state resistance match between channels	D–, D+ DM, DP	Δr_{ON}	V_I = 0.4 V, I_O = –2 mA, V_{BAT} = 3 V		0.5	1	Ω
ON-state resistance flatness	D–, D+ DM, DP	$r_{ON(flat)}$	V_I = 0 V to 3.6 V, I_O = –2 mA, V_{BAT} = 3 V		0.5	1	Ω
V_I or V_O OFF leakage current		$I_{IO(OFF)}$	V_I = 0.3 V, V_O = 2.7 V or V_I = 2.7 V, V_O = 0.3 V, V_{BAT} = 4.4 V, Switch OFF		45	360	nA
V_O ON leakage current		$I_{IO(ON)}$	V_I = OPEN, V_O = 0.3 V or 2.7 V, V_{BAT} = 4.4 V, Switch ON		50	360	nA
Dynamic							
Turn-ON time	From receipt of I^2C ACK bit	t_{ON}	V_I or V_O = V_{BAT}, R_L = 50 Ω, C_L = 35 pF		95		µs
Turn-OFF time	From receipt of I^2C ACK bit	t_{OFF}	V_I or V_O = V_{BAT}, R_L = 50 Ω, C_L = 35 pF		25		µs
V_I OFF capacitance		$C_{I(OFF)}$	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF		3		pF
V_O OFF capacitance		$C_{O(OFF)}$	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF		10		pF
V_I, V_O ON capacitance		$C_{I(ON)}$, $C_{O(ON)}$	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch ON		11		pF
Bandwidth		BW	R_L = 50 Ω, Switch ON		510		MHz
OFF Isolation		O_{ISO}	f = 240 MHz, R_L = 50 Ω, Switch OFF		–24		dB
Crosstalk		X_{TALK}	f = 240 MHz, R_L = 50 Ω		–40		dB

(1) V_O is equal to the asserted voltage on DP, DM, and ID pins. V_I is equal to the asserted voltage on D+, D–, and IDBP pins. I_O is equal to the current on the DP, DM, and ID pins. I_I is equal to the current on the D+, D–, and IDBP pins.

GENERAL OPERATION

The TSU6712 will automatically detect accessories plugged into the phone via the mini USB 5 pin connector. The type of accessory detected will be stored in I^2C registers within the TSU6712 for retrieval by the host. The TSU6712 has a network of switches that can be automatically opened and closed base on the accessory detection. See Table 1 for details of which switches are open during each mode of operation. For flexibility, the TSU6712 also offers a manual switching mode allowing the host processor to decide which switches should be opened and closed and execute the settings through the I^2C interface.

Standby Mode

Standby mode is the default mode upon power up and occurs when no accessory has been detected. During this mode, the VBUS and ID lines are continually monitored through comparators to determine when an accessory is inserted. Power consumption is minimal during standby mode.

Accessory ID Detection

If VBUS is high and the attachment is not a charger, then determine the impedance on the ID pin. If VBUS is low and an accessory is attached, then use an ADC for impedance sensing on the ID pin to identify which accessory is attached and/or what kind of remote control key button is pushed.

Impedance Buckets for Each Accessory and Remote Control Key Button

In order to implement ID detection, each accessory and remote control key button of audio accessory should contain below ID impedance resistor value which is 1% tolerance accuracy.

OVP OPERATION

The device continuously monitors the input voltage and the input current as described in detail in the following sections.

Input Overvoltage Protection

When the input voltage rises above V_{OVP}, the internal V_{BUS} switch is turned off, removing power from the circuit. The response is very rapid, with the FET switch turning off in less than 1 µs. The OVP_EN interrupt bit is set high when an overvoltage condition is detected. When the input voltage returns below $V_{OVP} – V_{HYS-OVP}$ and remains above V_{UVLO}, the V_{BUS} FET switch is turned on again after a deglitch time of $t_{ON(OVP)}$. The deglitch time ensures that the input supply has stabilized before turning the switch on. When the OVP condition is cleared, the OVP_OCP_DIS interrupt bit is set high.

OVP Glitch Immunity

When V_{BUS} is near the OVP threshold, noise on V_{BUS} cause spurious OVP triggering. To avoid this, OVP glitch immunity allows noise on the V_{BUS} line to be rejected. The glitch protection circuitry integrates the glitch over time allowing the OVP circuitry to trigger faster for larger voltage excursions above the OVP threshold and slower for shorter excursions. The protection circuitry has a maximum OV delay of 1 µs

AV Cable Detection

Once an A/V cable is attached with 365 kΩ ID resistance and/or 75 Ω load resistance, the ID voltage will drop below the internal comparator reference level of the TSU6712 and the ADC block of the TSU6712 will determine the ID line impedance value. The ID detect signal that is sent to the logic control block will be set equal to an A/V cable accessory. With the video driver in the phone enabled, detection block of the TSU6712 will sense that the 75ohm load resistance at the end of the A/V cable is still attached since the video sync pulse will always be present.

Power-On Reset

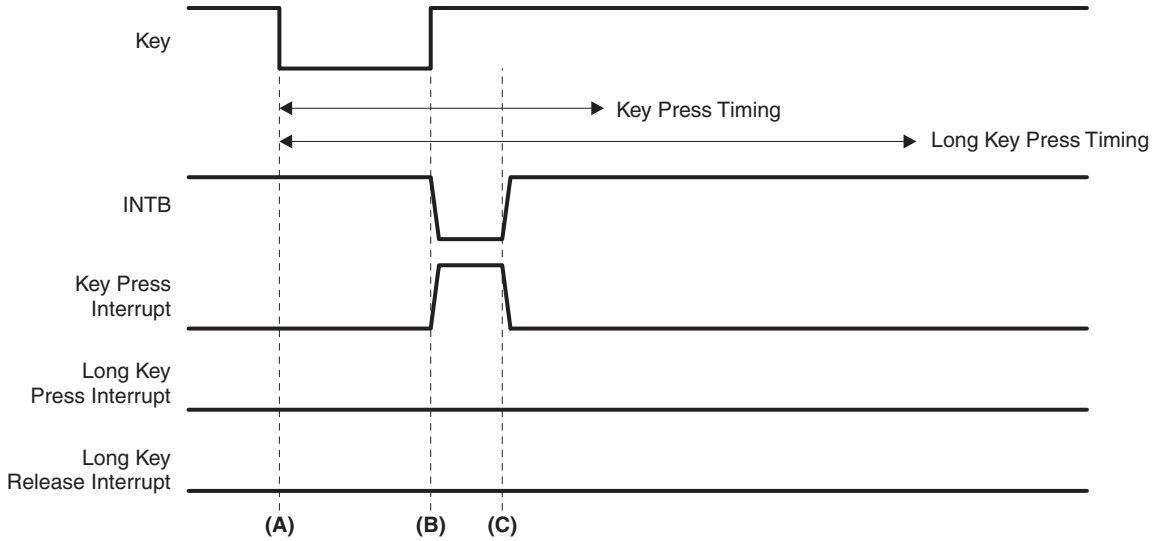
When power (from 0 V) is applied to V_{BAT}, an internal power-on reset holds the TSU6712 in a reset condition until V_{BAT} has reached V_{POR}. At that point, the reset condition is released, and the TSU6712 registers and I^2C state machine initialize to their default states.

After the initial power-up phase, V_{BAT} must be lowered to below 0.2 V and then back up to the operating voltage (V_{DDIO}) for a power-reset cycle.

Software Reset

The TSU6712 has software reset feature. Hold low both SCL and SDA more than 30ms will reset digital logic of the TSU6712. After resetting, INTB will keep low until INT_Mask bit of Control register (0x02) is cleared.

Key Press Identification

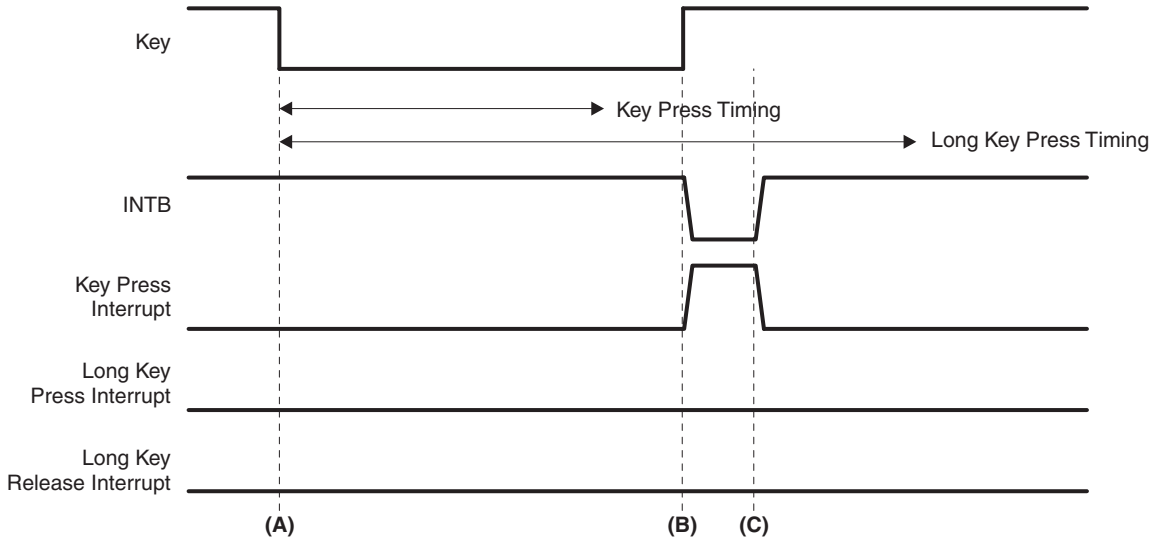


A. Key press

B. Released key press → Set KP Interrupt → Set error bit in Button register → INTB pulled low

C. I^2C read of INT register → Clear KP interrupt → INTB goes back high

Figure 1. Short Key Press

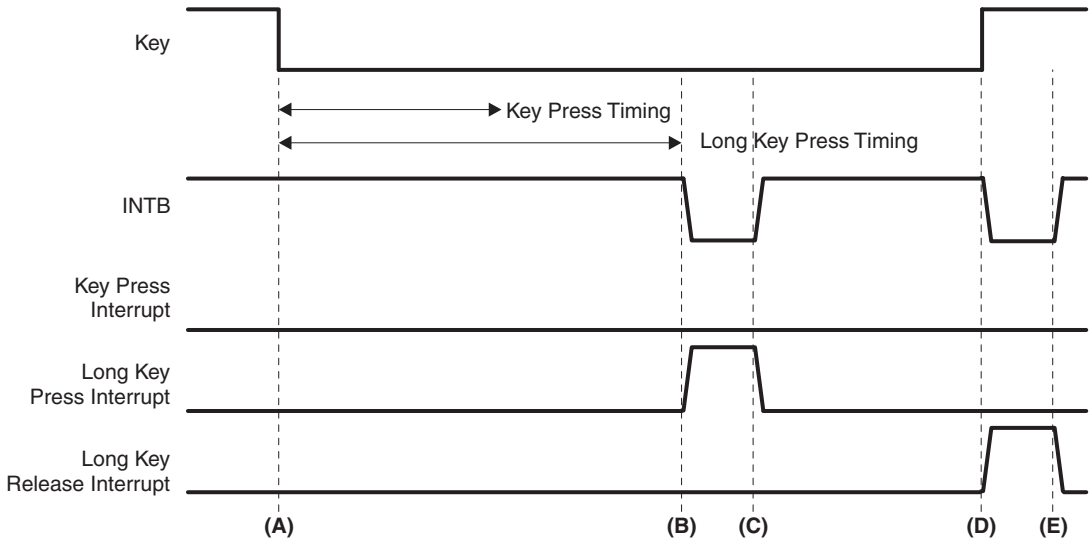


A. Key press

B. Released key press → Set KP Interrupt → Set Key (S/E, 1–12) bit in Button register → INTB pullled low

C. I^2C read of INT register → Clear KP interrupt → INTB goes back high

Figure 2. Normal Key Press



A. Key press

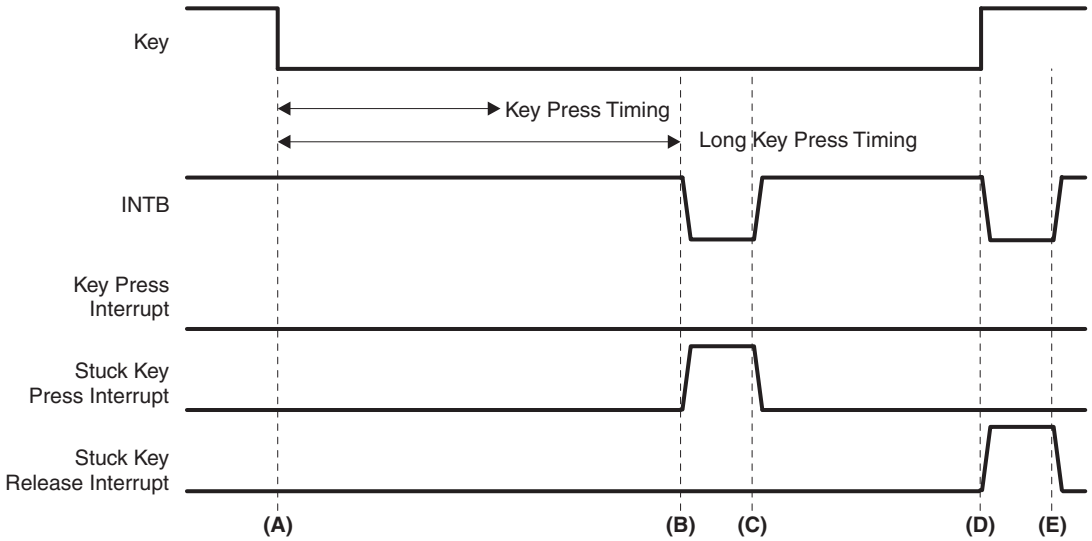
B. Long key press timing reached → Set LKP interrupt bit → Set Key (S/E, 1–12) bit in Button register → INTB pullled low

C. I^2C read of INT register → Clear LKP interrupt bit → INTB goes back high

D. Released key press → Set LKR Interrupt bit → INTB pullled low

E. I^2C read of INT register → Clear LKR interrupt bit→ INTB goes back high

Figure 3. Long Key Press



A. Key press detected when accessory attached
B. Long key press timing reached → Set SK interrupt bit → Set Key (S/E, 1–12) bit in Button register → INTB pullled low
C. I^2C read of INT register → Clear SK interrupt bit → INTB goes back high
D. Released key press detected when accessory ID resistor is 1 MΩ → Set SKR Interrupt bit → INTB pullled low
E. I^2C read of INT register → Clear SKR interrupt bit→ INTB goes back high

Figure 4. Stuck Key Press

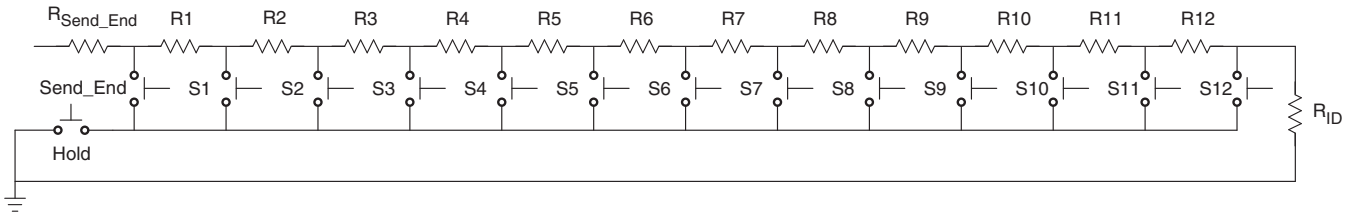


Figure 5. Audio / Remote Controller Accessory

Table 1. Accessory Detection Scheme
1% ID Resistor Tolerance (Resistor Values and Part Numbers)

ACCCESSORY	ID RESISTOR VALUE ON ACCESSORY	DETECTED IMPEDANCE ON TSU6712	ADC VALUE
OTG	–	–	00000
Send_End Button	2K	2K	00001
Stereo Headset with RC S1 Button	0.604K	2.604K	00010
Stereo Headset with RC S2 Button	0.604K	3.208K	00011
Stereo Headset with RC S3 Button	0.806K	4.014K	00100
Stereo Headset with RC S4 Button	0.806K	4.82K	00101
Stereo Headset with RC S5 Button	1.21K	6.03K	00110
Stereo Headset with RC S6 Button	2K	8.03K	00111
Stereo Headset with RC S7 Button	2K	10.03K	01000
Stereo Headset with RC S8 Button	2K	12.03K	01001
Stereo Headset with RC S9 Button	2.43K	14.46K	01010
Stereo Headset with RC S10 Button	2.8K	17.26K	01011
Stereo Headset with RC S11 Button	3.24K	20.5K	01100
Stereo Headset with RC S12 Button	3.57K	24.07K	01101
Audio Device Type 3	28.7K	28.7K	01110
Reserved Accessory #2	34K	34K	01111
Reserved Accessory #4	49.9K	49.9K	10001
Reserved Accessory #5	64.9K	64.9K	10010
Audio Device Type 2	56.2K	80.27K	10011
Phone Powered Device	102K	102K	10100
TTY Converter	121K	121K	10101
UART Cable	150K	150K	10110
Type 1 Charger	200K	200K	10111
Factory Mode Cable –Boot Off USB	255K	255K	11000
Factory Mode Cable –Boot On USB	301K	301K	11001
Audio/Video Cable	365K	365K	11010
Type 2 Charger	442K	442K	11011
Factory Mode Cable – Boot Off UART	523K	523K	11100
Factory Mode Cable – Boot On UART	619K	619K	11101
Stereo Headset with Remote (Audio Device Type 1)	976K	1000.07K	11110
Mono/Stereo Headset (Audio Device Type 1)	1000K	1002K	11110
No Device	–	–	11111

Standard I²C Interface Details

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by the master sending a START condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 6). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.

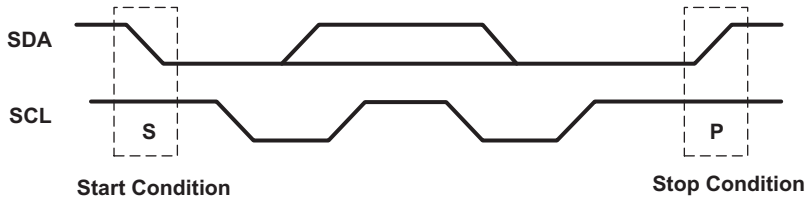


Figure 6. Definition of START and STOP Conditions

The data byte follows the address ACK. The R/W bit is kept low for transfer from the master to the slave. The data byte is followed by an ACK sent from this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (tpv) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I^2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (START or STOP) (see Figure 7).

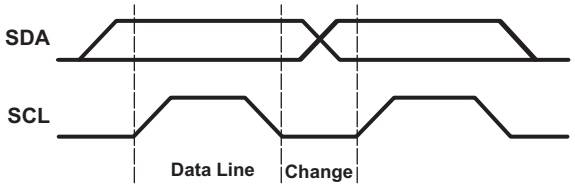


Figure 7. Bit Transfer

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 6).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 8). Setup and hold times must be taken into account.

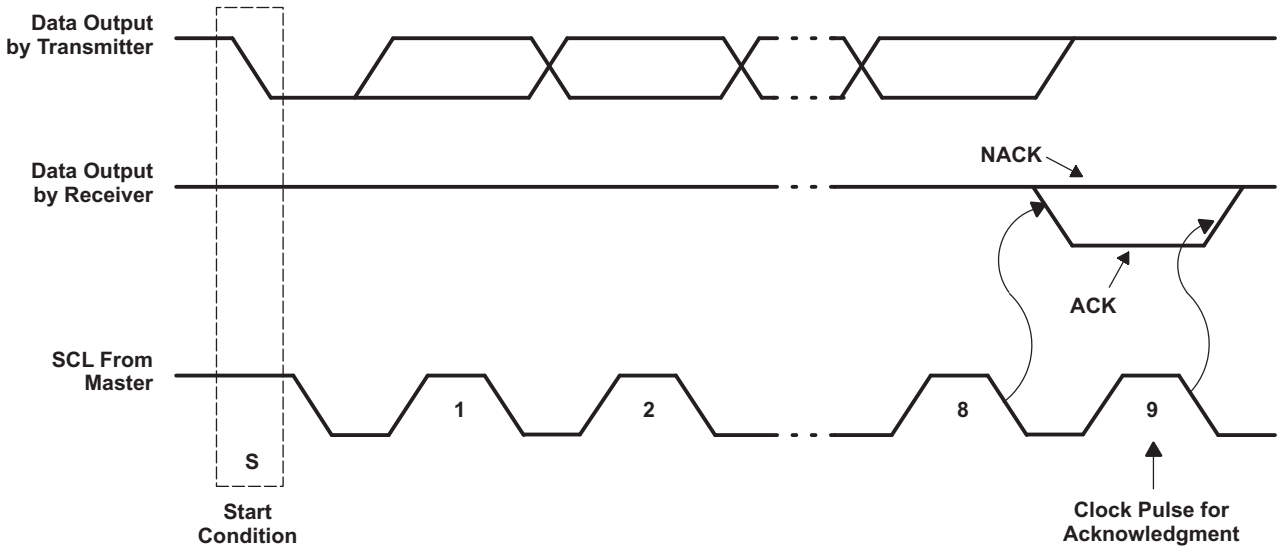


Figure 8. Acknowledgment on I^2C Bus

Writes

Data is transmitted to the TSU6712 by sending the device slave address and setting the LSB to a logic 0 (see Figure 9 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. The next byte is written to the specified register on the rising edge of the ACK clock pulse.

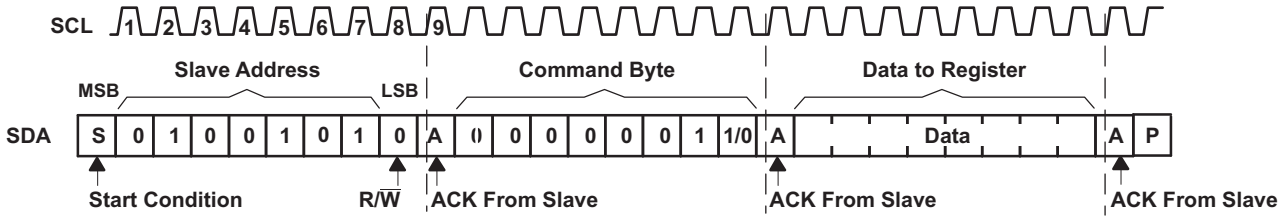


Figure 9. Write to Register

Reads

The bus master first must send the TSU6712 slave address with the LSB set to a logic 0. The command byte is sent after the address and determines which register is accessed. After a restart, the device slave address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TSU6712. Data is clocked into the SDA output shift register on the rising edge of the ACK clock pulse. See Figure 10.

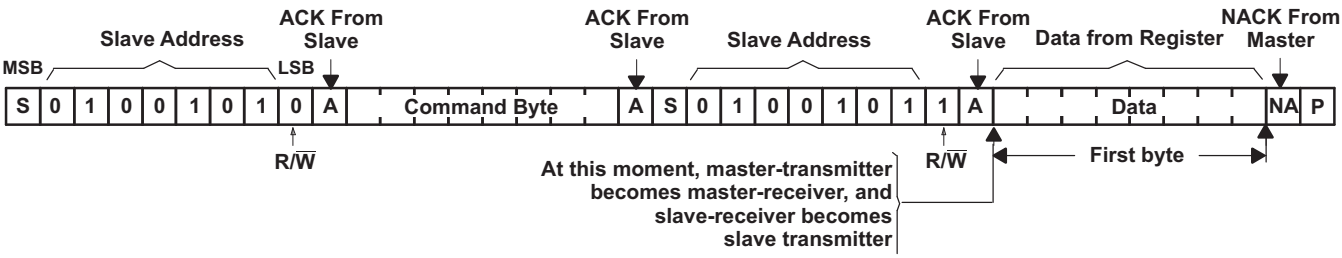


Figure 10. Read From Register

Clear INT Registers Upon Read

The TSU6712 I^2C logic core is set to clear all INT bits in a register after that register is read by the host. When the acknowledge is received from the Master after the INT register has been read, the contents of the register is reset to the default state.

I^2C Timing

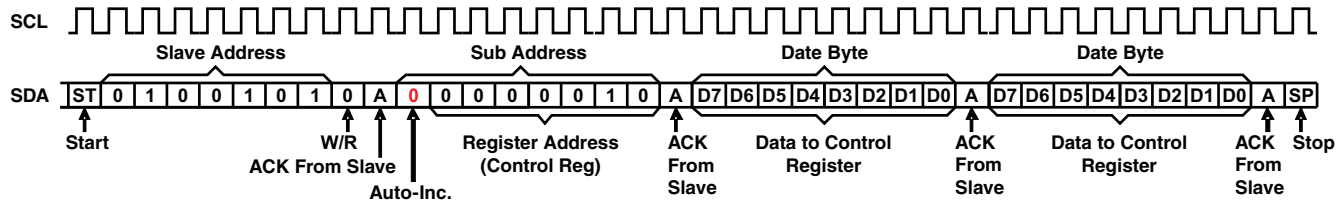


Figure 11. Repeated Data Write to a Single Register

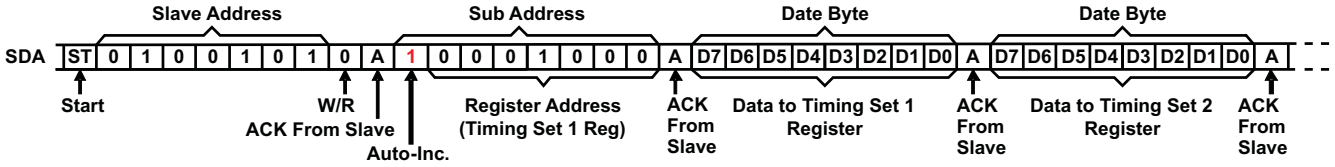


Figure 12. Burst Data Write to Multiple Registers

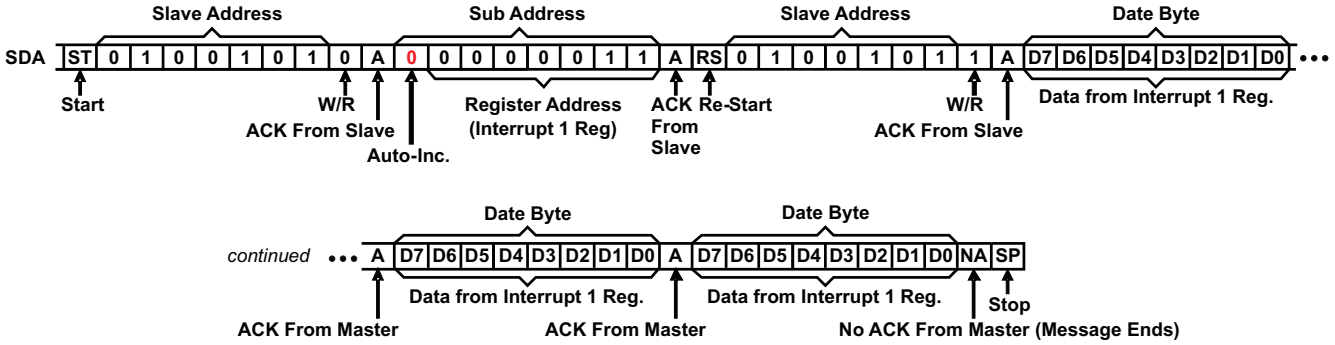


Figure 13. Repeated Data Read from a Single Register – Combined Mode

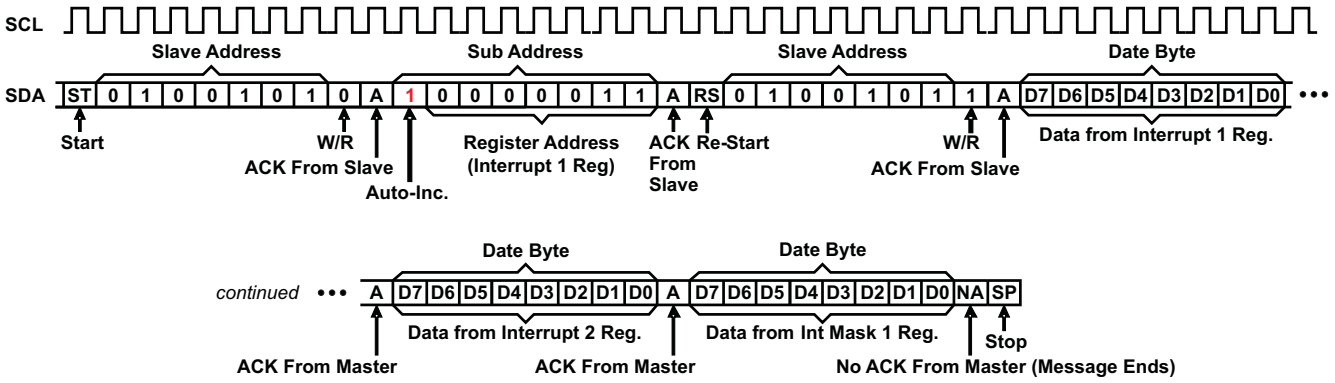


Figure 14. Burst Data Read from Multiple Registers – Combined Mode

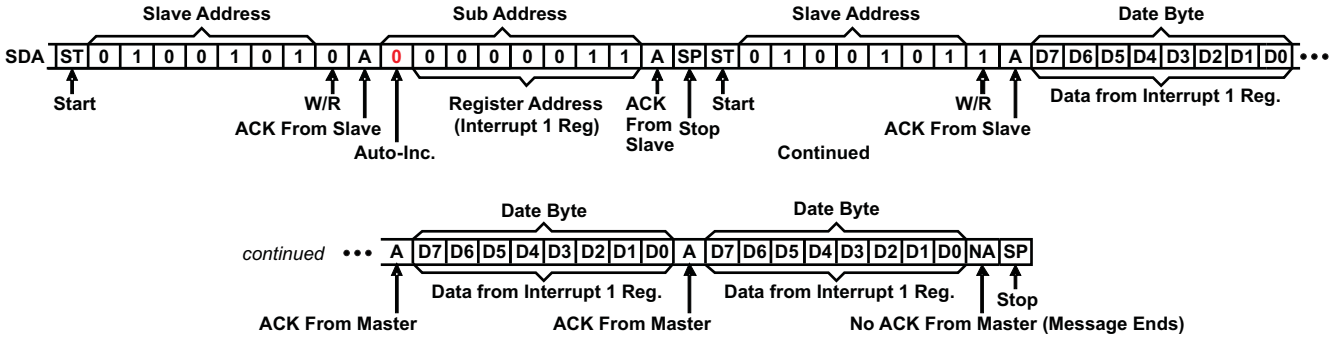


Figure 15. Repeated Data Read from a Single Register – Split Mode

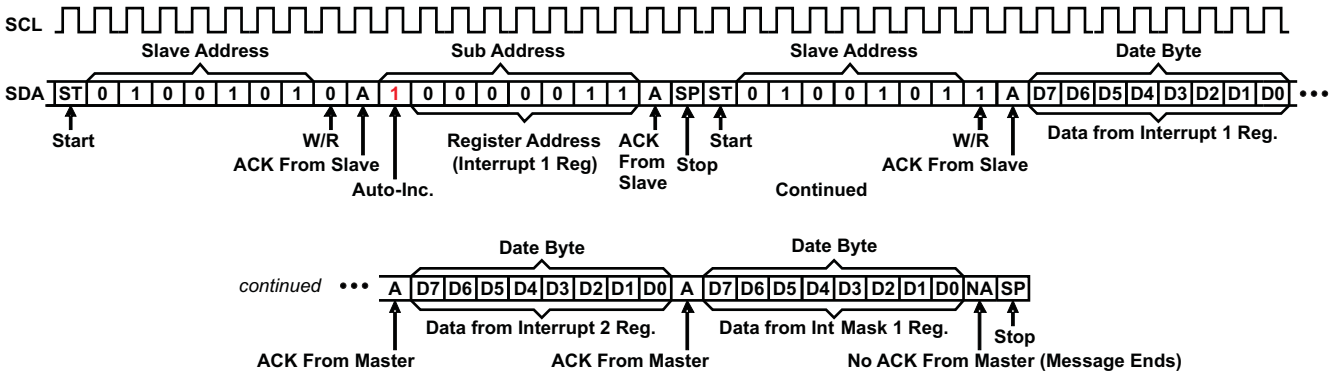


Figure 16. Burst Data Read from Multiple Registers – Split Mode

A. SDA is pulled low on ACK from slave or ACK from master.

B. Register writes always require sub-address write before first data byte.

C. Repeated data writes to a single register continue indefinitely until stop or restart.

D. Repeated data reads from a single register continue indefinitely until no ACK from master.

E. Burst data writes start at the specified register address, then advance to the next register address, even to the read-only registers. For these registers, data write appears to occur, though no data are changed by the writes. After register 14h is written, writing resumes to register 01h and continues until stop or restart.

F. Burst data reads start at the specified register address, then advance to the next register address. Once register 14h is read, reading resumes from register 01h and continues until No ACK from master.

I²C Register Map (1) (2) (3)

ADDR	REGISTER	TYPE	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT4	BIT 3	BIT 2	BIT1	BIT0
01h	Device ID	R	01010010	Version ID					Vendor ID		
02h	Control	R/W	xxx11111				Switch Open	Raw Data	Manual S/W	Wait	INT Mask
03h	Interrupt 1	R	00000000	OVP_OCP_DIS	OCP_EN	OVP_EN	LKR	LKP	KP	Detach	Attach
04h	Interrupt 2	R	x0000000		OTP_EN	CONNECT	Stuck_Key_RCV	Stuck_Key	ADC_Change	Reserved_Attach	A/V_Charging
05h	Interrupt Mask 1	R/W	00000000	OVP_OCP_DIS	OCP_EN	OVP_EN	LKR	LKP	KP	Detach	Attach
06h	Interrupt Mask 2	R/W	x0000000		OTP_EN	CONNECT	Stuck_Key_RCV	Stuck_Key	ADC_Change	Reserved_Attach	A/V_Charging
07h	ADC	R	xxx11111				ADC Value				
08h	Timing Set 1	R/W	00000000	Key Press				Device Wake Up			
09h	Timing Set 2	R/W	00000000	Switching Wait				Long Key Press			
0Ah	Device Type 1	R	00000000	USB OTG	DCP	CDP		UART	USB	Audio Type2	Audio Type1
0Bh	Device Type 2	R	00000000	Audio Type3	A/V	TTY	PPD	JIG_UART_OFF	JIG_UART_ON	JIG_USB_OFF	JIG_USB_ON
0Ch	Button 1	R	00000000	7	6	5	4	3	2	1	Send_End
0Dh	Button 2	R	x0000000		Unknown	Error	12	11	10	9	8
0Fh	Unused Int 1 (4)	R	00000000								
10h	Unused Int 2 (4)	R	xxxx0000								
11h	Unused Int Mask 1 (4)	R/W	00000000								
12h	Unused Int Mask 2 (4)	R/W	xxxx0000								
13h	Manual S/W 1	R/W	00000000	D– Switching			D+ Switching			VBUS Switching	
14h	Manual S/W 2	R/W	xxx00000				Charger DET	BOOT_SW	JIG-ON	ID Switching	

(1) Do not use blank register bits.
(2) Write "0" to the blank register bits.
(3) Values read from the blank register bits are not defined and invalid.
(4) In order to prevent unused interrupts from interfering with normal operation, it is advised to write ‘FFh’ to Reg. 11h and ‘0Fh’ to Reg. 12h on start-up. Otherwise, Reg. 0Fh and 10h must be read to clear an interrupt if Reg. 03h and 04h have been read and contain data ‘00h’

Table 2. Slave Address

NAME	SIZE(BITS)	DESCRIPTION							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Slave address	8	0	1	0	0	1	0	1	R/W

Device ID

Address: 01h
Reset Value: 01010010
Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0-2	Version ID	4	A unique number for vendor 010b for Texas Instruments
4-7	Vendor ID	5	A unique number for chip version 01010b for TSU6712

Control

Address: 02h
Reset Value: xxx11111
Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	INT Mask	1	0: Unmask interrupt 1: Mask interrupt
1	Wait	1	0: Wait until host re-sets this bit(WAIT bit) high 1: Wait until Switching timer is expired defined in Timing Set 1
2	Manual S/W	1	0: Manual Switching 1: Automatic Switching
3	RAW Data	1	0: Report the status changes on ID to Host 1: Don't report the status changes on ID
4	Switch Open	1	0: Open all Switches (Including load switch) 1: Automatic Switching by accessory status
5-7	Unused	3	

Interrupt 1

Address: 03h
Reset Value: 00000000
Type: Read and Clear

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Attach	1	1: Accessory is attached
1	Detach	1	1: Accessory is detached
2	KP	1	1: Key press
3	LKP	1	1: Long key press
4	LKR	1	1: Long key release
5	OVP_EN	1	1: OVP enabled
6	OCP_EN	1	1: OCP enabled
7	OVP_OCP_DIS	1	1: OVP_OCP disabled

Interrupt 2

Address: 04h
Reset Value: x0000000
Type: Read and Clear

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	A/V_Charging	1	1: Charger detected when A/V cable is attached
1	Reserved_Attach	1	1: Reserved Device is attached
2	ADC_Change	1	1: ADC value is changed when RAW data is enabled
3	Stuck_Key	1	1: Stuck Key is detected
4	Stuck_Key_RCV	1	1: Stuck Key is recovered
5	Connect	1	1: Switch is connected(closed)
6	OTP_EN	1	1: Over Temperature Protection enabled
7	Unused	1	

Interrupt Mask 1

Address: 05h
Reset Value: 00000000
Type: Read and Clear

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Attach	1	0: Unmask Attach Interrupt 1: Mask Attach Interrupt
1	Detach	1	1: Mask Detach Interrupt 0: Unmask Key press Interrupt
2	KP	1	0: Unmask Key press Interrupt 1: Mask Key press Interrupt
3	LKP	1	0: Unmask Long key press Interrupt 1: Mask Long key press Interrupt
4	LKR	1	0: Unmask Long key release Interrupt 1: Mask Long key release Interrupt
5	OVP_EN	1	0: Unmask OVP_EN Interrupt 1: Mask OVP_EN Interrupt
6	OCP_EN	1	0: Unmask OCP_EN Interrupt 1: Mask OCP_EN Interrupt
7	OVP_OCP_DIS	1	0: Unmask OVP_OCP_DIS Interrupt 1: Mask OVP_OCP_DIS Interrupt

Interrupt Mask 2

Address: 06h
Reset Value: x0000000
Type: Read and Clear

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	A/V_Charging	1	0: Unmask A/V_Charging Interrupt 1: Mask A/V_Charging Interrupt
1	Reserved_Attach	1	0: Unmask Reserved_Attach Interrupt 1: Mask Reserved_Attach Interrupt
2	ADC_Change	1	0: Unmask ADC_Change Interrrupt 1: Mask ADC_Change Interrrupt
3	Stuck_Key	1	0: Unmask Stuck_Key Interrupt 1: Mask Stuck_Key Interrupt
4	Stuck_Key_RCV	1	0: Unmask Stuck_Key_RCV Interrupt 1: Mask Stuck_Key_RCV Interrupt
5	Connect	1	0: Unmask Connect Interrupt 1: Mask Connect Interrupt t
6	OTP_EN	1	0: Unmask OTP_EN Interrupt 1: Mask OTP_EN Interrupt
7	Unused	1	

ADC Value

Address: 07h
Reset Value: xxx11111
Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0-4	ADC value	5	ADC value read from ID
5-7	N/A	3	

Timing Set 1

Address: 08h
Reset Value: 00000000
Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0-3	Device wake up	4	Device wake up duration
4-7	Key press	4	Normal key press duration

Timing Set 2

Address: 09h
Reset Value: 00000000
Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0-3	Long key press	4	Long key press duration
4-7	Switching wait	4	Waiting duration before switching

Table 3. Time Table

SETTING VALUE	DEVICE WAKE UP	KEY PRESS	LONG KEY PRESS	SWITCHING WAIT
0000	50 ms	100 ms	300 ms	10 ms
0001	100 ms	200 ms	400 ms	30 ms
0010	150 ms	300 ms	500 ms	50 ms
0011	200 ms	400 ms	600 ms	70 ms
0100	300 ms	500 ms	700 ms	90 ms
0101	400 ms	600 ms	800 ms	110 ms
0110	500 ms	700 ms	900 ms	130 ms
0111	600 ms	800 ms	1000 ms	150 ms
1000	700 ms	900 ms	1100 ms	170 ms
1001	800 ms	1000 ms	1200 ms	190 ms
1010	900 ms	–	1300 ms	210 ms
1011	1000 ms	–	1400 ms	–
1100	–	–	1500 ms	–
1101	–	–	–	–
1110	–	–	–	–
1111	–	–	–	–

Device Type 1

Address: 0Ah
Reset Value: 000x0000
Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Audio type 1	1	Audio device type 1
1	Audio type 2	1	Audio device type 2
2	USB	1	USB host
3	UART	1	UART
4	Unused	1	
5	CDP	1	Charging Downstream Port (USB Host Hub Charger)
6	DCP	1	Dedicated Charging Charger
7	USB OTG	1	USB on-the-go device

Device Type 2

Address: 0Bh
Reset Value: 00000000
Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	JIG_USB_ON	1	Factory mode cable
1	JIG_USB_OFF	1	Factory mode cable
2	JIG_UART_ON	1	Factory mode cable
3	JIG_UART_OFF	1	Factory mode cable
4	PPD	1	Phone-powered device
5	TTY	1	TTY converter
6	A/V	1	A/V cable
7	Audio Type 3	1	Audio device type 3

Button 1

Address: 0Ch
Reset Value: 00000000
Type: Read and Clear

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Send_End	1	Send_End key is pressed
1	1	1	Number 1 key is pressed
2	2	1	Number 2 key is pressed
3	3	1	Number 3 key is pressed
4	4	1	Number 4 key is pressed
5	5	1	Number 5 key is pressed
6	6	1	Number 6 key is pressed
7	7	1	Number 7 key is pressed

Button 2

Address: 0Dh
Reset Value: x0000000
Type: Read and Clear

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	8	1	Number 8 key is pressed
1	9	1	Number 9 key is pressed
2	10	1	Number 10 key is pressed
3	11	1	Number 11 key is pressed
4	12	1	Number 12 key is pressed
5	Error	1	Error key is pressed
6	Unknown	1	Unknown key is pressed
7	Unused		

Manual S/W 1

Address: 13h
Reset Value: 00000000
Type: Read and write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0-1	V_{BUS} Switching	2	00: Open all switch 01: V_{BUS} is connected to OUT (charger) 10: V_{BUS} is connected to MIC
2-4	D+ Switching	3	000: Open all switch 001: D+ is connected to D+ of USB port 010: D+ is connected to S_R 011: D+ is connected to RxD of UART 100: D+ Connected to V_R
5-7	D– Switching	3	000: Open all switch 001: D– is connected to D– of USB port 010: D– is connected to S_L 011: D– is connected to TxD of UART 100: D– Connected to V_L

Manual S/W 2

Address: 14h
Reset Value: xxx00000
Type: Read and write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0-1	ID Switching	2	00: Open all switch 01: ID is connected to Video 10: ID is connected to IDBP
2	JIG	1	0: Low 1: High
3	BOOT	1	0: Low 1: High
4	ISET	1	0: High Impedance 1: GND
5-7	N/A		

Application Schematic

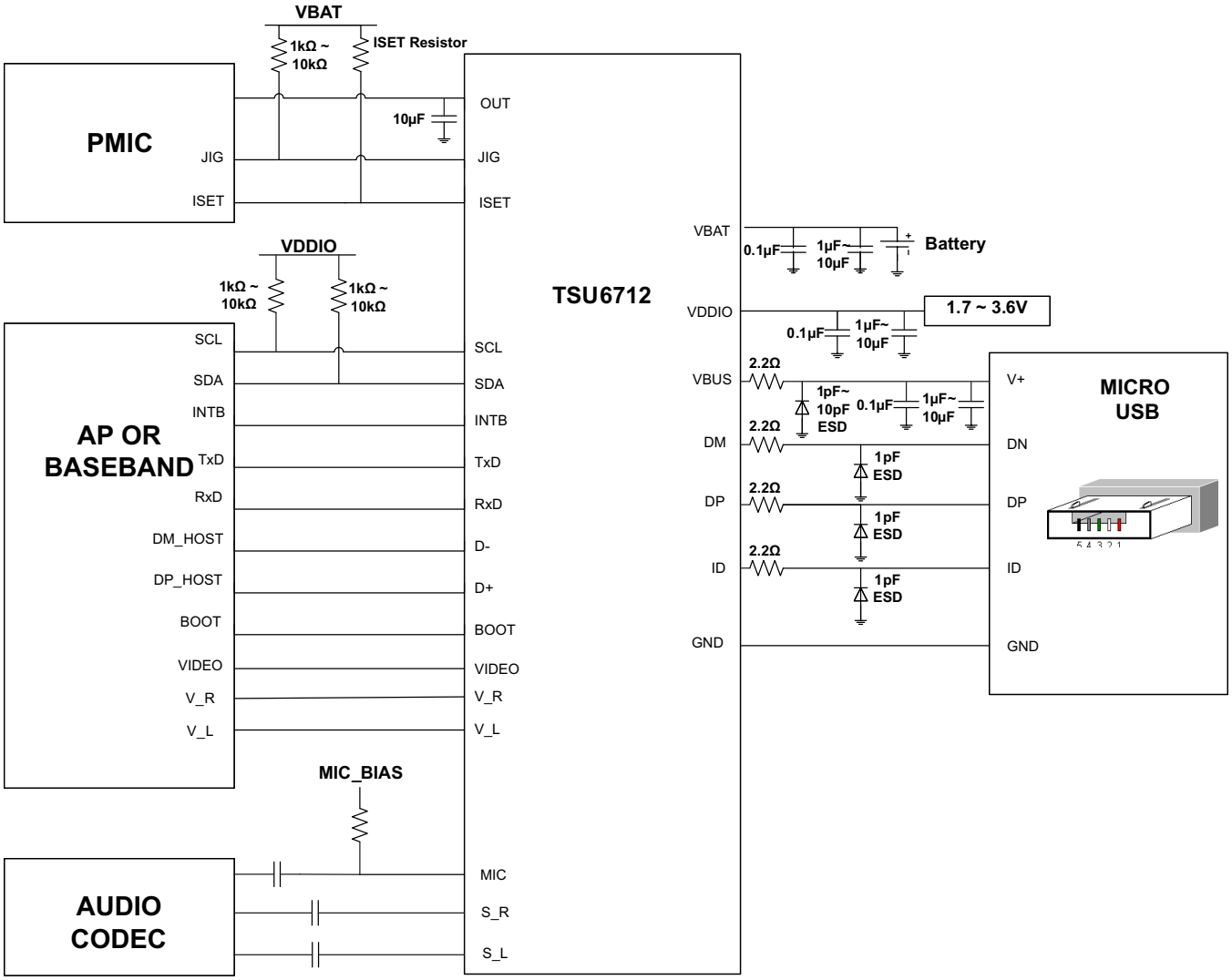


Figure 17. TSU6712 Application Schematic

Table 4. Critical Components

Pin Name	Pin Number	Critical Component
V_{BUS}	A5	1µF~10µF
		ESD Protection Diode
		0.1 µF
V_{DDIO}	A2	1µF~10 µF
		0.1 µF
V_{BAT}	D1	1µF~10µF
		Battery
		0.1 µF
JIG	E4	1kΩ~10kΩ
MIC	B4	2.2 kΩ
		10 µF
ISET	A3	Resistor determine by Battery Charger
S_R	C4	220 µF(1)
S_L	B3	220 µF(1)
SCL	C2	1kΩ~10kΩ
SDA	B2	1kΩ~10kΩ
DM	B5	2.2Ω
		ESD Protection Diode
DP	C5	2.2Ω
		ESD Protection Diode
ID	D5	2.2Ω(1)
		ESD Protection Diode

(1) Optional Components

Schematic Guidelines

1. V_{BUS}, V_{DDIO}, & VBAT require 1µF~10µF and 0.1µF decoupling capacitors to reduce noise from circuit elements. The capacitors act as a shunt to block off the noise. The 0.1µF capacitor smoothes out high frequencies and has a lower series inductance. The 1µF~10µF capacitor smoothes out the lower frequencies and has a much higher series inductance. Placing both capacitors will provide better load regulation across the frequency spectrum.
2. OUT requires a 10µF load capacitor to prevent sudden increases of voltage on the pin during charging.
3. JIG is an open-drain output and therefore requires a 1kΩ ~ 10kΩ pull-up resistor to VBAT.
4. ISET is an open drain output. It can be used by the battery charger to set the input current limit with a series resistor (for example 75Ω determined by the charger).
5. SCL and SDA require 1kΩ ~ 10kΩ pull-up resistors to VDDIO to prevent floating inputs.
6. Depending on the codec used, S_R and S_L may require DC blocking capacitors as high as 220µF. The capacitor might not be needed if the codec has the capability to provide ground centered signals.
7. MIC requires a 2.2kΩ pull-up resistor to MIC_BIAS to provide DC bias for the microphone. Additionally the 10µF capacitor is required to block the DC signals from MIC_BIAS to the Audio Codec.
8. V_{BUS} , DM and DP are recommended to have an external resistor 2.2Ω to provide extra ballasting to protect the chip and internal circuitry.
   (a) For ID, if there is less stress on the ID pin then the external 2.2Ω resistor is optional.

9. DM, DP, and ID are rated for 6kV IEC contact discharge protection. To prevent failure in case of an IEC contact discharge greater than 6kV, it is recommended to have an external ESD Protection Diode (~1pF of capacitance allowed) rated for greater than 6kV IEC protection. It is also recommended to have an external ESD Protection Diode to prevent DP and DM from failure in the event of EOS related to electrical surge propagated downstream from the AC power supply.
10. V_{BUS} is rated for 6kV IEC contact discharge protection. To prevent failure in case of an IEC contact discharge greater than 6kV, it is recommended to have an external ESD Protection Diode (~1pF of capacitance allowed) rated for greater than 6kV IEC protection. It is also recommended to have an external ESD Protection Diode to prevent VBUS from failure in the event of EOS related to electrical surge propagated downstream from the AC power supply.

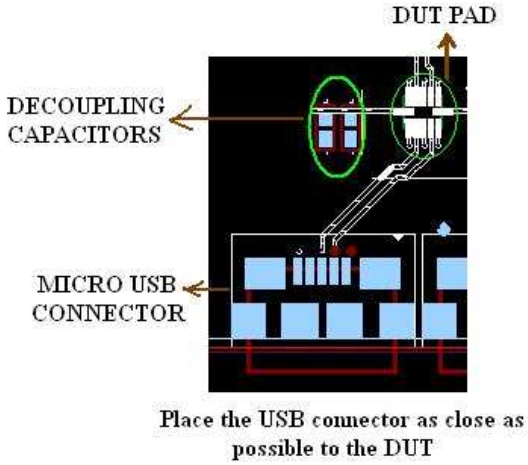
PCB Routing Guidelines

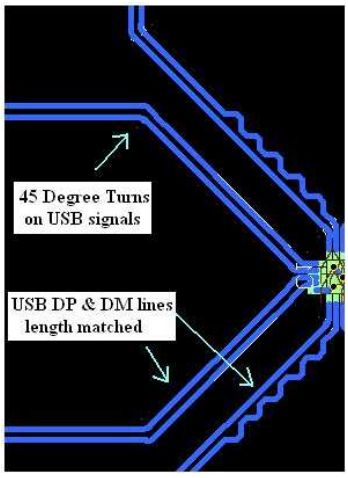
Routing Guidelines for USB Signal Integrity

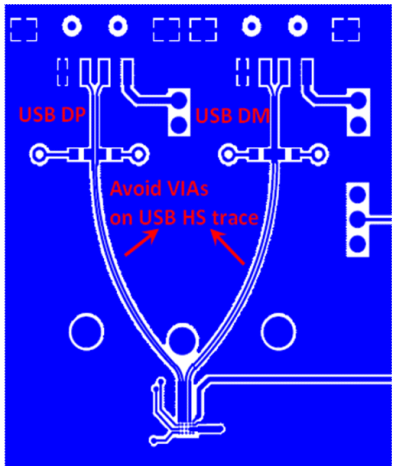
a. All the USB lines DP, DM, D+ & D-
   - Must have 45Ω single ended characteristic impedance
   - Must have 90Ω differential ended impedance
   - To fulfill USB 2.0 requirements

b. TSU6712 location
   - Close to the USB connector as possible
   - The distance between the USB controller and the device less than 1 inch
   - Shorter length of the trace will reduce effect of stray noise and radiate less EMI

c. Minimize use of VIAs for USB related signals
   - Differential transmission lines should be matched as close as possible
   - No VIAs for optimum USB2.0 performance







REVISION HISTORY

Changes from Original (May 2011) to Revision A	Page
• Removed all references of carkit from document.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSU6712YFPRB	ACTIVE	DSBGA	YFP	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	56N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

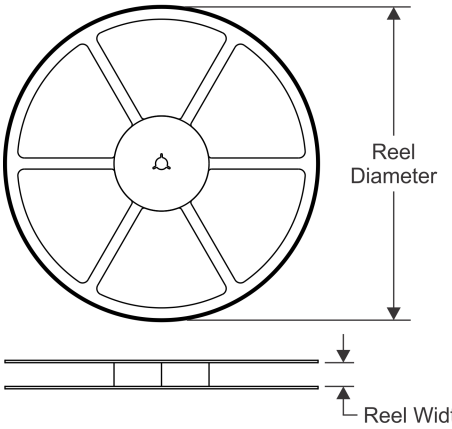
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

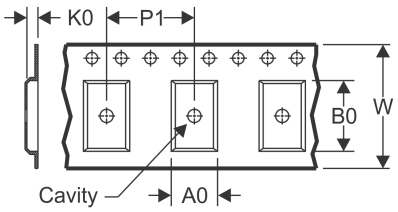
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

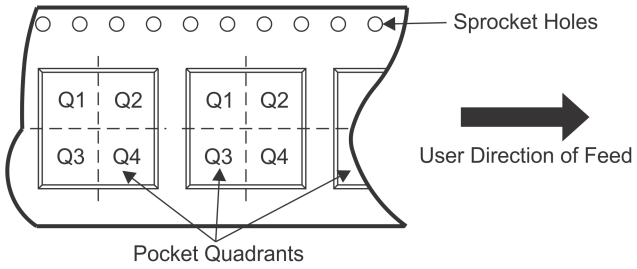


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

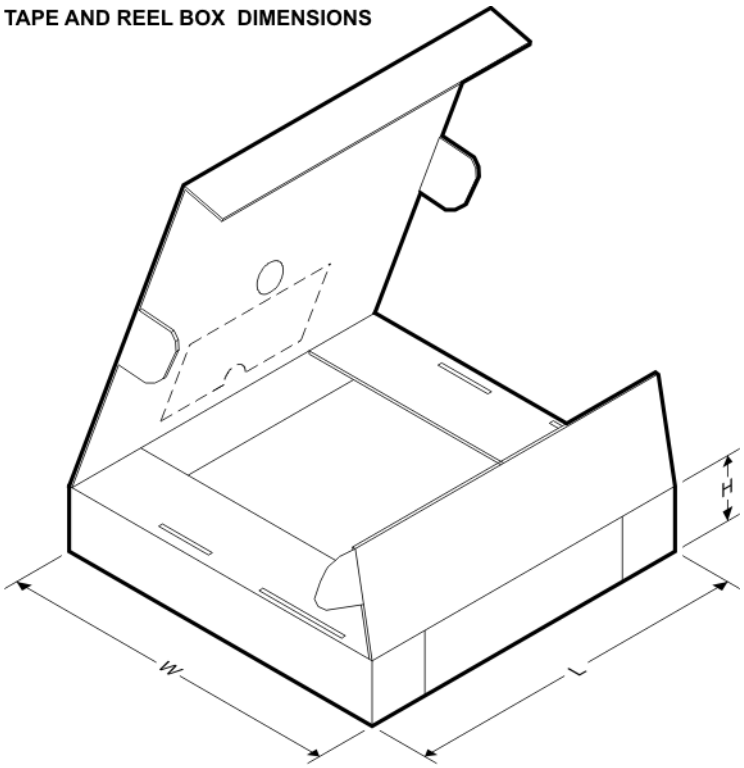
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSU6712YFPRB	DSBGA	YFP	25	3000	178.0	9.2	2.19	2.19	0.62	4.0	8.0	Q1

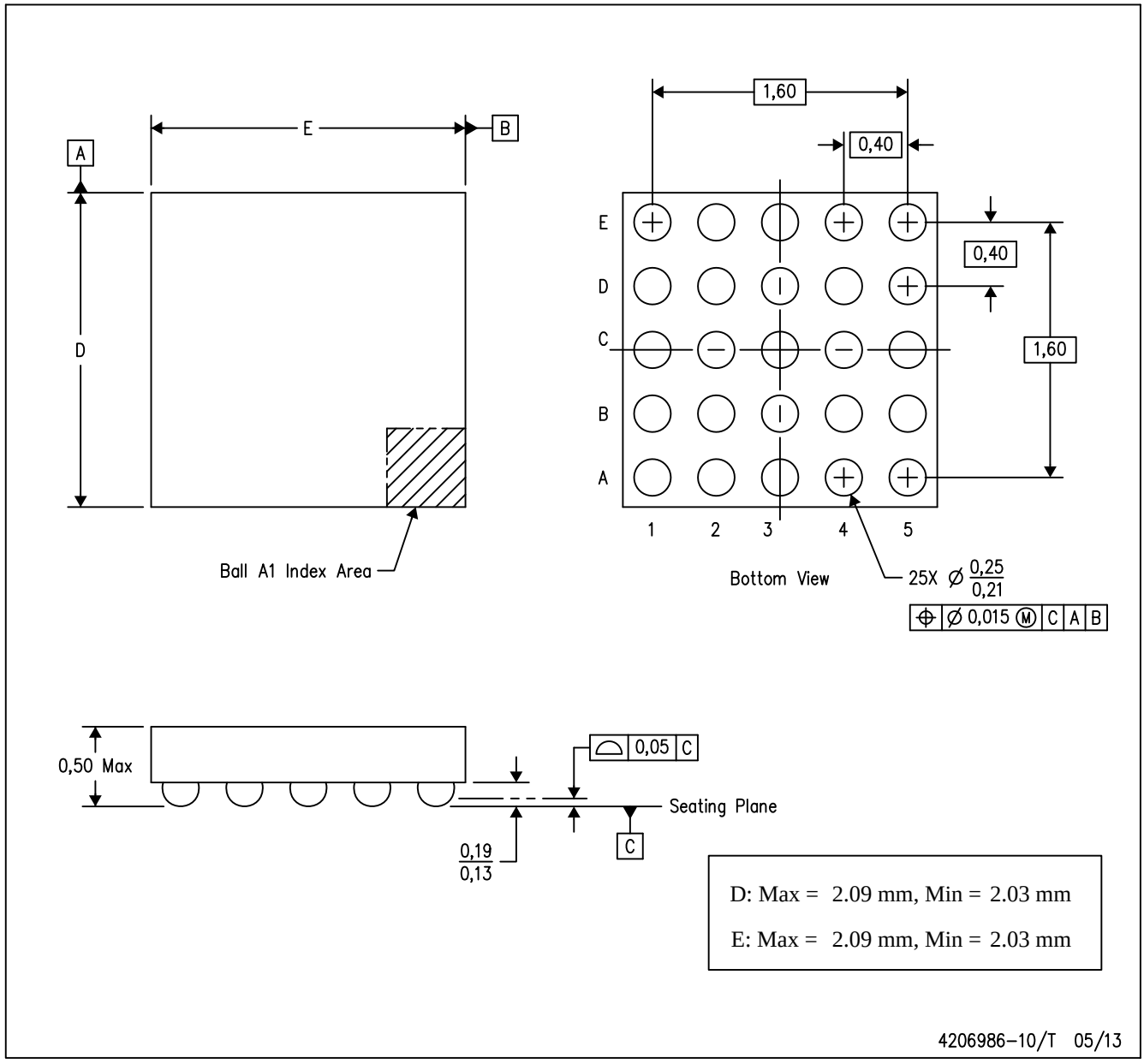
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSU6712YFPRB	DSBGA	YFP	25	3000	220.0	220.0	35.0

YFP (S–XBGA–N25) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265