DS90LV049H high temperature 3-V LVDS dual line driver and receiver pair

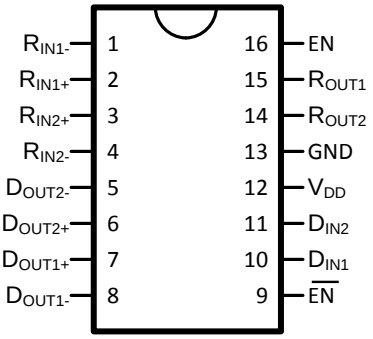
1 Features

- High Temperature +125°C Operating Range
- Up to 400-Mbps Switching Rates
- Flow-Through Pinout Simplifies PCB Layout
- 50-ps Typical Driver Channel-to-Channel Skew
- 50-ps Typical Receiver Channel-to-Channel Skew
- 3.3-V Single Power Supply Design
- TRI-STATE Output Control
- Internal Fail-Safe Biasing of Receiver Inputs
- Low Power Dissipation (70 mW at 3.3-V Static)
- High Impedance on LVDS Outputs on Power Down
- Conforms to TIA/EIA-644-A LVDS Standard
- Available in Low Profile 16-Pin TSSOP Package

2 Applications

- Board-to-Board Communication
- Test and Measurement
- Motor Drives
- LED Video Walls
- Wireless Infrastructure
- Telecom Infrastructure
- Multi-Function Printers
- NIC Cards
- Rack Servers
- Ultrasound Scanners

Dual-In-Line



3 Description

The DS90LV049H is a dual CMOS differential line driver-receiver pair designed for applications requiring ultra low power dissipation, exceptional noise immunity, and high data throughput. The device is designed to support data rates in excess of 400 Mbps utilizing Low Voltage Differential Signaling (LVDS) technology. The DS90LV049H TSSOP package allows for flow-through routing for easy PCB layout.

The DS90LV049H drivers accept LVTTL/LVCMOS signals and translate them to LVDS signals. The receivers accept LVDS signals and translate them to 3-V CMOS signals. The LVDS input buffers have internal fail-safe biasing that places the outputs to a known H (high) state for floating receiver inputs. In addition, the DS90LV049H supports a TRI-STATE function for a low idle power state when the device is not in use.

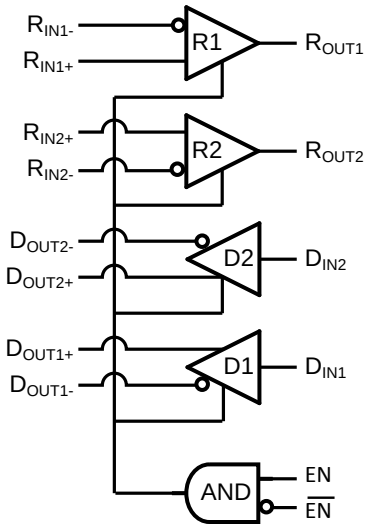
The EN and $\overline{EN}$ inputs are ANDed together and control the TRI-STATE outputs. The enables are common to all four gates.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90LV049H	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2013) to Revision B **Page**

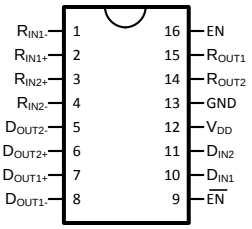
- Added *Device Information* table, *Device Comparison* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Added navigation links and removed the NRND banner at the top of the datasheet page ... 1
- Moved the thermal resistance (θ_{JA}) parameter in the *Absolute Maximum Ratings* table to the *Thermal Information* table ... 4

Changes from Original (April 2013) to Revision A **Page**

- Changed layout of National Data Sheet to TI format ... 17

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
D_{IN}	10, 11	I	Driver input pins, LVCMOS levels. There is a pulldown current source present.
D_{OUT+}	6, 7	O	Noninverting driver output pins, LVDS levels.
D_{OUT-}	5, 8	O	Inverting driver output pins, LVDS levels.
R_{IN+}	2, 3	I	Noninverting receiver input pins, LVDS levels. There is a pullup current source present.
R_{IN-}	1, 4	I	Inverting receiver input pins, LVDS levels. There is a pulldown current source present.
R_{OUT}	14, 15	O	Receiver output pins, LVCMOS levels.
EN, $\overline{EN}$	9, 16	I	Enable and Disable pins. There are pulldown current sources present at both pins.
V_{DD}	12	I	Power supply pin.
GND	13	I	Ground pin.

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

		MIN	MAX	UNIT
Supply Voltage (V_{DD})		−0.3	4	V
LVCMOS Input Voltage (D_{IN})		−0.3	(V_{DD} + 0.3)	V
LVDS Input Voltage (R_{IN+}, R_{IN-})		−0.3		V
Enable Input Voltage (EN, $\overline{EN}$)		−0.3	(V_{DD} + 0.3)	V
LVCMOS Output Voltage (R_{OUT})		−0.3	(V_{DD} + 0.3)	V
LVDS Output Voltage (D_{OUT+}, D_{OUT-})		−0.3	3.9	V
LVCMOS Output Short Circuit Current (R_{OUT})			100	mA
LVDS Output Short Circuit Current (D_{OUT+}, D_{OUT-})			24	mA
LVDS Output Short Circuit Current Duration (D_{OUT+}, D_{OUT-})		Continuous		
Lead Temperature Range	Soldering (4 sec.)		260	°C
Maximum Junction Temperature			150	°C
Maximum Package Power Dissipation at +25°C	PW0016A Package		866	mW
	Derate PW0016A Package (above +25°C)		6.9	mW/°C
Storage Temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] (1.5 kΩ, 100 pF)	7000	V
		(MM, 0 Ω, 200 pF)	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±7000 V may actually have higher performance.

6.3 Recommended Operating Conditions

	MIN	TYP	MAX	UNIT
Supply Voltage (V_{DD})	+3.0	+3.3	+3.6	V
Ambient Temperature (T_A)	−40	25	+125	°C
Junction Temperature (T_J)			+130	°C

6.4 Thermal Information

THERMAL METRIC[1]		DS90LV049H PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified.(1)(2)(3)

PARAMETER		TEST CONDITIONS	PIN	MIN	TYP	MAX	UNIT
LVCMOS Input DC Specifications (Driver Inputs, ENABLE Pins)							
V_{IH}	Input High Voltage		D_{IN} $\overline{EN}$ EN	2		V_{DD}	V
V_{IL}	Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	$V_{IN} = V_{DD}$		−10	1	+10	µA
I_{IL}	Input Low Current	V_{IN} = GND		−10	−0.1	+10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5	−0.6		V
LVDS Output DC Specifications (Driver Outputs)							
$\lvert V_{OD} \rvert$	Differential Output Voltage	R_L = 100 Ω (Figure 2)	D_{OUT-} D_{OUT+}	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States				1	35	|mV|
V_{OS}	Offset Voltage			1.125	1.23	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				1	25	|mV|
I_{OS}	Output Short-Circuit Current(4)	ENABLED, $D_{IN} = V_{DD}$, D_{OUT+} = 0 V or D_{IN} = GND, D_{OUT-} = 0 V			−5.8	−9	mA
I_{OSD}	Differential Output Short-Circuit Current(4)	ENABLED, V_{OD} = 0 V			−5.8	−9	mA
I_{OFF}	Power-off Leakage	V_{OUT} = 0 V or 3.6 V, V_{DD} = 0 V or Open		−20	±1	+20	µA
I_{OZ}	Output TRI-STATE Current	EN = 0 V and $\overline{EN}$ = V_{DD}, V_{OUT} = 0 V or V_{DD}		−10	±1	+10	µA
LVDS Input DC Specifications (Receiver Inputs)							
V_{TH}	Differential Input High Threshold	V_{CM} = 1.2 V, 0.05 V, 2.35 V	R_{IN+} R_{IN-}		−15	35	mV
V_{TL}	Differential Input Low Threshold			–100	−15		mV
V_{CMR}	Common-Mode Voltage Range	V_{ID} = 100 mV, V_{DD}=3.3 V		0.05		3	V
I_{IN}	Input Current	V_{DD}=3.6 V, V_{IN} =0 V or 2.8 V		−12	±4	+12	µA
		V_{DD}=0 V, V_{IN} =0 V or 2.8 V or 3.6 V		−10	±1	+10	µA
LVCMOS Output DC Specifications (Receiver Outputs)							
V_{OH}	Output High Voltage	I_{OH} = -0.4 mA, V_{ID}= 200 mV	R_{OUT}	2.7	3.3		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = 200 mV			0.05	0.25	V
I_{OZ}	Output TRI-STATE Current	Disabled, V_{OUT} =0 V or V_{DD}		–10	±1	+10	µA
General DC Specifications							
I_{DD}	Power Supply Current(5)	EN = 3.3 V	V_{DD}		21	35	mA
I_{DDZ}	TRI-State Supply Current	EN = 0 V			15	25	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{TH}, V_{TL}, V_{OD} and ΔV_{OD}.
(2) All typical values are given for: V_{DD} = +3.3 V, T_A = +25°C.
(3) The DS90LV049H's drivers are current mode devices and only function within datasheet specifications when a resistive load is applied to their outputs. The typical range of the resistor values is 90 Ω to 110 Ω.
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.
(5) Both driver and receiver inputs are static. All LVDS outputs have 100 Ω load. All LVCMOS outputs are floating. None of the outputs have any lumped capacitive load.

6.6 Switching Characteristics

V_{DD} = +3.3V ± 10%, T_A = −40°C to +125°C(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS Outputs (Driver Outputs)						
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100 Ω (Figure 3 and Figure 4)		0.7	2	ns
t_{PLHD}	Differential Propagation Delay Low to High			0.7	2	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$(3)(4)		0	0.05	0.4	ns
t_{SKD2}	Differential Channel-to-Channel Skew(3)(5)		0	0.05	0.5	ns
t_{SKD3}	Differential Part-to-Part Skew(3)(6)		0		1	ns
t_{TLH}	Rise Time(3)		0.2	0.4	1	ns
t_{THL}	Fall Time(3)		0.2	0.4	1	ns
t_{PHZ}	Disable Time High to Z	R_L = 100 Ω (Figure 5 and Figure 6)		1.5	3	ns
t_{PLZ}	Disable Time Low to Z			1.5	3	ns
t_{PZH}	Enable Time Z to High		1	3	6	ns
t_{PZL}	Enable Time Z to Low		1	3	6	ns
f_{MAX}	Maximum Operating Frequency(7)		200	250		MHz
LVCMOS Outputs (Receiver Outputs)						
t_{PHL}	Propagation Delay High to Low	(Figure 7 and Figure 8)	0.5	2	3.5	ns
t_{PLH}	Propagation Delay Low to High		0.5	2	3.5	ns
t_{SK1}	Pulse Skew $\|t_{PHL} - t_{PLH}\|$(8)		0	0.05	0.4	ns
t_{SK2}	Channel-to-Channel Skew(9)		0	0.05	0.5	ns
t_{SK3}	Part-to-Part Skew(10)		0		1	ns
t_{TLH}	Rise Time(3)		0.3	0.9	1.4	ns
t_{THL}	Fall Time(3)		0.3	0.75	1.4	ns
t_{PHZ}	Disable Time High to Z	(Figure 9 and Figure 10)	3	5.6	8	ns
t_{PLZ}	Disable Time Low to Z		3	5.4	8	ns
t_{PZH}	Enable Time Z to High		2.5	4.6	7	ns
t_{PZL}	Enable Time Z to Low		2.5	4.6	7	ns
f_{MAX}	Maximum Operating Frequency(11)		200	250		MHz

(1) All typical values are given for: V_{DD} = +3.3 V, T_A = +25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, and t_f ≤ 1 ns.
(3) These parameters are specified by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage, temperature) ranges.
(4) t_{SKD1} or differential pulse skew is defined as $|t_{PHLD} - t_{PLHD}|$. It is the magnitude difference in the differential propagation delays between the positive going edge and the negative going edge of the same driver channel.
(5) t_{SKD2} or differential channel-to-channel skew is defined as the magnitude difference in the differential propagation delays between two driver channels on the same device.
(6) t_{SKD3} or differential part-to-part skew is defined as $|t_{PLHD\ Max} - t_{PLHD\ Min}|$ or $|t_{PHLD\ Max} - t_{PHLD\ Min}|$. It is the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.
(7) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output Criteria: duty cycle = 45%/55%, V_{OD} > 250 mV, all channels switching.
(8) t_{SK1} or pulse skew is defined as $|t_{PHL} - t_{PLH}|$. It is the magnitude difference in the propagation delays between the positive going edge and the negative going edge of the same receiver channel.
(9) t_{SK2} or channel-to-channel skew is defined as the magnitude difference in the propagation delays between two receiver channels on the same device.
(10) t_{SK3} or part-to-part skew is defined as $|t_{PLH\ Max} - t_{PLH\ Min}|$ or $|t_{PHL\ Max} - t_{PHL\ Min}|$. It is the difference between the minimum and maximum specified propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.
(11) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, V_{ID} = 200 mV, V_{CM} = 1.2 V . Output Criteria: duty cycle = 45%/55%, V_{OH} > 2.7 V, V_{OL} < 0.25 V, all channels switching.

6.7 Typical Characteristics

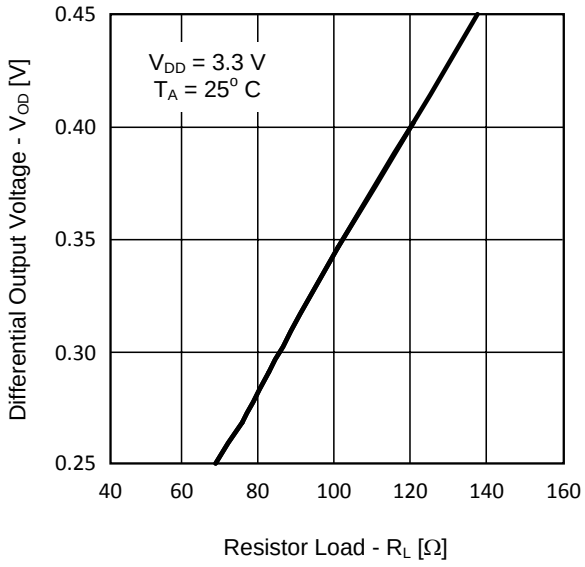


Figure 1. Differential Output Voltage vs Load Resistor

7 Parameter Measurement Information

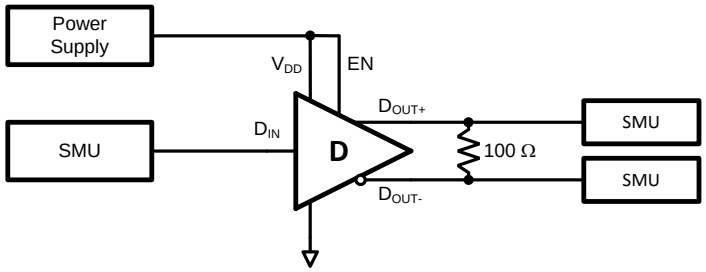


Figure 2. Driver V_{OD} and V_{OS} Test Circuit

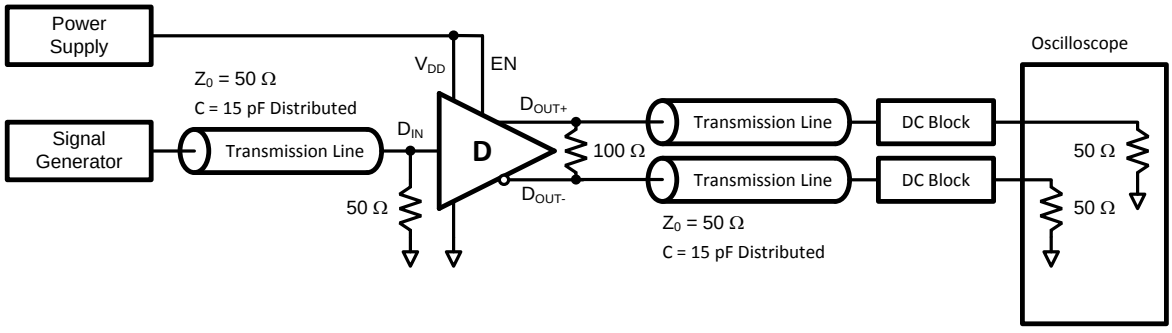


Figure 3. Driver Propagation Delay and Transition Time Test Circuit

Parameter Measurement Information (continued)

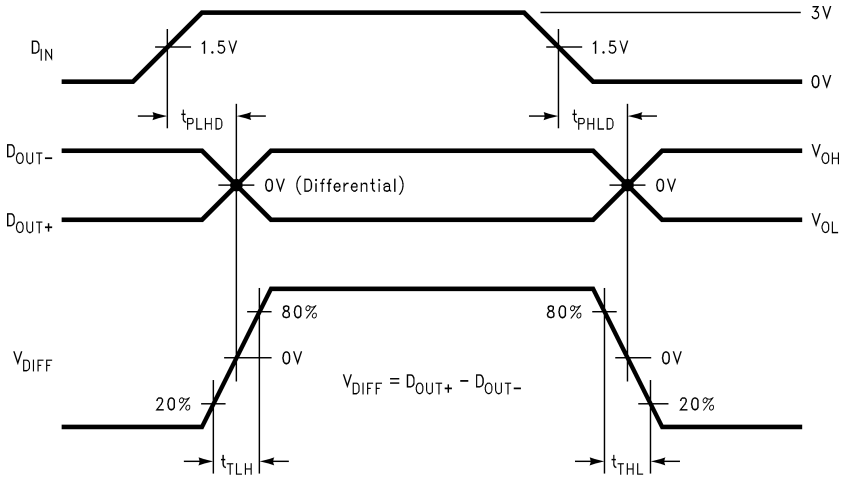


Figure 4. Driver Propagation Delay and Transition Time Waveforms

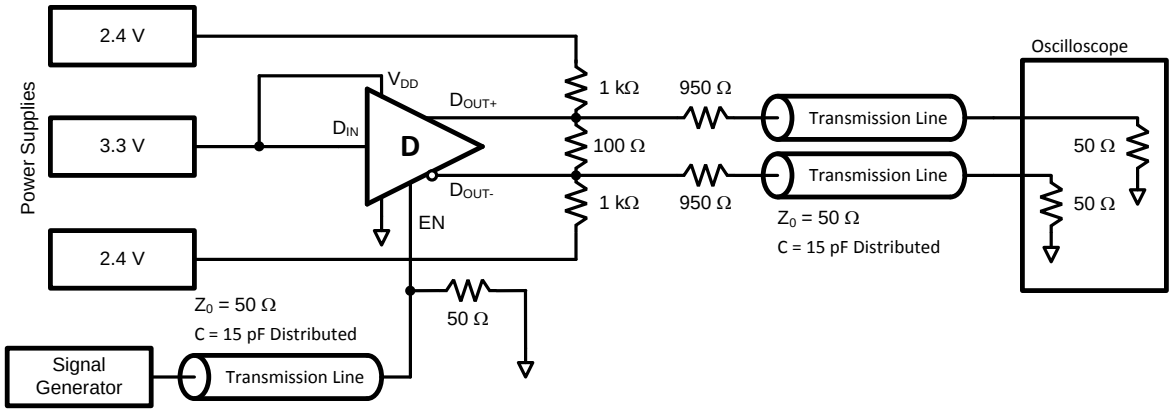


Figure 5. Driver TRI-STATE Delay Test Circuit

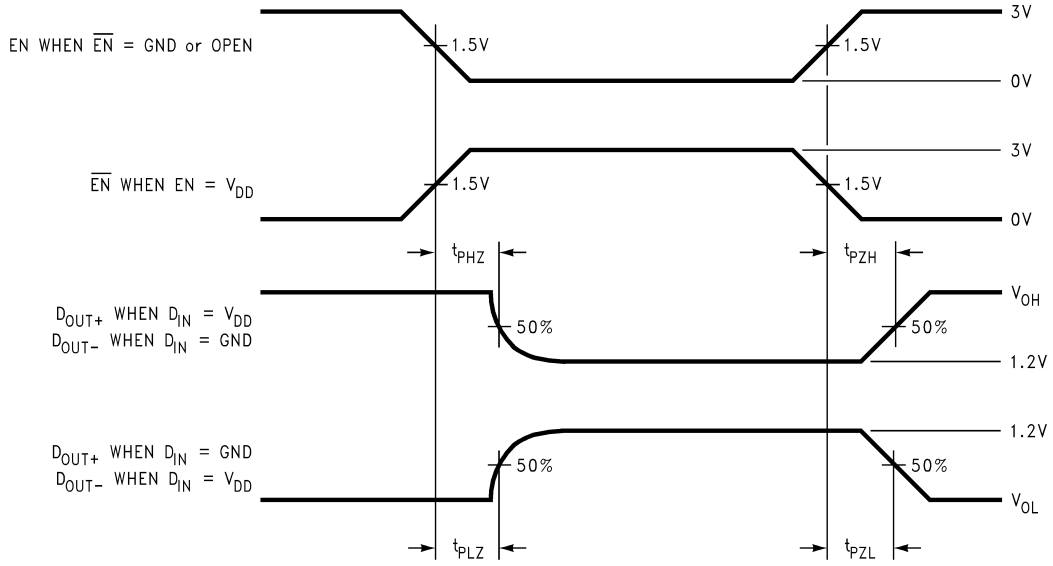


Figure 6. Driver TRI-STATE Delay Waveform

Parameter Measurement Information (continued)

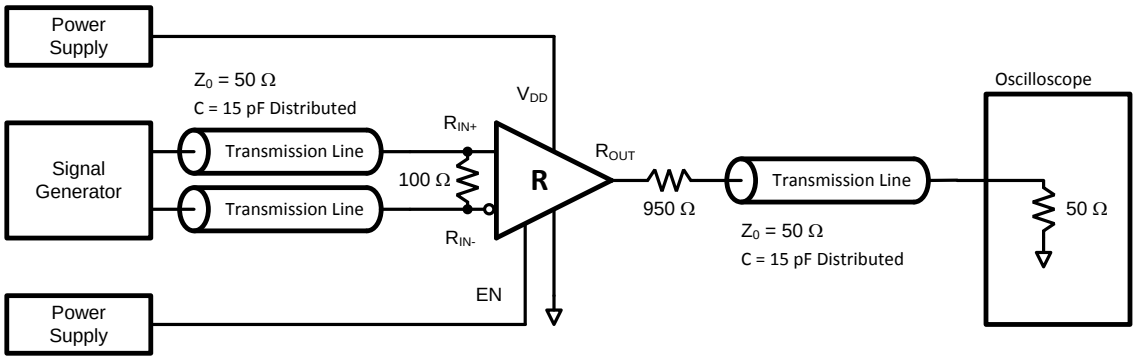


Figure 7. Receiver Propagation Delay and Transition Time Test Circuit

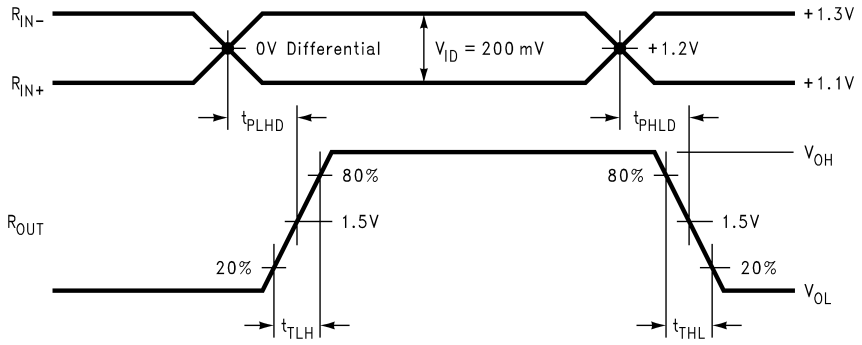


Figure 8. Receiver Propagation Delay and Transition Time Waveforms

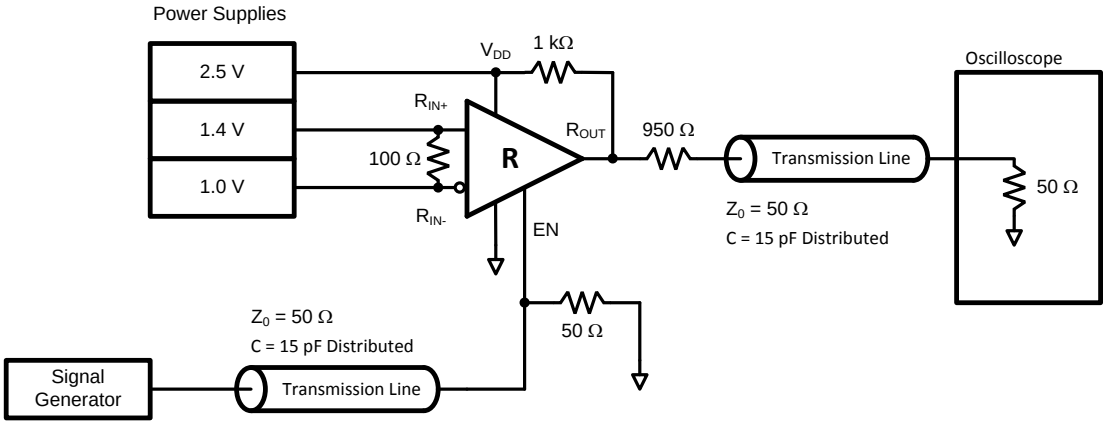


Figure 9. Receiver TRI-STATE Delay Test Circuit

Parameter Measurement Information (continued)

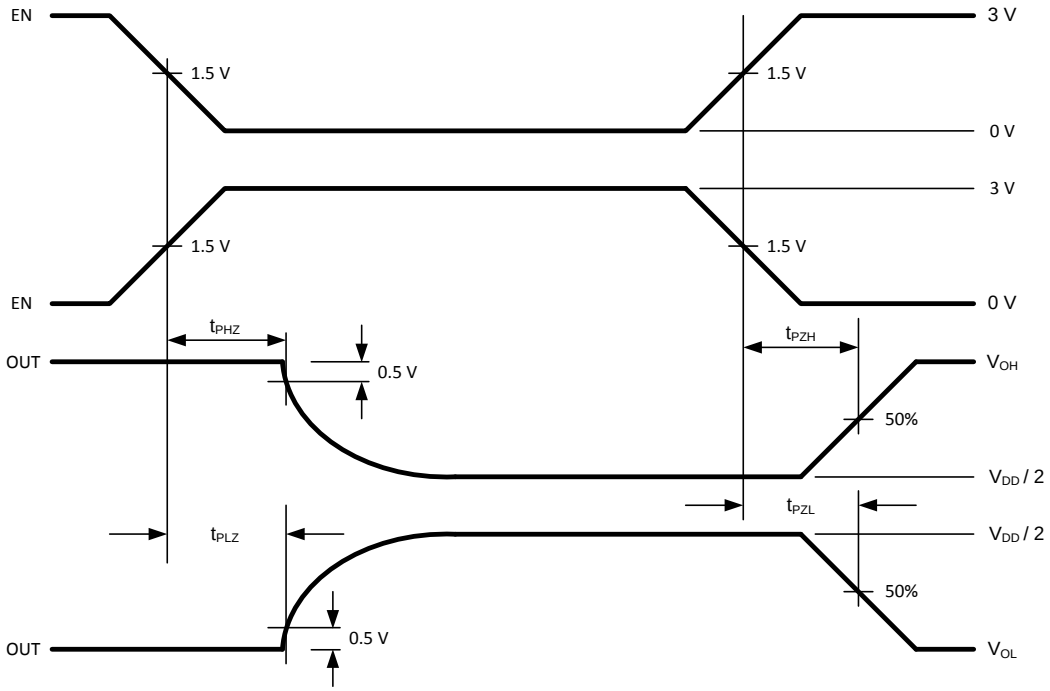


Figure 10. Receiver TRI-STATE Delay Waveforms

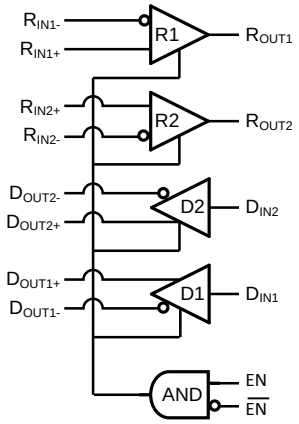
8 Detailed Description

8.1 Overview

The DS90LV049H integrates both low-voltage differential signaling (LVDS) line drivers, with a balanced current source design, and LVDS line receivers into a single package. This device operates from a single power supply that is nominally 3.3 V, but the supply can be as low as 3.0 V and as high as 3.6 V. The input signal to the DS90LV049H LVDS line drivers is an LVCMOS/LVTTL signal. The output of the DS90LV049H LVDS line drivers is a differential signal complying with the LVDS standard (TIA/EIA-644). The input to the DS90LV049H LVDS line receivers is a differential signal complying with the LVDS Standard (TIA/EIA-644) and the output is a 3.3-V LVCMOS/LVTTL signal. The differential output signal of the DS90LV049H LVDS line drivers operates with a signal level of 350 mV, nominally, at a common-mode voltage of 1.2 V. This low differential output voltage results in low electromagnetic interference (EMI). The differential input signal of the DS90LV049H LVDS line receivers operates with a signal level of 350 mV, nominally, at a common-mode voltage of 1.2 V. The differential nature of the LVDS outputs and inputs provides immunity to common-mode coupled signals (noise) that the driven/received signal may experience.

The DS90LV049H is primarily used in point-to-point configurations, as seen in Figure 11. This configuration provides a clean signaling environment for the fast edge rates of the DS90LV049H and other LVDS components. The DS90LV049H is connected through a balanced media which may be a standard twisted-pair cable, a parallel pair cable, or simply PCB traces to a LVDS receiver. Typically, the characteristic differential impedance of the media is in the range of 100 Ω. The DS90LV049H device is intended to drive a 100-Ω transmission line. The 100-Ω termination resistor is selected to match the media and is placed as close to the LVDS receiver input pins as possible.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DS90LV049H LVDS Driver and Receiver Functionality

Table 1 shows how the LVDS driver single-ended input to differential output relationship is defined for DS90LV049H. When the driver input is left open, the differential output is undefined.

Table 1. DS90LV049H LVDS Driver Functionality(1)

INPUT	OUTPUT	
D_{INx}	D_{OUTx+}	D_{OUTx-}
H	H	L
L	L	H
Open	?	?

(1) x = 1,2 to indicate pin designation.

Table 2 shows how the LVDS receiver differential input to single-ended output relationship is defined for DS90LV049H. The DS90LV049H receiver is capable of detecting signals as low as 100 mV, over a ±1-V common-mode range centered around 1.2 V.

Table 2. DS90LV049H LVDS Receiver Functionality(1)

INPUTS	OUTPUT
$V_{ID} = [R_{INx+}] - [R_{INx-}]$	R_{OUTx}
$V_{ID} \geq 0$ V	H
$V_{ID} \leq -0.1$ V	L
Full Fail-Safe OPEN/SHORT or Terminated	H

(1) x = 1,2 to indicate pin designation.

8.3.2 Termination

Use a termination resistor that best matches the differential impedance or the transmission line. The resistor should be between 90 Ω and 130 Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10 mm (12 mm MAX).

8.3.3 Fail-Safe Feature

The LVDS receiver is a high-gain, high-speed device that amplifies a small differential signal (20 mV) to LVCMOS/LVTTL logic levels. Due to the high gain and tight threshold of the receiver, take care to prevent noise from appearing as a valid signal. The internal fail-safe circuitry of the receiver is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated, or shorted receiver inputs.

1. **Open Input Pins**: It is not required to tie the receiver inputs to ground or any supply voltage. Internal fail-safe circuitry will ensure a HIGH, stable output state for open inputs.
2. **Terminated Input**: If the driver is disconnected (cable unplugged), or if the driver is in a power-off condition, the receiver output will again be in a HIGH state, even with the end cable 100-Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10 mV of differential noise, the receiver may see the noise as a valid signal and switch. To ensure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. A twisted-pair cable will offer better balance than a flat ribbon cable.
3. **Shorted Inputs**: If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0-V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4 V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pullup and pulldown resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pullup and pulldown resistors should be in the 5-kΩ to 15-kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2 V (less than 1.75 V) to be compatible with the internal circuitry. The DS90LV049H is compliant to the original ANSI EIA/TIA-644 specification and is also compliant to the new ANSI EIA/TIA-644-A specification with the exception of the newly added ΔIIN specification. Due to the internal fail-safe circuitry, ΔIIN cannot meet the 6-μA maximum specified. This exception will not be relevant unless more than 10 receivers are used.

Additional information on the fail-safe biasing of LVDS devices may be found in *AN-1194 Fail-Safe Biasing of LVDS Interfaces* (SNLA051).

8.4 Device Functional Modes

Table 3 reflects the functional state of DS90LV049H when EN and $\overline{EN}$ change state.

Table 3. DS90LV049H Functional Modes

EN	$\overline{EN}$	LVDS Out	LVCMOS Out
L or Open	L or Open	OFF	OFF
H	L or Open	ON	ON
L or Open	H	OFF	OFF
H	H	OFF	

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

LVDS drivers and receivers are intended to be used primarily in a point-to-point configurations as is shown in Figure 11. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media that may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic differential impedance of the media is in the range of 100 Ω. A termination resistor of 100 Ω (selected to match the media), and is placed as close to the receiver input pins as possible. The termination resistor converts the driver output current (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account. The TRI-STATE function allows the device outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required. The DS90LV049H has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device allow for easy matching of the electrical lengths for the differential pair trace lines between the driver and the receiver, and the signal placement allows the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

9.2 Typical Application

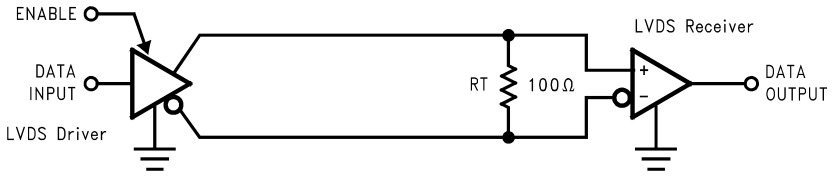


Figure 11. Point-to-Point Application

9.2.1 Design Requirements

Table 4 lists the design parameters for this example.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply Voltage (V_{DD})	3 to 3.6 V
Single-ended Input Voltage	0 to V_{DD}
Signaling Rate 1 Ground shift between driver and receiver	0 to 400 Mbps
Interconnect Characteristic Impedance	100 Ω
Number of LVDS Channel	4
Number of Receiver/Transmitter Nodes	2
Ground shift between driver and receiver	±1 V

9.2.2 Detailed Design Procedure

9.2.2.1 Power Decoupling Recommendations

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1-μF and 0.001-μF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin.

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 μF to 1000 μF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one must resort to the use of smaller capacitors (nF to μF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by Equation 1 and Equation 2 according to Johnson(1) equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV. However, this figure varies depending on the noise budget available in the design. (1)

$$C_{chip} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \tag{1}$$

$$C_{LVDS} = \left(\frac{1A}{0.2V} \right) \times 200\ ps = 0.001\ \mu F \tag{2}$$

Figure 12 lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 μF) and the value of capacitance found above (0.001 μF). TI recommends that the user place the smallest value of capacitance as close to the chip as possible.

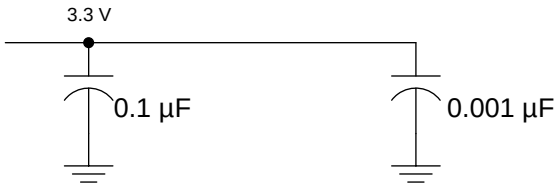


Figure 12. Recommended LVDS Bypass Capacitor Layout

9.2.2.2 PCB Transmission Lines

As per the *LVDS Owner's Manual Design Guide, 4th Edition* (SNLA187), Figure 13 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and return path with a uniform cross section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. Figure 13 shows examples of edge-coupled microstrip lines, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent (like if S is less than 2 W, for example), the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

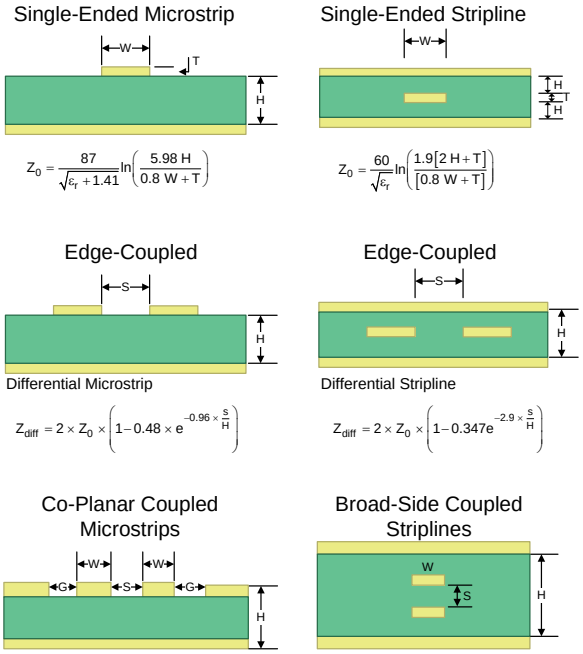


Figure 13. Controlled-Impedance Transmission Lines

9.2.2.3 Input Fail-Safe Biasing

External pullup and pulldown resistors may be used to provide enough of an offset to enable an input fail-safe under open-circuit conditions. This configuration ties the positive LVDS input pin to VDD through a pullup resistor, and the negative LVDS input pin is tied to GND by a pulldown resistor. The pullup and pulldown resistors should be in the 5 kΩ to 15 kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should ideally be set to approximately 1.2 V (less than 1.75 V) to be compatible with the internal circuitry. Refer to application note *AN-1194 Fail-Safe Biasing of LVDS Interfaces* (SNLA051) for more information.

9.2.2.4 Probing LVDS Transmission Lines on PCB

Always use high impedance (> 100 kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will skew results.

9.2.2.5 Interconnecting Media

The physical communication channel between the LVDS driver and the LVDS receiver may be any balanced and paired metal conductors meeting the requirements of the LVDS standard, the key points of which are included here. This media may be twisted-pair, twinax cables, flat ribbon cables, or PCB traces. The nominal characteristic impedance of the interconnect media should be between 100 Ω and 120 Ω with a variation of no more than 10% (90 Ω to 132 Ω). Balanced cables (for example, twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax.) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver. There should not introduce major impedance discontinuities in the system.

9.2.3 Application Curve

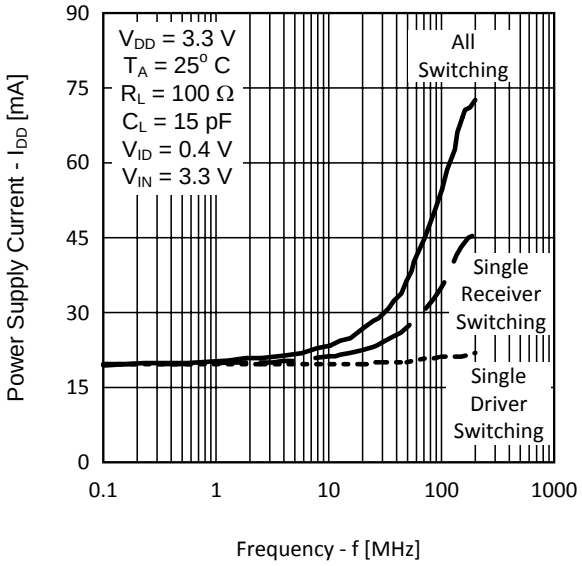


Figure 14. Power Supply Current vs Frequency

10 Power Supply Recommendations

The DS90LV049H LVDS transceiver is designed to operate from a single power supply with supply voltage in the range of 3.0 V to 3.6 V. In a typical point-to-point application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the driver power supply would be less than |±1 V|. Board level and local device level bypass capacitance should be used.

11 Layout

11.1 Layout Guidelines

11.1.1 Microstrip vs. Stripline Topologies

As per the *LVDS Application and Data Handbook* (SLLD009), printed-circuit boards usually offer designers two transmission line options: microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 15.

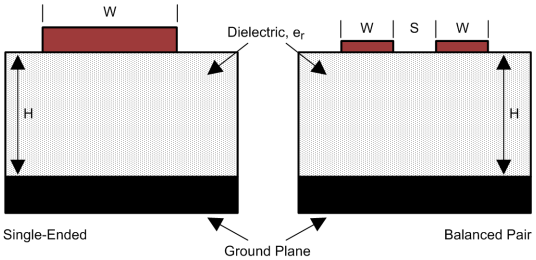


Figure 15. Microstrip Topology

Layout Guidelines (continued)

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines when possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1[(2)], 2[(3)], and 3[(4)] provide formulas for Z_O and t_{PD} for differential and single-ended traces. (2) (3) (4)

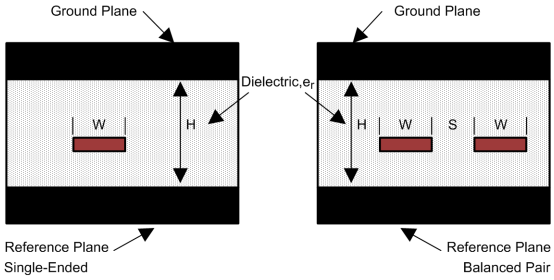


Figure 16. Stripline Topology

11.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of LVCMOS/LVTTL signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 may be desired. When the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 μm or 0.0003 in (minimum).
- Copper plating should be 25.4 μm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

11.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, the designer must decide how many levels to use in the stack. To reduce the LVCMOS/LVTTL to LVDS crosstalk, it is good practice to have at least two separate signal planes as shown in Figure 17.

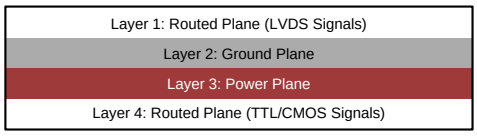


Figure 17. Four-Layer PCB Board

NOTE

The separation between layers 2 and 3 should be 127 μm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

(2) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(3) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(4) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

Layout Guidelines (continued)

One of the most common stack configurations is the six-layer board, as shown in Figure 18.

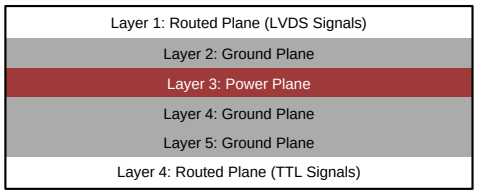


Figure 18. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity, but fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes in addition to ensuring reference to a ground plane for signal layers 1 and 6.

11.1.4 Separation Between Traces

The separation between traces depends on several factors, but the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

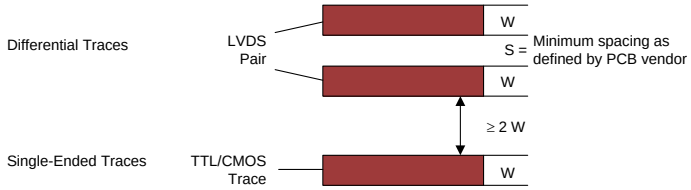


Figure 19. 3-W Rule for Single-Ended and Differential Traces (Top View)

Exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

11.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close to its originating trace as possible. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

11.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. TI recommends that the user place a via immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

Layout Guidelines (continued)

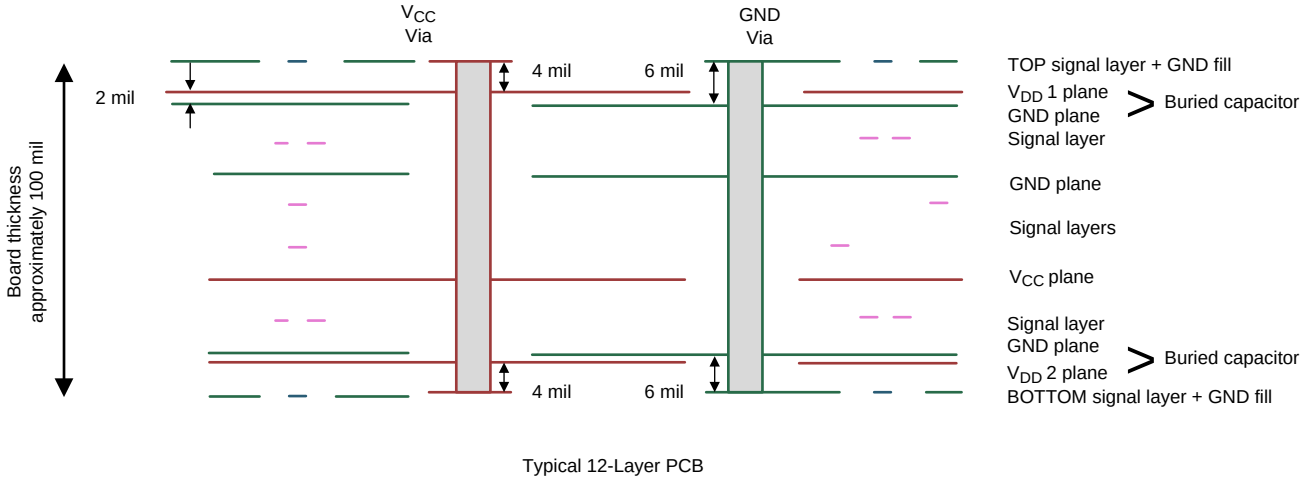


Figure 20. Low Inductance, High-Capacitance Power Connection

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402 or even 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in Figure 21(a).

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 μF, and 0.1 μF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Refer back to Figure 13 for some examples. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center dap must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the dap connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in Figure 13) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases the GND dap that is so important for heat dissipation makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-dap spacing as shown in Figure 21(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.

Figure 21. Typical Decoupling Capacitor Layouts

Layout Guidelines (continued)

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 22.

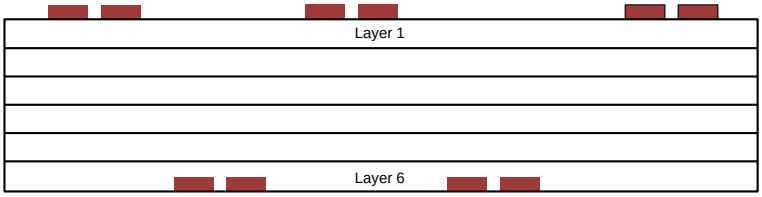


Figure 22. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers. Thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 23. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

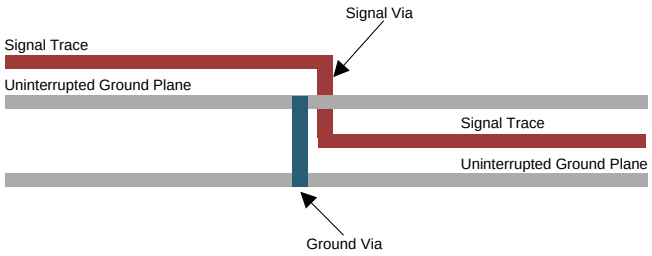


Figure 23. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

11.2 Layout Example

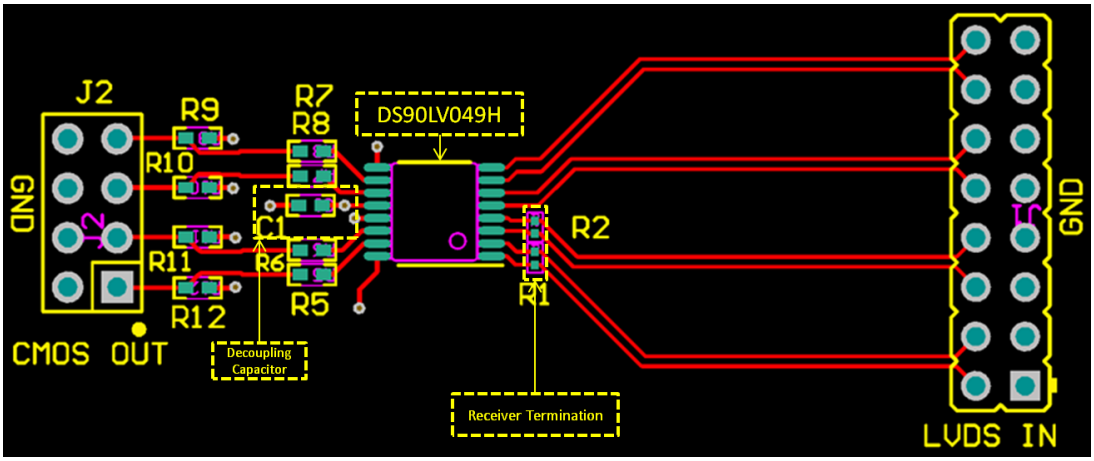


Figure 24. Example DS90LV049H Layout

12 Device and Documentation Support

12.1 Related Documentation

For related documentation, see the following:

- *LVDS Owner's Manual* (SNLA187)
- *AN-808 Long Transmission Lines and Data Signal Quality* (SNLA028)
- *AN-977 LVDS Signal Quality: Jitter Measurements Using Eye Patterns Test Report #1* (SNLA166)
- *AN-971 An Overview of LVDS Technology* (SNLA165)
- *AN-916 A Practical Guide to Cable Selection* (SNLA219)
- *AN-805 Calculating Power Dissipation for Differential Line Drivers* (SNOA233)
- *AN-903 A Comparison of Differential Termination Techniques* (SNLA034)
- *AN-1194 Fail-Safe Biasing of LVDS Interfaces* (SNLA051)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
Rogers is a trademark of Rogers Corporation.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV049HMT/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	90LV049 HMT	Samples
DS90LV049HMTX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	90LV049 HMT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

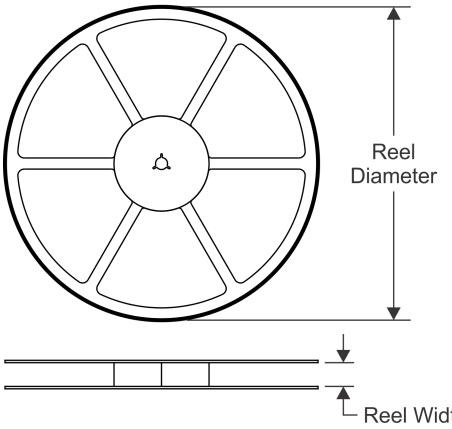
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

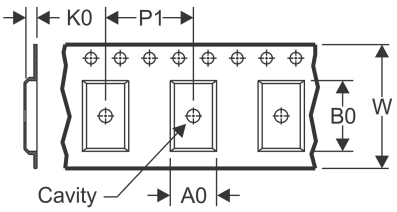
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

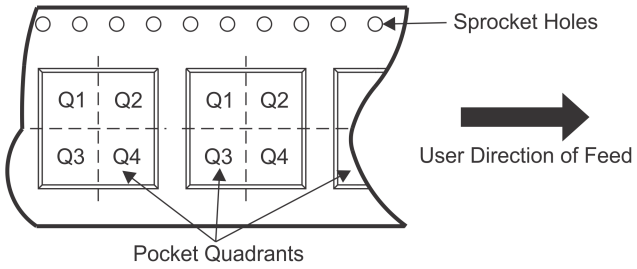


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

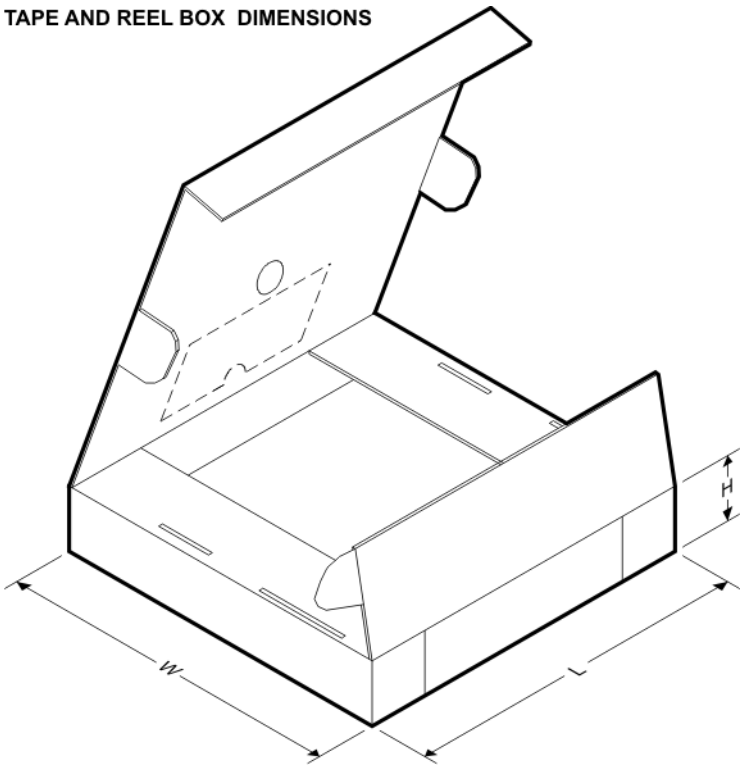
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV049HMTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

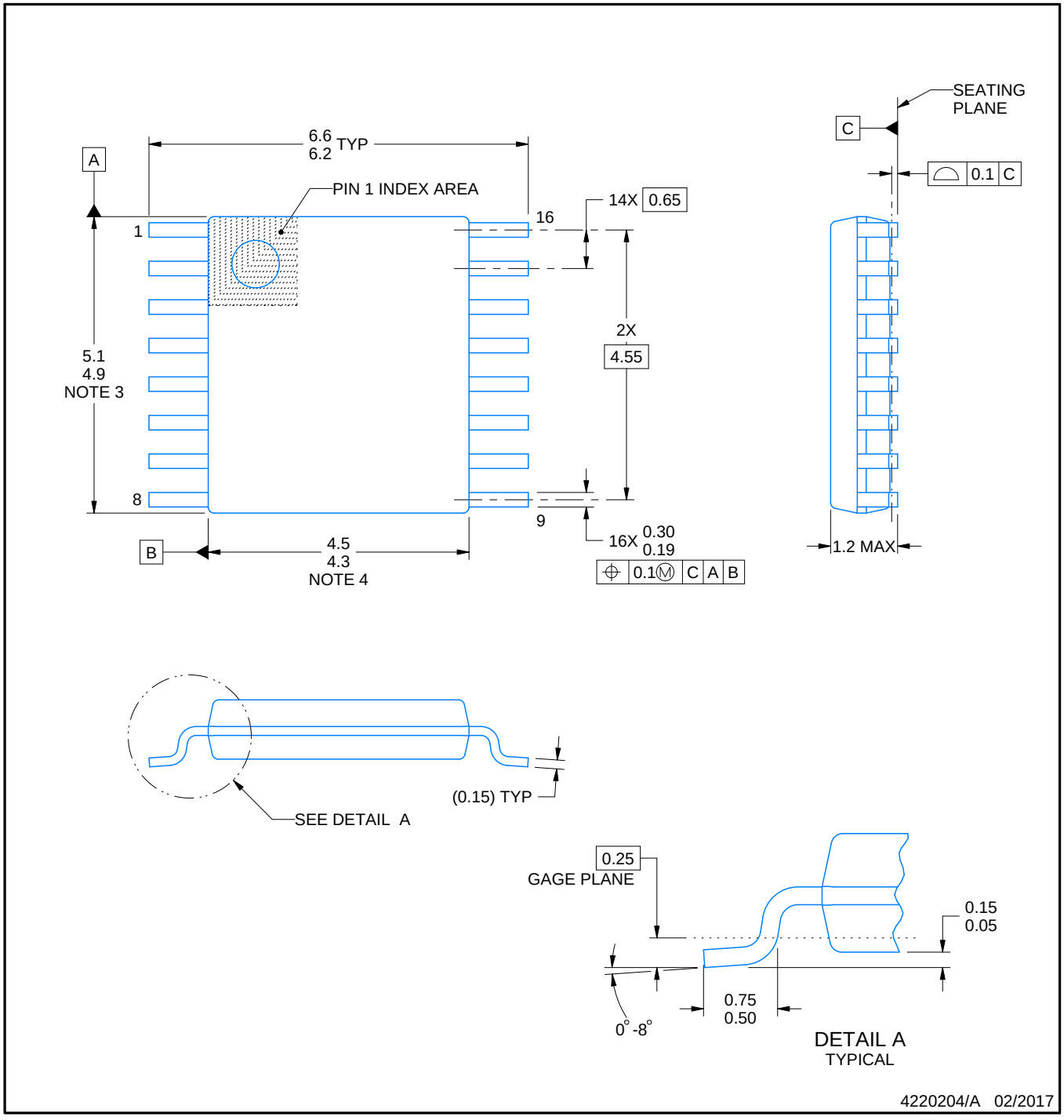
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV049HMTX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0

PACKAGE OUTLINE

PW0016A

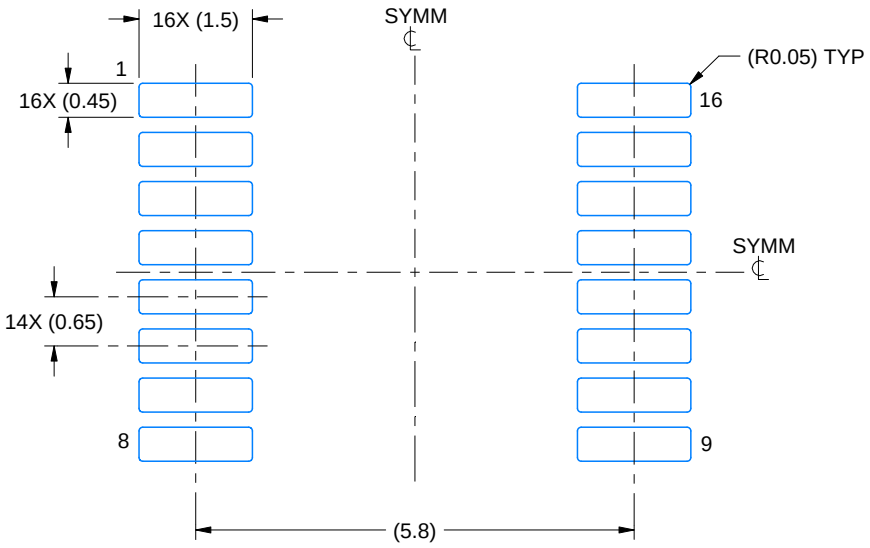
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

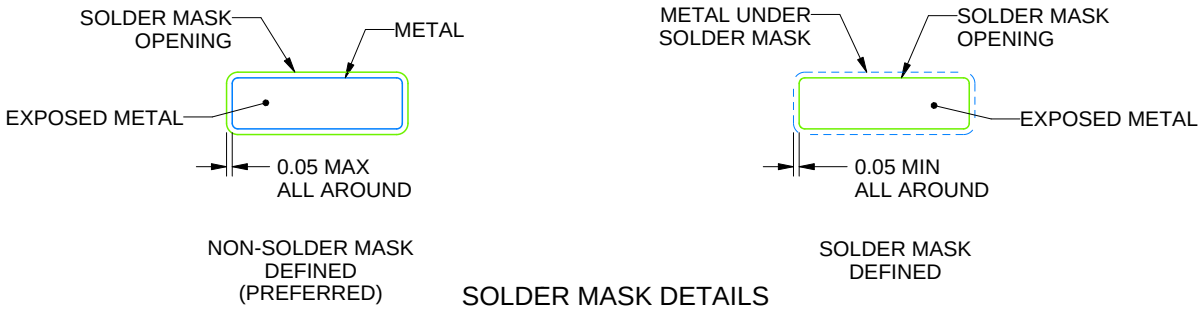


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

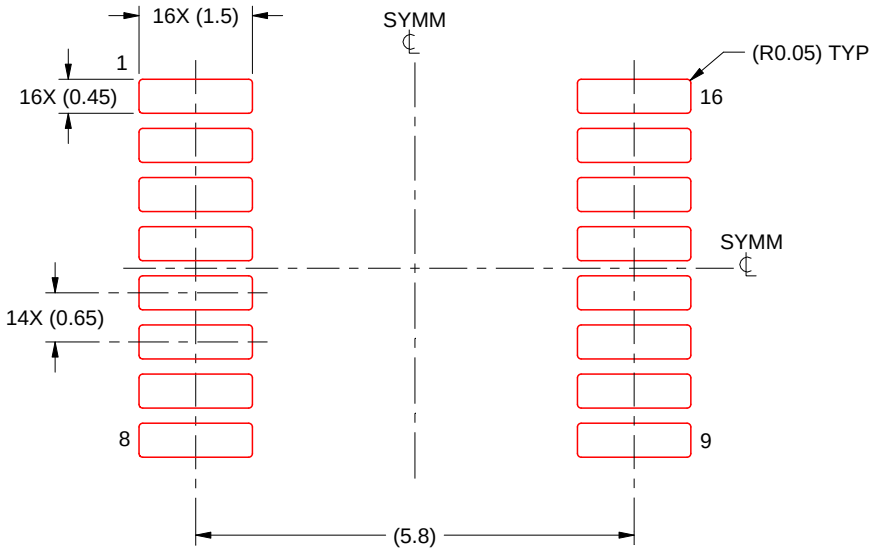


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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