

16-Channel, 12-Bit, ES-PWM, Full Self-Diagnosis LED Driver for 7-Bit Global BC LED Lamp

Check for Samples: [TLC5949](#)

FEATURES

- 16 Constant-Current Sink Output Channels
- Sink Current Capability with Maximum BC Data: 2 mA to 45 mA
- Global Brightness Control (BC):
 - 7-Bit (128 Steps) with 25% to 100% Range
- Grayscale Control (GS) with Enhanced Spectrum or Conventional PWM:
 - 12-Bit (4096 Steps)
- LED Power-Supply Voltage: Up to 10 V
- VCC: 3.0 V to 3.6 V
- Constant-Current Accuracy:
 - Channel-to-Channel: $\pm 0.6\%$ (typ), $\pm 2\%$ (max)
 - Device-to-Device: $\pm 1\%$ (typ), $\pm 4\%$ (max)
- Data Transfer Rate: 33 MHz
- Grayscale Control Clock: 33 MHz
- Auto Display Repeat and Auto Data Refresh
- Display Timing Reset
- Power-Save Mode to Minimize VCC Current
- LOD and LSD with Invisible Detection Mode (IDM)
- Output Leakage Detection (OLD)
- Current Reference Terminal Short Flag (ISF)
- Thermal Shutdown (TSD) and Error Flag (TEF)

- Pre-Thermal Warning (PTW)
- Four-Channel Grouped Delay Switching to Prevent Inrush Current
- Operating Temperature: -40°C to $+85^{\circ}\text{C}$

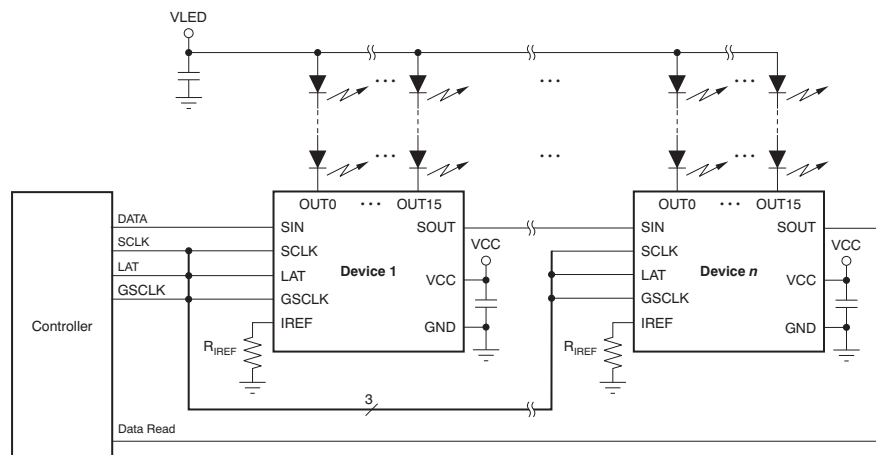
APPLICATIONS

- LED Video Displays
- LED Signboards

DESCRIPTION

The TLC5949 is a 16-channel, constant-current sink LED driver. Each channel has an individually-adjustable, pulse width modulation (PWM) grayscale (GS) brightness control with 4096 steps. All channels have a 128-step global brightness control (BC). BC adjusts brightness deviation with other LED drivers. GS and BC data are accessible with a serial interface port.

The TLC5949 has six error flags: LED open detection (LOD), LED short detection (LSD), output leakage detection (OLD), reference current terminal short flag detection (ISF), pre-thermal warning (PTW), and thermal error flag (TEF). The error detection results can be read with a serial interface port.



Typical Application Circuit (Multiple Daisy-Chained TLC5949s)



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE AND ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA
TLC5949	DBQ	TLC5949DBQR	Tape and Reel
		TLC5949DBQ	Tube
	PWP	TLC5949PWPR	Tape and Reel
		TLC5949PWP	Tube

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Voltage ⁽²⁾	VCC	–0.3	+6.0	V
	SIN, SCLK, LAT, GSCLK, IREF	–0.3	V _{CC} + 0.3	V
	SOUT	–0.3	V _{CC} + 0.3	V
	OUT0 to OUT15	–0.3	+11	V
Current	OUT0 to OUT15		+60	mA
Temperature	Operating junction, T _J (max)		+150	°C
	Storage, T _{stg}	–55	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)		3000	V
	Charged device model (CDM)		2000	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to device ground terminal.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TLC5949		UNITS
		DBQ (SSOP, QSOP)	PWP (HTSSOP)	
		24 PINS	24 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	80.4	39.9	°C/W
θ_{JTop}	Junction-to-case (top) thermal resistance	44.2	23.2	
θ_{JB}	Junction-to-board thermal resistance	33.5	21.5	
ψ_{JT}	Junction-to-top characterization parameter	8.8	0.6	
ψ_{JB}	Junction-to-board characterization parameter	33.2	21.3	
θ_{JBot}	Junction-to-case (bottom) thermal resistance	N/A	3.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com).

RECOMMENDED OPERATING CONDITIONS

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ and $V_{CC} = 3\text{ V}$ to 3.6 V , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DC CHARACTERISTICS						
V_{CC}	Supply voltage		3.0		3.6	V
V_O	Voltage applied to output	OUT0 to OUT15			10	V
V_{IH}	High-level input voltage	SIN, SCLK, LAT, GSCLK	$0.7 \times V_{CC}$		V_{CC}	V
V_{IL}	Low-level input voltage	SIN, SCLK, LAT, GSCLK	GND		$0.3 \times V_{CC}$	V
I_{OH}	High-level output current	SOUT			-2	mA
I_{OL}	Low-level output current	SOUT			2	mA
I_{OLC}	Constant output sink current	OUT0 to OUT15, $3\text{ V} \leq V_{CC} \leq 3.6\text{ V}$			45	mA
T_A	Operating free-air temperature range		-40		+85	$^{\circ}\text{C}$
T_J	Operating junction temperature range		-40		+125	$^{\circ}\text{C}$
AC CHARACTERISTICS						
f_{CLK} (SCLK)	Data shift clock frequency	SCLK			33	MHz
f_{CLK} (GSCLK)	Grayscale control clock frequency	GSCLK			33	MHz
t_{WH0}	Pulse duration	SCLK	10			ns
t_{WL0}		SCLK	10			ns
t_{WH1}		GSCLK	10			ns
t_{WL1}		GSCLK	10			ns
t_{WH2}		LAT	30			ns
t_{SU0}	Setup time	SIN \uparrow to SCLK \uparrow	5			ns
t_{SU1}		LAT \uparrow to SCLK \uparrow	120			ns
t_{SU2}		LAT \uparrow for BLANK bit '0' set to GSCLK \uparrow	50			ns
t_{SU3}		LAT \uparrow for GS data written to GSCLK \uparrow when display time reset mode is enabled	100			ns
t_{H0}	Hold time	SCLK \uparrow to SIN \uparrow ↓	5			ns
t_{H1}		SCLK \uparrow to LAT \uparrow	5			ns

ELECTRICAL CHARACTERISTICS

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ and $V_{CC} = 3\text{ V}$ to 3.6 V , unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$ and $V_{CC} = 3.3\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage (SOUT)	$I_{OH} = -2\text{ mA}$	$V_{CC} - 0.4$		V_{CC}	V
V_{OL}	Low-level output voltage (SOUT)	$I_{OL} = 2\text{ mA}$			0.4	V
V_{LOD0}	LED open-detection threshold	All $OUT_n = \text{on}$, $LODVLT = 00$	0.25	0.30	0.35	V
V_{LOD1}		All $OUT_n = \text{on}$, $LODVLT = 01$	0.55	0.6	0.65	V
V_{LOD2}		All $OUT_n = \text{on}$, $LODVLT = 10$	0.85	0.9	0.95	V
V_{LOD3}		All $OUT_n = \text{on}$, $LODVLT = 11$	1.15	1.2	1.25	V
V_{LSD0}	LED short-detection threshold	All $OUT_n = \text{on}$, $LSDVLT = 00$	$0.30 \times V_{CC}$	$0.35 \times V_{CC}$	$0.40 \times V_{CC}$	V
V_{LSD1}		All $OUT_n = \text{on}$, $LSDVLT = 01$	$0.40 \times V_{CC}$	$0.45 \times V_{CC}$	$0.50 \times V_{CC}$	V
V_{LSD2}		All $OUT_n = \text{on}$, $LSDVLT = 10$	$0.50 \times V_{CC}$	$0.55 \times V_{CC}$	$0.60 \times V_{CC}$	V
V_{LSD3}		All $OUT_n = \text{on}$, $LSDVLT = 11$	$0.60 \times V_{CC}$	$0.65 \times V_{CC}$	$0.70 \times V_{CC}$	V
V_{REF}	Reference voltage output	$R_{REF} = 1.1\text{ k}\Omega$	1.17	1.20	1.23	V
I_{IN}	Input current (SIN, SCLK, LAT, GSCLK)	$V_{IN} = V_{CC}$ or GND	-1		1	μA
I_{CC0}	Supply current (V_{CC})	SIN, SCLK, LAT, and GSCLK = GND, BLANK = 1, $GS_n = \text{FFFh}$, BC = 7Fh, $V_{OUT_n} = 0.8\text{ V}$, $R_{REF} = \text{open}$ (all outputs off)	1.5		3	mA
I_{CC1}		SIN, SCLK, LAT, and GSCLK = GND, BLANK = 1, $GS_n = \text{FFFh}$, BC = 7Fh, $V_{OUT_n} = 0.8\text{ V}$, $R_{REF} = 2.2\text{ k}\Omega$ (all outputs off, $I_{OUT_n} = 23.1\text{-mA}$ target)	5		7	mA
I_{CC2}		SIN, SCLK, and LAT = GND, BLANK = 0, auto display repeat enabled, GSCLK = 33 MHz, $GS_n = \text{FFFh}$, BC = 7Fh, $V_{OUT_n} = 0.8\text{ V}$, $R_{REF} = 2.2\text{ k}\Omega$ ($I_{OUT} = 23.1\text{-mA}$ target)	7		9	mA
I_{CC3}		SIN, SCLK, and LAT = GND, BLANK = 0, auto display repeat enabled, GSCLK = 33 MHz, $GS_n = \text{FFFh}$, BC = 7Fh, $V_{OUT_n} = 0.8\text{ V}$, $R_{REF} = 1.1\text{ k}\Omega$ ($I_{OUT} = 46.1\text{-mA}$ target)	11		14	mA
I_{CC4}		$V_{CC} = 3.3\text{ V}$, SIN, SCLK, LAT, and GSCLK = GND, BLANK = 0, auto display repeat enabled, $GS_n = 000\text{h}$, BC = 7Fh, in power-save mode, $V_{OUT_n} = 0.8\text{ V}$, $R_{REF} = 1.1\text{ k}\Omega$ ($I_{OUT} = 46.1\text{-mA}$ target)	10		40	μA
I_{OLC0}	Constant output sink current (OUT0 to OUT15)	All $OUT_n = \text{on}$, BC = 7Fh, $V_{OUT_n} = V_{OUT_{fix}} = 0.8\text{ V}$, $R_{REF} = 1.1\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ ($I_{OLC_n} = 46.1\text{-mA}$ target)	43.4	46.1	48.8	mA
I_{OLKG0}	Output leakage current (OUT0 to OUT15)	All $OUT_n = \text{off}$, BLANK = 1, $V_{OUT_n} = V_{OUT_{fix}} = 10\text{ V}$, $R_{REF} = 1.1\text{ k}\Omega$	$T_J = +25^\circ\text{C}$		0.1	μA
I_{OLKG1}			$T_J = +85^\circ\text{C}^{(1)}$		0.2	μA
I_{OLKG2}			$T_J = +125^\circ\text{C}^{(1)}$		0.3	μA

(1) Not tested; specified by design.

ELECTRICAL CHARACTERISTICS (continued)

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ and $V_{CC} = 3\text{ V}$ to 3.6 V , unless otherwise noted. Typical values are at $T_A = +25^{\circ}\text{C}$ and $V_{CC} = 3.3\text{ V}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔI_{OLC0}	Constant-current error (channel-to-channel, OUT0 to OUT15) ⁽²⁾		± 0.6	± 2	%
ΔI_{OLC1}	Constant-current error (device-to-device, OUT0 to OUT15) ⁽³⁾		± 1	± 4	%
ΔI_{OLC2}	Line regulation (OUT0 to OUT15) ⁽⁴⁾		± 0.1	± 1	%/V
ΔI_{OLC3}	Load regulation (OUT0 to OUT15) ⁽⁵⁾		± 0.1	± 1	%/V
T_{TEF}	Thermal error flag threshold	150	165	180	$^{\circ}\text{C}$
T_{HYS}	Thermal error flag hysteresis	5	10	20	$^{\circ}\text{C}$
T_{PTW}	Pre-thermal warning threshold	125	138	150	$^{\circ}\text{C}$

(2) The deviation of each output from the OUT0 to OUT15 constant-current average. Deviation is calculated by the formula:

$$\Delta (\%) = 100 \times \left[\frac{\frac{I_{OLCn}}{I_{OLC0} + I_{OLC1} + \dots + I_{OLC14} + I_{OLC15}} - 1}{16} \right]$$

where $n = 0$ to 15 .

(3) Deviation of the OUT0 to OUT15 constant-current average from the ideal constant-current value. Deviation is calculated by the formula:

$$\Delta (\%) = 100 \times \left[\frac{\frac{(I_{OLC0} + I_{OLC1} + \dots + I_{OLC14} + I_{OLC15})}{16} - \text{Ideal Output Current}}{\text{Ideal Output Current}} \right]$$

Ideal current is calculated by the formula:

$$I_{OUTn} = \left[\frac{1}{4} + \frac{3/4 \text{ BC}}{127} \right] \times I_{OLCMax}$$

(4) Line regulation is calculated by the formula:

$$\Delta (\%/V) = \left[\frac{(I_{OLCn} \text{ at } V_{CC} = 3.6 \text{ V}) - (I_{OLCn} \text{ at } V_{CC} = 3 \text{ V})}{I_{OLCn} \text{ at } V_{CC} = 3 \text{ V}} \right] \times \frac{100}{3.6 \text{ V} - 3 \text{ V}}$$

where $n = 0$ to 15 .

(5) Load regulation is calculated by the equation:

$$\Delta (\%/V) = \left[\frac{(I_{OLCn} \text{ at } V_{OUTn} = 3 \text{ V}) - (I_{OLCn} \text{ at } V_{OUTn} = 0.8 \text{ V})}{I_{OLCn} \text{ at } V_{OUTn} = 0.8 \text{ V}} \right] \times \frac{100}{3 \text{ V} - 0.8 \text{ V}}$$

where $n = 0$ to 15 .

(6) Not tested; specified by design.

SWITCHING CHARACTERISTICS (See Figure 4, Figure 5, and Figure 8 through Figure 11)

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 3\text{ V}$ to 3.6 V , $C_L = 15\text{ pF}$, $R_L = 82\ \Omega$, $R_{REF} = 1.1\text{ k}\Omega$, and $V_{LED} = 5.0\text{ V}$, unless otherwise noted. Typical values are at $V_{CC} = 3.3\text{ V}$ and $T_A = +25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{R0}	Rise time	SOUT			5	ns
t_{R1}		OUT n and BC = 7Fh		13		ns
t_{F0}	Fall time	SOUT			5	ns
t_{F1}		OUT n and BC = 7Fh		23		ns
t_{D0}	Propagation delay	SCLK \uparrow to SOUT $\uparrow\downarrow$		15	25	ns
t_{D1}		LAT \uparrow for BLANK = 1 and OUT0, OUT7, OUT8, and OUT15 off		40	75	ns
t_{D2}		GSCLK \uparrow to OUT0, OUT7, OUT8, and OUT15 on/off with BC = 7Fh	5	36	65	ns
t_{D3}		GSCLK \uparrow to OUT1, OUT6, OUT9, and OUT14 on/off with BC = 7Fh	20	62	97	ns
t_{D4}		GSCLK \uparrow to OUT2, OUT5, OUT10, and OUT13 on/off with BC = 7Fh	35	88	129	ns
t_{D5}		GSCLK \uparrow to OUT3, OUT4, OUT11, and OUT12 on/off with BC = 7Fh	50	114	161	ns
t_{D6}		LAT \uparrow to power-save mode by writing data for OUT n off with BLANK = 1 and PSMODE = 110			200	ns
t_{D7}		SCLK \uparrow to normal mode with PSMODE = 101 or LAT \uparrow to normal mode by writing GS data for OUT n on with BLANK = 1 and PSMODE = 110			50	μs
t_{ON_ERR}	Output on-time error ⁽¹⁾	$t_{OUTON} - t_{GSCLK}$, GS n = 001h, GSCLK = 33 MHz, BC = 7Fh, $T_A = +25^\circ\text{C}$	-20		10	ns

- (1) Output on-time error (t_{ON_ERR}) is calculated by the formula: $t_{ON_ERR} = t_{OUT_ON} - t_{GSCLK}$. t_{OUTON} is the actual on-time of the constant-current driver. t_{GSCLK} is the GSCLK period.

PARAMETER MEASUREMENT INFORMATION

PIN-EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

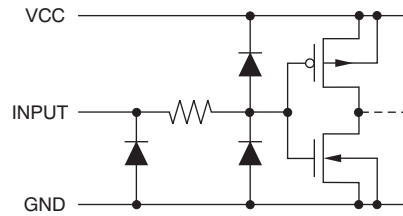


Figure 1. SIN, SCLK, LAT, GSCLK

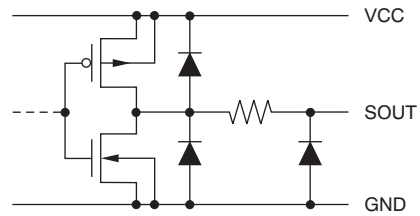
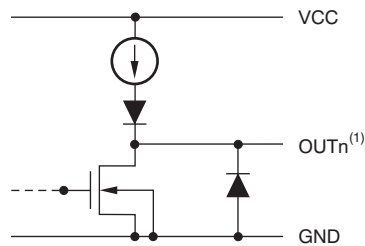


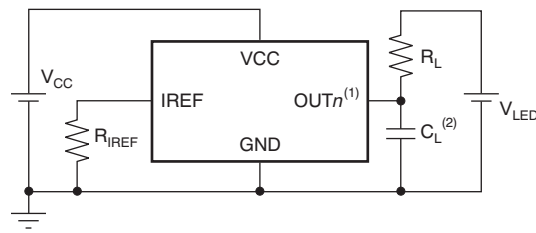
Figure 2. SOUT



(1) n = 0 to 15.

Figure 3. OUT0 Through OUT15

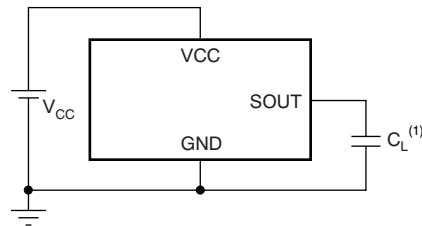
TEST CIRCUITS



(1) $n = 0$ to 15.

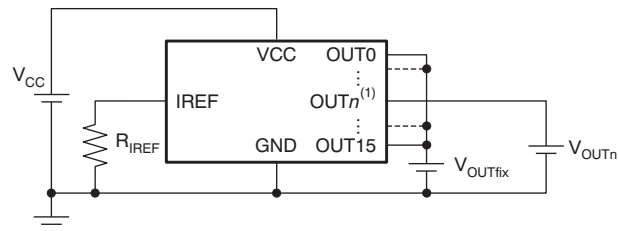
(2) C_L includes measurement probe and jig capacitance.

Figure 4. Rise Time and Fall Time Test Circuit for OUT_n



(1) C_L includes measurement probe and jig capacitance.

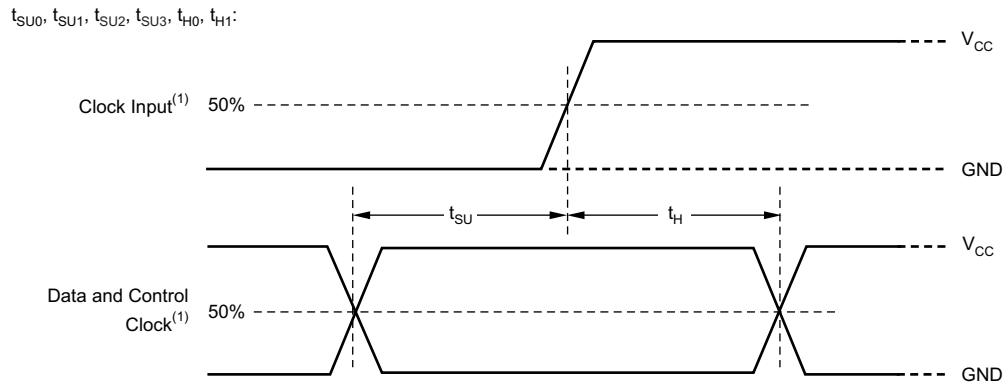
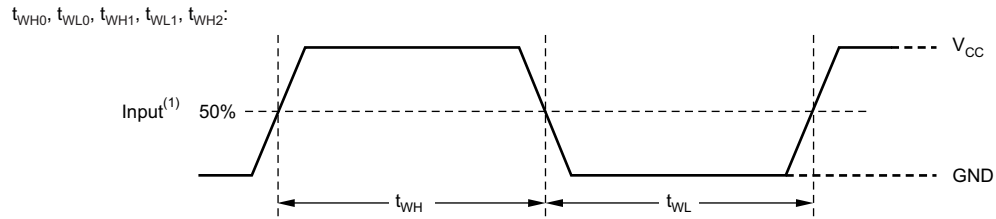
Figure 5. Rise Time and Fall Time Test Circuit for SOUT



(1) $n = 0$ to 15.

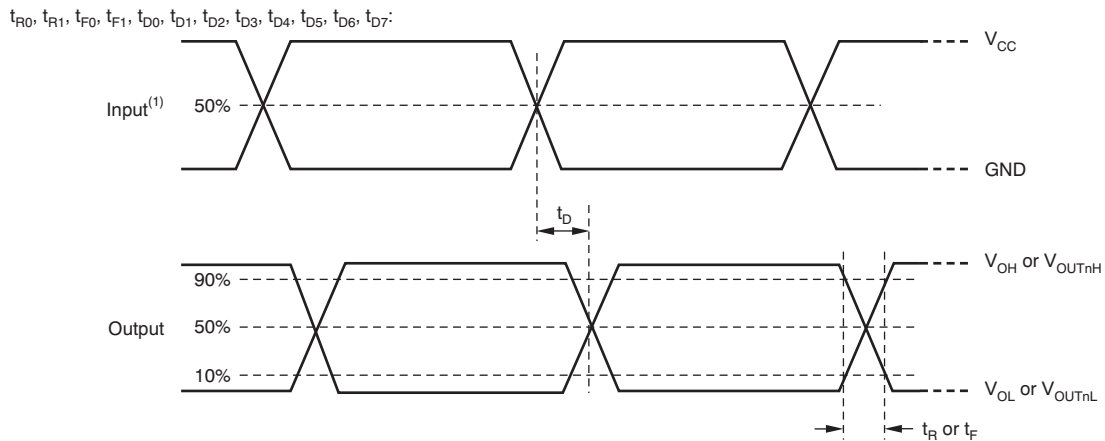
Figure 6. Constant-Current Test Circuit for OUT_n

TIMING DIAGRAMS



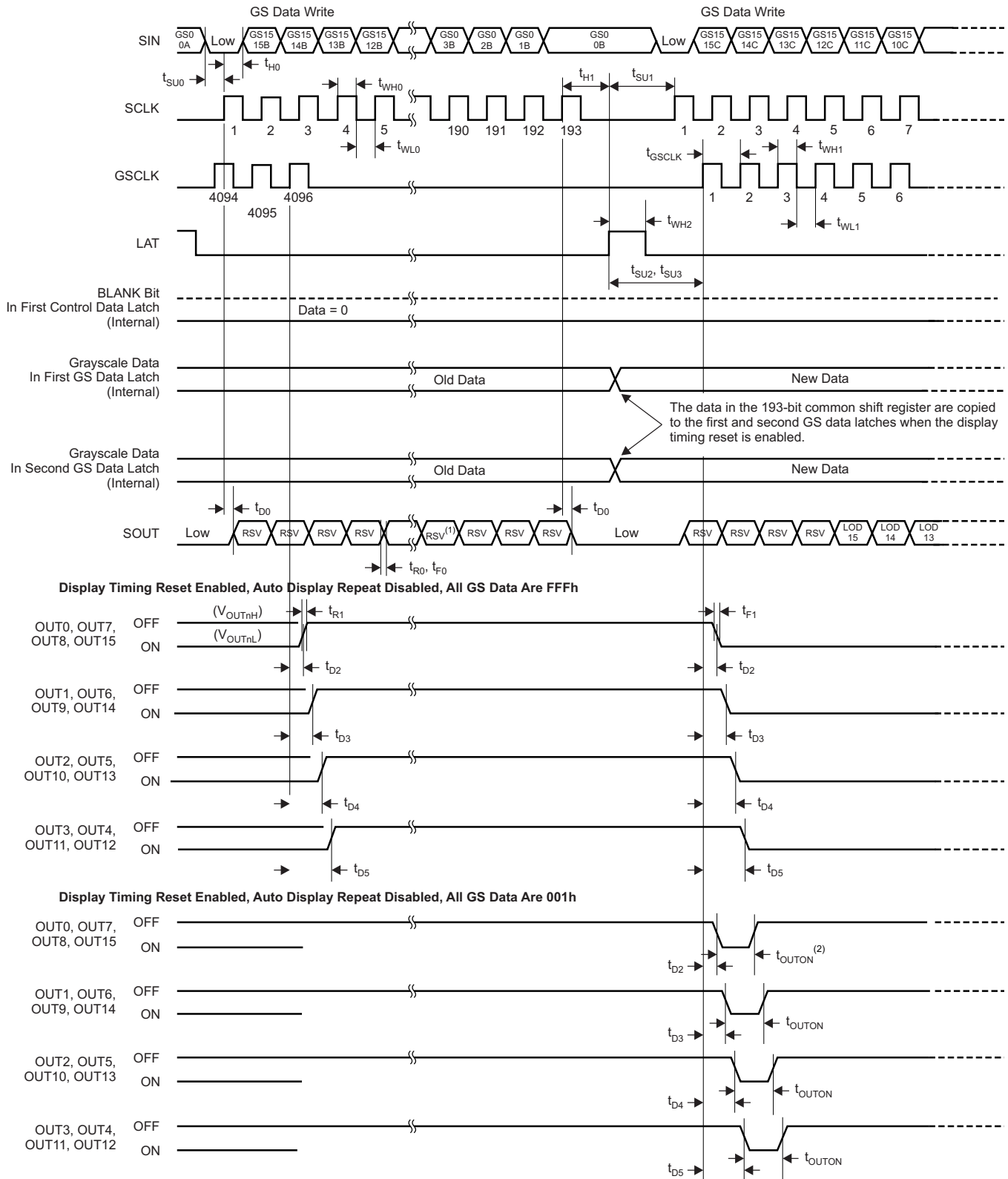
(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 7. Input Timing



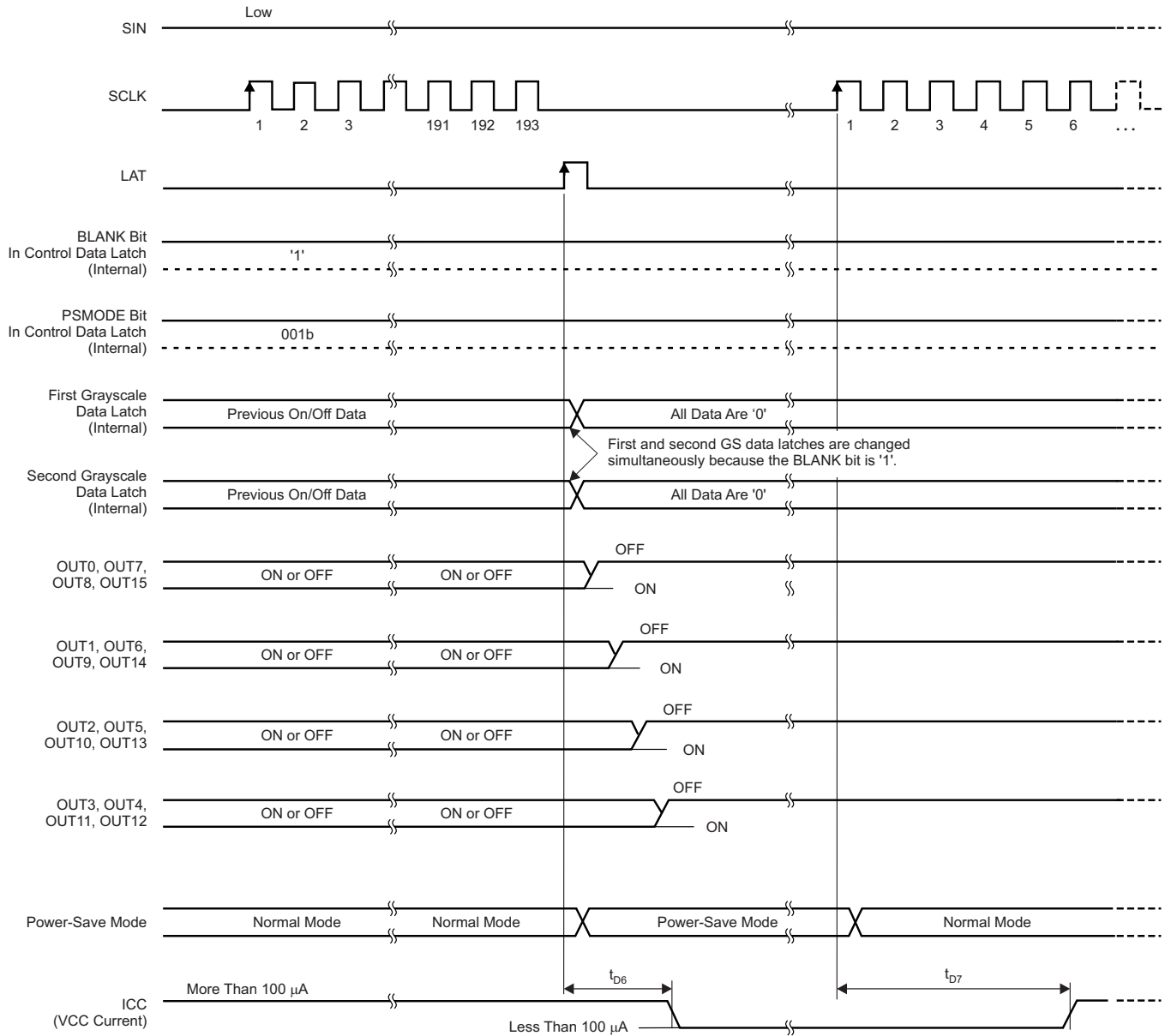
(1) Input pulse rise and fall time is 1 ns to 3 ns.

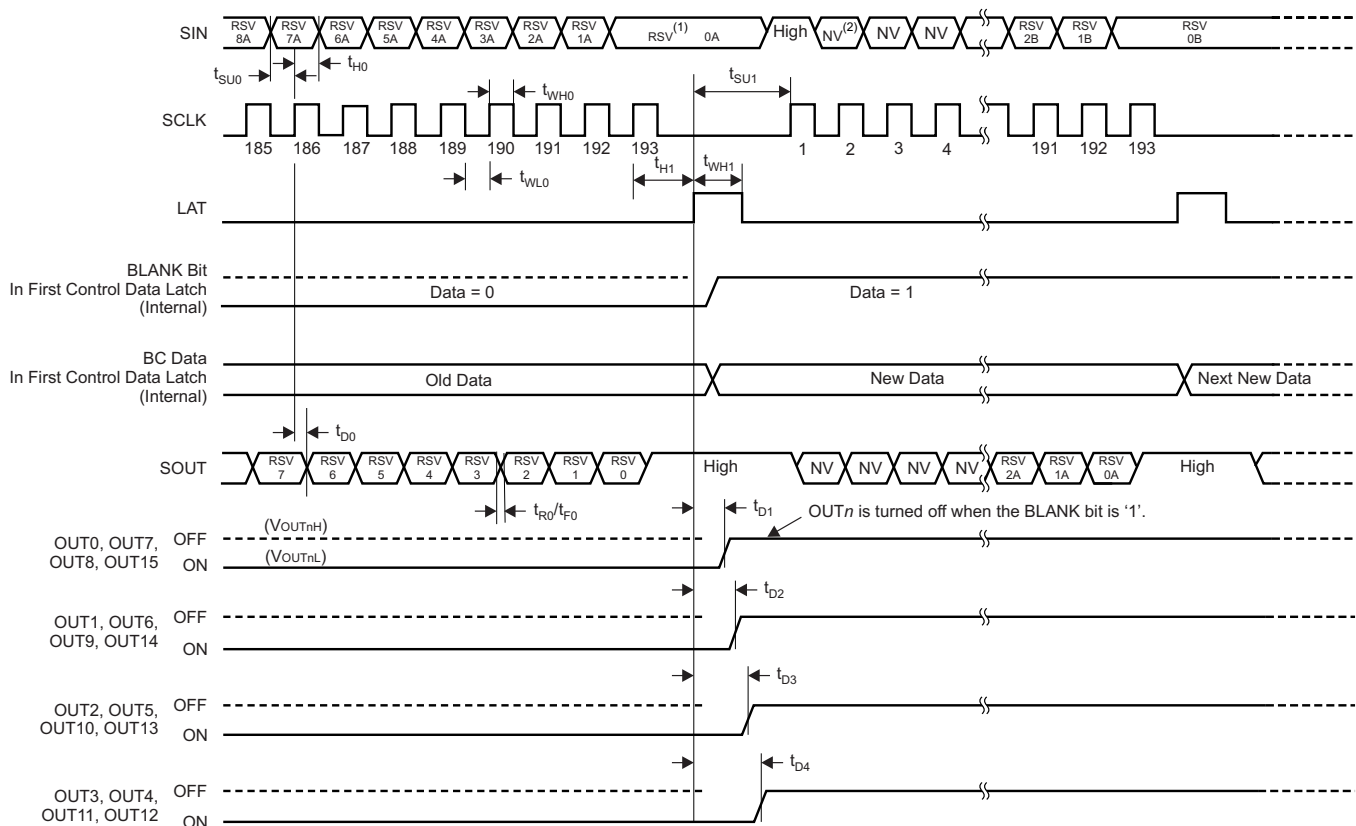
Figure 8. Output Timing



(1) RSV = reserved.

(2) t_{OUTON} refers to t_{ON_ERR} = t_{OUTON} - t_{GSCLK}.**Figure 9. Grayscale Data Write Timing**


Figure 10. Power-Save Mode Timing



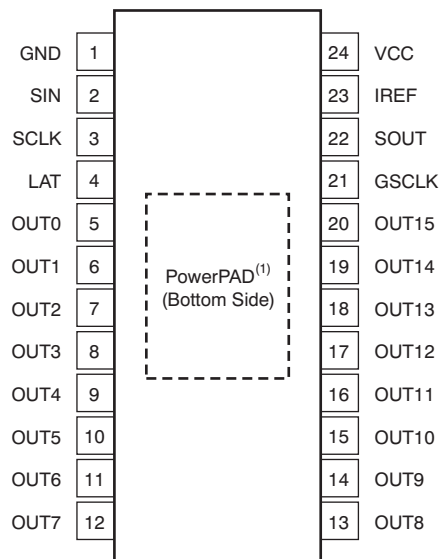
(1) RSV = reserved.

(2) NV = Not valid; these data are not used for any function.

Figure 11. Control Data Write Timing

PIN CONFIGURATION

DBQ AND PWP PACKAGES SSOP-24, QSOP-24, AND HTSSOP-24 (TOP VIEW)

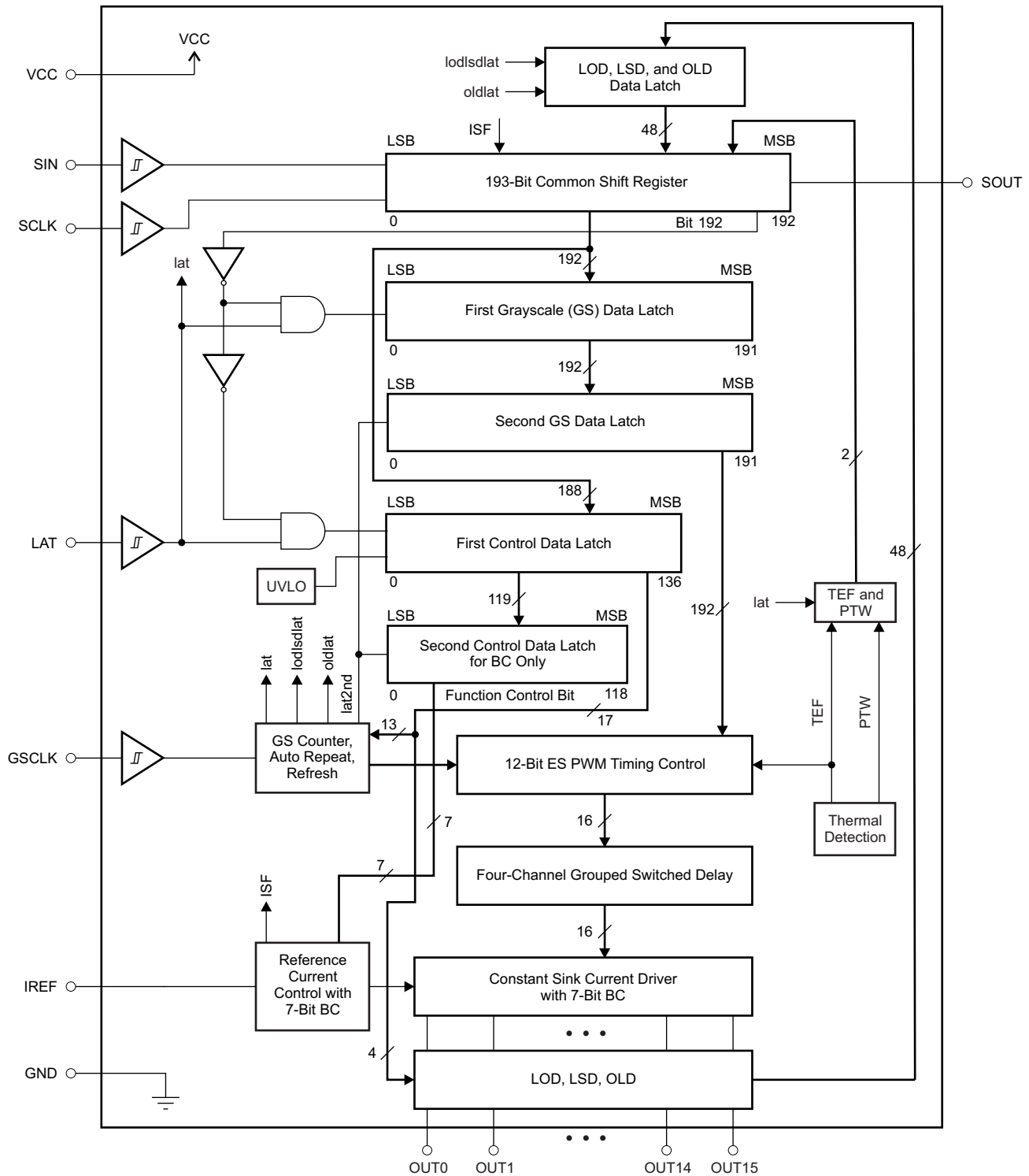


NOTE: The PowerPAD only applies to the PWP package.

PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Power ground
GSCLK	21	I	Grayscale (GS) pulse width modulation (PWM) reference clock control for OUT _n . When BLANK = 0, each GSCLK rising edge increments the GS counter for PWM control. When BLANK = 1, all constant-current outputs (OUT0 to OUT15) are forced off, the GS counter is reset to '0', and the GS PWM timing controller is initialized.
IREF	23	I/O	Reference current terminal. A resistor connected between IREF to GND sets the maximum current for all constant-current outputs. When IREF is shorted to GND with low resistance, all constant-current outputs are forced off and the IREF short flag (ISF) bit in the status information data (SID) is set to '1'.
LAT	4	I	The LAT rising edge either latches the data from the 193-bit common shift register into the first GS data latch when the common shift register MSB is '0' or latches the data into the first control data latch when the common shift register MSB is '1'. When the display timing reset bit (TMGRST) in the first control data latch is '1', the GS counter is initialized at the LAT signal for GS data writes. At the same time, the data in the 193-bit common shift register are copied to the first and second GS data latches simultaneously and the BC data in the first control data latch are copied to the second data latch.
OUT0	5	O	Constant-current outputs. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
OUT1	6	O	
OUT2	7	O	
OUT3	8	O	
OUT4	9	O	
OUT5	10	O	
OUT6	11	O	
OUT7	12	O	
OUT8	13	O	
OUT9	14	O	
OUT10	15	O	
OUT11	16	O	
OUT12	17	O	
OUT13	18	O	
OUT14	19	O	
OUT15	20	O	
SCLK	3	I	Serial data shift clock. Data present on SIN are shifted to the 193-bit common shift register LSB with the SCLK rising edge. Data in the shift register are shifted towards the MSB at each SCLK rising edge. The common shift register MSB appears on SOUT.
SIN	2	I	193-bit common shift register serial data input.
SOUT	22	O	193-bit common shift register serial data output. LED open detection (LOD), LED short detection (LSD), output leak detection (OLD), thermal error flag (TEF), and the IREF pin short flag (ISF) bits can be read out with SOUT as SID after the LAT rising edge. SOUT is connected to the 193-bit common shift register MSB. Data are clocked out at the SCLK rising edge.
VCC	24	—	Power-supply voltage

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

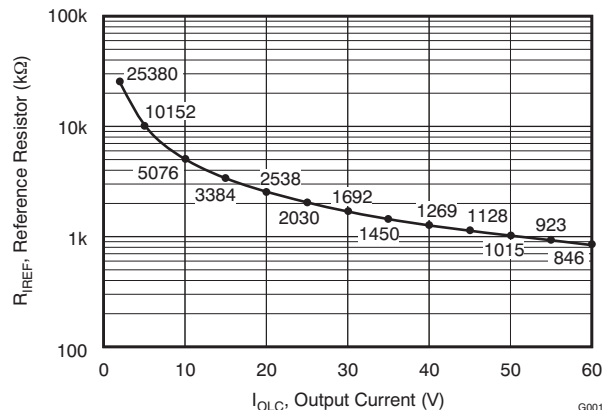


Figure 12. REFERENCE RESISTOR vs OUTPUT CURRENT

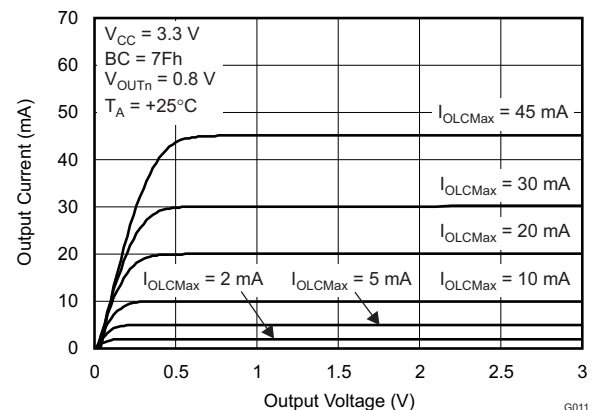


Figure 13. OUTPUT CURRENT vs OUTPUT VOLTAGE (+3.3 V)

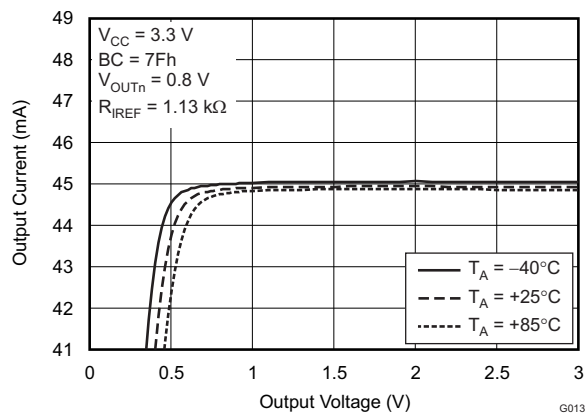


Figure 14. OUTPUT CURRENT vs OUTPUT VOLTAGE (+3.3 V)

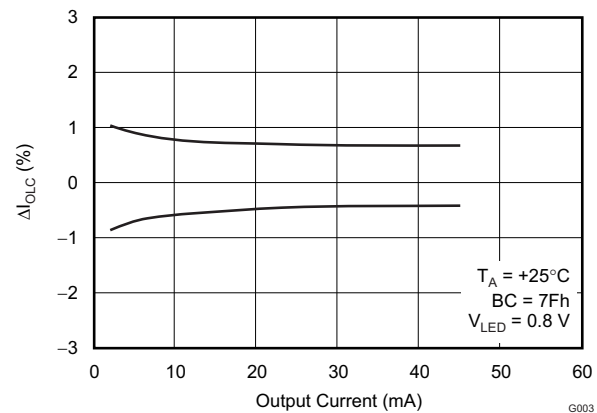


Figure 15. CONSTANT-CURRENT ERROR vs OUTPUT CURRENT

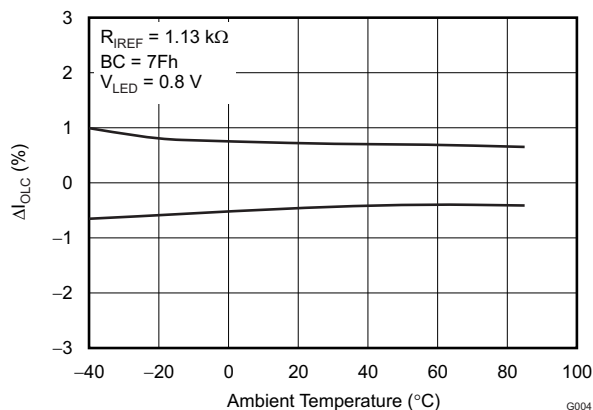


Figure 16. CONSTANT-CURRENT ERROR vs AMBIENT TEMPERATURE

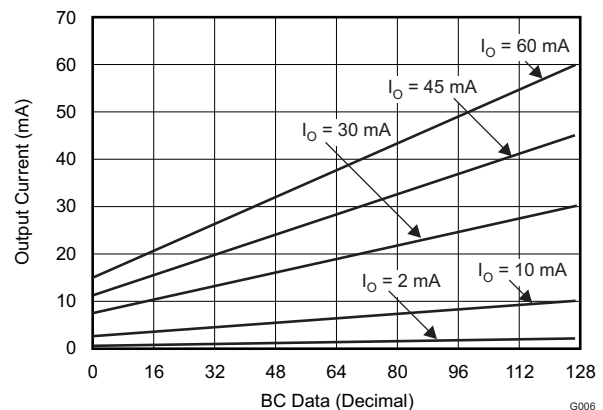


Figure 17. GLOBAL BRIGHTNESS CONTROL LINEARITY

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

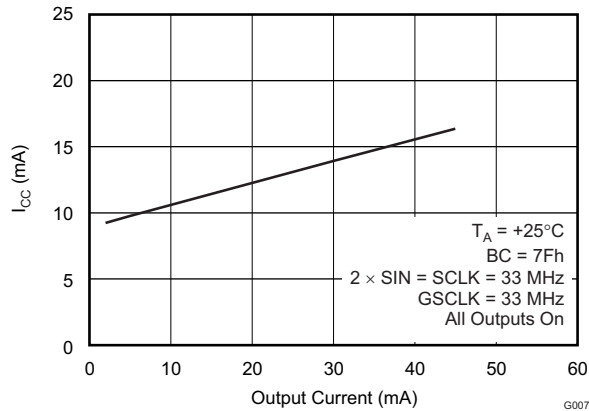


Figure 18. SUPPLY CURRENT vs OUTPUT CURRENT

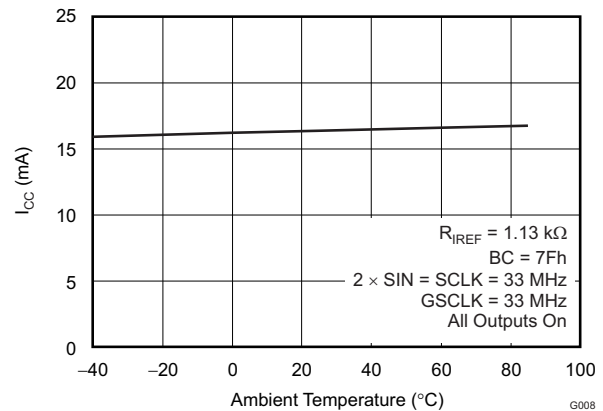


Figure 19. SUPPLY CURRENT vs AMBIENT TEMPERATURE

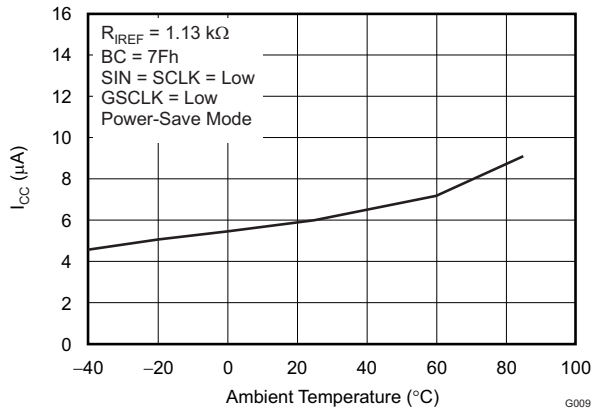


Figure 20. SUPPLY CURRENT IN POWER-SAVE MODE vs AMBIENT TEMPERATURE

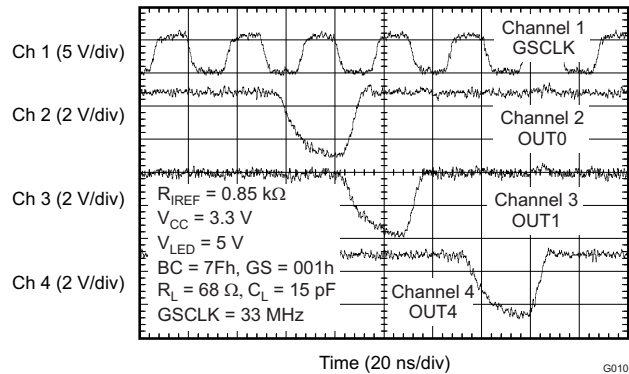


Figure 21. CONSTANT-CURRENT OUTPUT VOLTAGE WAVEFORM

DETAILED DESCRIPTION

MAXIMUM CONSTANT SINK CURRENT VALUE

The maximum output current value of each channel (I_{OLCMax}) is programmed by a single resistor (R_{IREF}) that is placed between the IREF and GND pins. The current value can be calculated by [Equation 1](#):

$$R_{IREF} = \frac{V_{IREF}}{I_{OLCMax}} \times 42.3$$

Where:

V_{IREF} = the internal reference voltage on IREF, typically 1.20 V when the global brightness control (BC) data are at maximum

I_{OLCMax} = 2 mA to 45 mA with BC = 7Fh (127) (1)

I_{OLCMax} is the highest current for each output. Each output sinks I_{OLCMax} current when it is turned on, and the global brightness control (BC) data are set to the maximum value of 7Fh (127). Each output sink current can be reduced by lowering the BC value.

R_{IREF} must be between 1.13 kΩ and 25.4 kΩ in order to hold I_{OLCMax} between 45 mA (typ) and 2 mA (typ). Otherwise, the output may be unstable. Output currents lower than 2 mA can be achieved by setting I_{OLCMax} to 2 mA or higher and then using global BC to lower the output current.

[Table 1](#) shows the characteristics of the constant-current sink versus the external resistor, R_{IREF} .

Table 1. Maximum Constant-Current Output versus External Resistor Value

I_{OLCMax} (mA)	R_{IREF} (kΩ, typ)
45	1.13
40	1.27
35	1.45
30	1.70
25	2.03
20	2.53
15	3.38
10	5.08
5	10.2
2	25.4

GLOBAL BRIGHTNESS CONTROL (BC) FUNCTION

The TLC5949 is capable of adjusting the output current of all constant-current outputs simultaneously. This function is called *global brightness control* (BC). The global BC for all outputs (OUT0 to OUT15) is programmed with a 7-bit word. The global BC adjusts all output currents in 128 steps from 25% to 100%, where 100% corresponds to the maximum output current set by R_{IREF} . [Equation 2](#) calculates the actual output current as a function of R_{IREF} and global BC value. BC data can be set via the serial interface. When the device is powered on, the BC data in the first and second control data latches contain random data. Therefore, BC data must be written to the BC data latch before turning the constant-current output on.

The output current value controlled by BC can be calculated by [Equation 2](#).

$$I_{OUTn} = \left[\frac{1}{4} + \frac{3/4 \text{ BC}}{127} \right] \times I_{OLCMax}$$

Where:

I_{OLCMax} = the maximum constant-current value for each output determined by R_{IREF}

BC = the global brightness control value in the second control data latch (0h to 7Fh) (2)

Table 2 summarizes the BC data versus the set current value.

Table 2. BC Data versus Constant-Current Ratio and Set Current Value

BC DATA			RATIO OF OUTPUT CURRENT TO I _{OLCMax} (%)	I _{OUT} (mA) (I _{OLCMax} = 45 mA, typ)	I _{OUT} (mA) (I _{OLCMax} = 2 mA, typ)
BINARY	DECIMAL	HEX			
000 0000	0	00h	25.0	11.25	0.50
000 0001	1	01h	25.6	11.52	0.51
000 0010	2	02h	26.2	11.78	0.52
—	—	—	—	—	—
111 1101	125	7Dh	98.8	44.47	1.98
111 1110	126	7Eh	99.4	44.73	1.99
111 1111	127	7Fh	100.0	45.00	2.00

GRAYSCALE (GS) FUNCTION (PWM CONTROL)

The TLC5949 can adjust the brightness of each output channel using a pulse width modulation (PWM) control scheme. The architecture of 12 bits per channel results in 4096 brightness steps, from 0% up to 100% brightness.

The PWM operation for OUT_n is controlled by a 12-bit grayscale (GS) counter. The GS counter increments on each GS reference clock (GSCLK) rising edge. The GS counter resets to 000h when the BLANK bit in the first control data latch is set to '1'; the counter value is held at 000h while the BLANK bit is '1', even if the GS clock input is toggled high and low.

The TLC5949 has two types of PWM control: conventional PWM control and enhanced spectrum (ES) PWM control. The conventional PWM control can be selected when the ESPWM bit in the first control data latch is '0'. The ES PWM control is selected when the ESPWM bit is '1'.

The on-time (t_{OUT_ON}) of each output (OUT_n) can be calculated by Equation 3.

$$t_{OUT_ON} = t_{GSCLK} \times GS_n \quad (3)$$

Table 3 summarizes the GS data values versus the output on-time duty cycle. When the device powers up, the BLANK bit in the first control data latch is set to '1'. The 193-bit common shift register and the first and second GS data latches contain random data. Therefore, GS data must be written to the GS latches before the BLANK bit is set to '0'. All constant-current outputs are off when the BLANK bit is '1'.

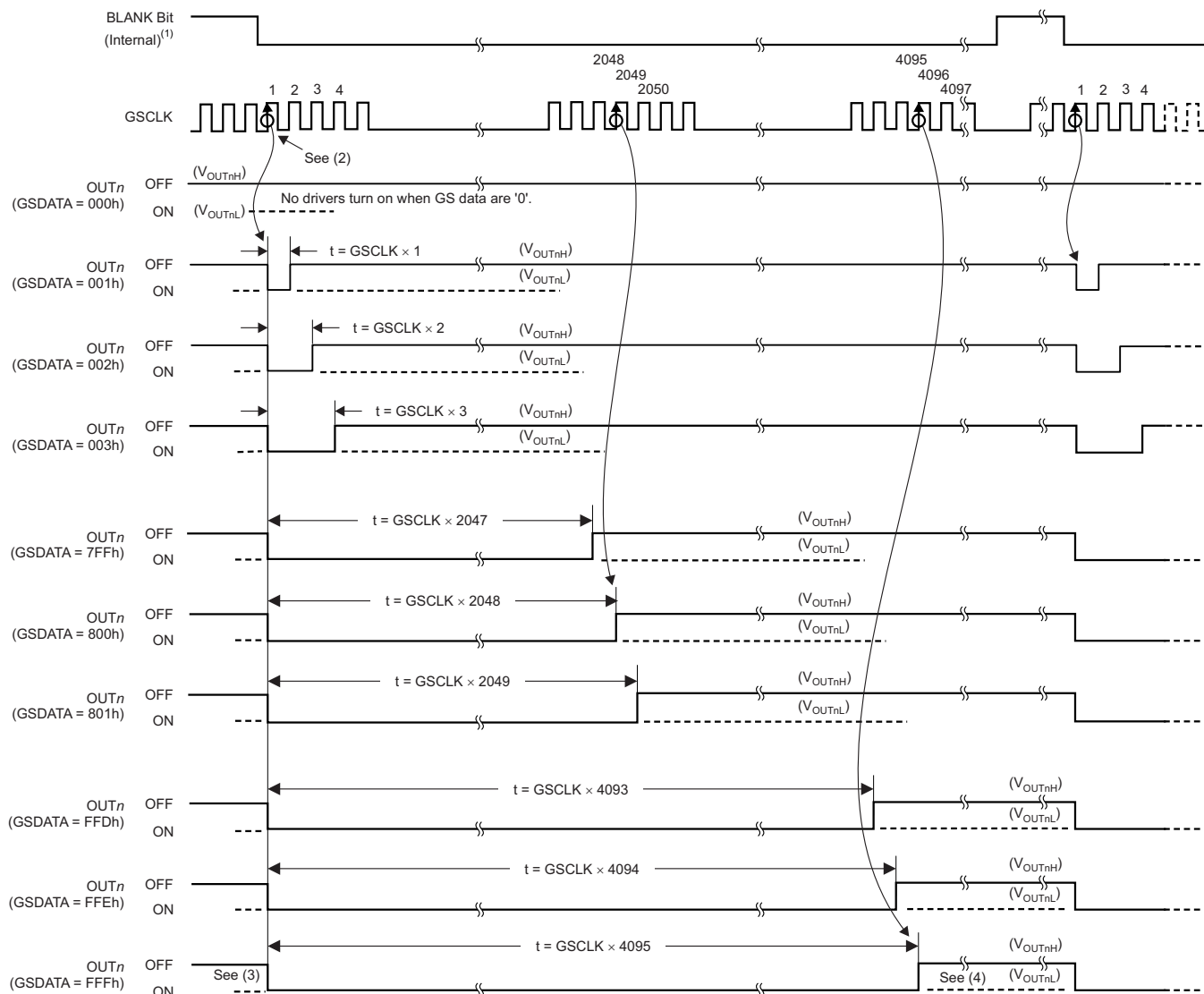
Table 3. Output Duty Cycle and On-Time versus GS Data

GS DATA		ON-TIME DUTY (%)	GS DATA		ON-TIME DUTY (%)
DECIMAL	HEX		DECIMAL	HEX	
0	000h	0	2048	800h	50.001
1	001h	0.002	2049	801h	50.002
2	002h	0.003	2050	802h	50.004
3	003h	0.005	2051	803h	50.005
—	—	—	—	—	—
511	1FFh	12.499	2559	9FFh	62.499
512	200h	12.500	2560	A00h	62.501
513	201h	12.502	2561	A01h	62.502
—	—	—	—	—	—
1023	3FFh	24.999	3071	BFFh	74.997
1024	400h	25.000	3072	C00h	74.998
1025	401h	25.002	3073	C01h	75.000
—	—	—	—	—	—
1535	5FFh	37.499	3583	DFFh	87.500
1536	600h	37.501	3584	E00h	87.501
1537	601h	37.502	3585	E01h	87.503
—	—	—	—	—	—
2045	7FDh	49.996	4093	FFDh	99.997
2046	7FEh	49.998	4094	FFEh	99.998
2047	7FFh	49.999	4095	FFFh	100.000

Conventional PWM Control

In this PWM control, the GS clock is enabled when the BLANK bit is set to '0'. The first GS clock rising edge after the BLANK bit is set to '0' increments the GS counter by one and switches on all outputs with a non-zero GS value programmed into the second GS data latch. Each additional GS clock rising edge increases the corresponding GS counter by one.

The GS counter keeps track of the number of clock pulses from the GS clock inputs. Each output stays on while the counter is less than or equal to the programmed GS value. Each output turns off at the GS counter value rising edge when the counter becomes greater than the output GS latch value. [Figure 22](#) illustrates the conventional PWM operation.



(1) The internal signal is generated when LAT inputs GS data with the display timing reset bit (TMGRST) set to '1'. This signal has the same function as a BLANK = 1 pulse. Furthermore, the signal is generated at the 4096th GSCLK when the auto display repeat bit (DSPRPT) is set to '1'.

(2) The GS counter begins to count GSCLK pulses after the BLANK bit is set to '0' or when the LAT signal for a GS data write is input with the display time reset mode enabled.

(3) OUT_n turns on at the first GSCLK rising edge except when GS data are '0' after the BLANK bit is set to '0' or when the LAT signal for a GS data write is input with the display time reset mode enabled.

(4) OUT_n does not turn on again until BLANK is set to '1' at least one time, except when the TMGRST or DSPRPT bits are '1'.

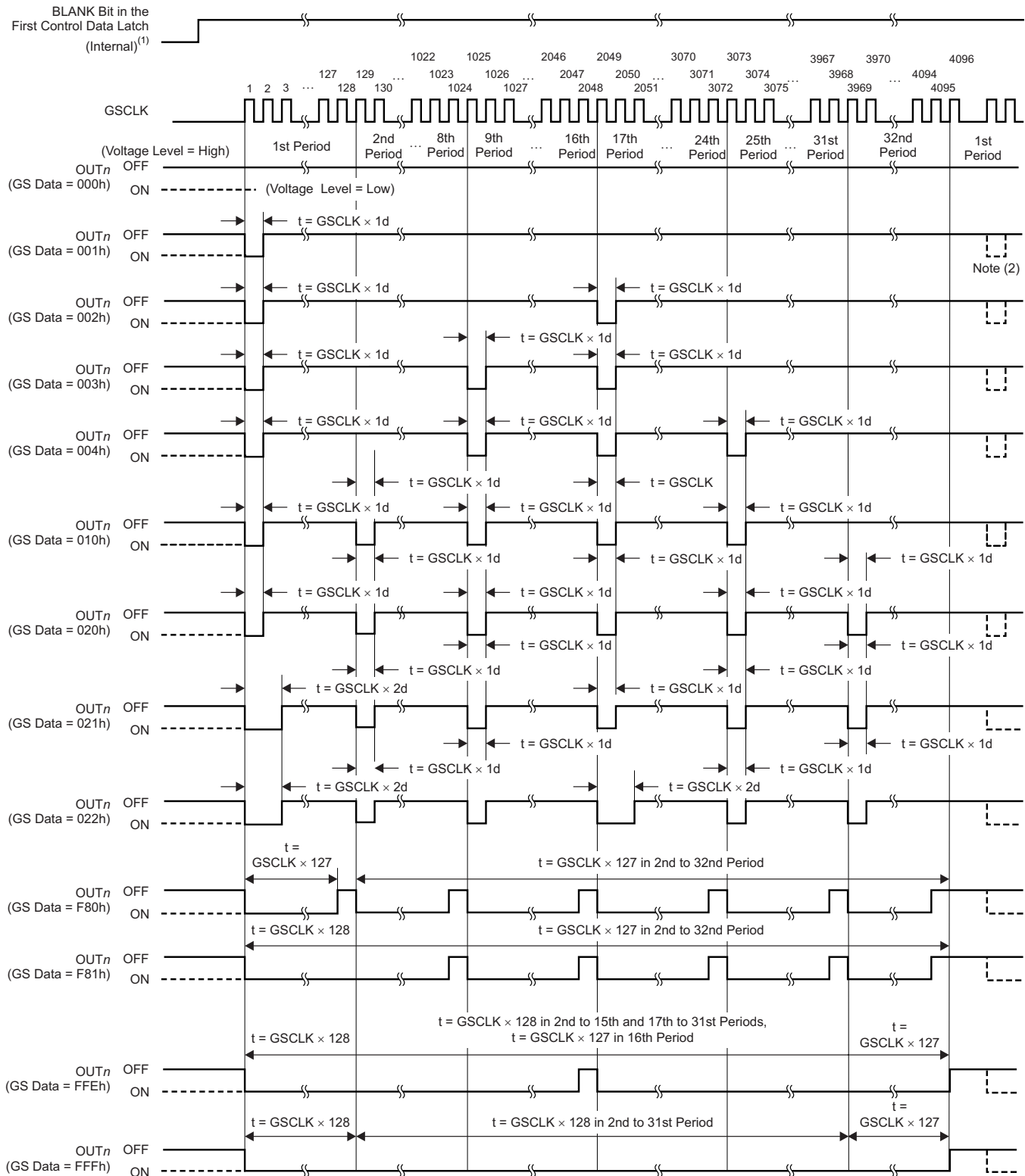
Figure 22. Conventional PWM Operation

Enhanced Spectrum (ES) PWM Control

In this PWM control, the total display period is divided into 32 display segments. The total display period is the time from the first GS clock (GSCLK) to the 4096th GSCLK input after the BLANK bit is set to '0'. Each display segment has a maximum of 128 GSCLKs. The OUT_n on-time changes, depending on the 12-bit GS data. Refer to [Table 4](#) for the sequence of information and to [Figure 23](#) for the timing information.

Table 4. ES PWM Drive Turn-On Time Length

GS DATA		OUT _n DRIVER OPERATION
DECIMAL	HEX	
0	000h	Does not turn on
1	001h	Turns on for one GSCLK period in the first display segment
2	002h	Turns on for one GSCLK period in the first and 17th display segments
3	003h	Turns on for one GSCLK period in the first, 17th, and 9th display segments
4	004h	Turns on for one GSCLK period in the first, 17th, 9th, and 25th display segments
5	005h	Turns on for one GSCLK period in the first, 17th, 9th, 25th, and 5th display segments
6	006h	Turns on for one GSCLK period in the first, 17th, 9th, 25th, 5th, and 21st display segments
—	—	The number of display segments where OUT _n is turned on for one GSCLK is incremented by increasing GS data in the following order: 1 > 17 > 9 > 25 > 5 > 21 > 13 > 29 > 3 > 19 > 11 > 27 > 7 > 23 > 15 > 31 > 2 > 18 > 10 > 26 > 6 > 22 > 14 > 30 > 4 > 20 > 12 > 28 > 8 > 24 > 16 > 32.
31	01Fh	Turns on for one GSCLK period in the first to 31st display segments, but does not turn on in the 32nd display segment
32	020h	Turns on for one GSCLK period in all display segments (first to 32nd)
33	021h	Turns on for two GSCLK periods in the first display period and for one GSCLK period in all other display periods
—	—	The number of display segments where OUT _n is turned on for one GSCLK is incremented by increasing GS data in the following order: 1 > 17 > 9 > 25 > 5 > 21 > 13 > 29 > 3 > 19 > 11 > 27 > 7 > 23 > 15 > 31 > 2 > 18 > 10 > 26 > 6 > 22 > 14 > 30 > 4 > 20 > 12 > 28 > 8 > 24 > 16 > 32.
63	03Fh	Turns on for two GSCLK periods in the first to 31st display segments and turns on one GSCLK period in the 32nd display segment
64	040h	Turns on for two GSCLK periods in all display segments (first to 32nd)
65	041h	Turns on for three GSCLK periods in the first display segment and for two GSCLK periods in all other display segments
—	—	The number of display segments where OUT _n is turned on for one GSCLK is incremented by increasing GS data in the following order: 1 > 17 > 9 > 25 > 5 > 21 > 13 > 29 > 3 > 19 > 11 > 27 > 7 > 23 > 15 > 31 > 2 > 18 > 10 > 26 > 6 > 22 > 14 > 30 > 4 > 20 > 12 > 28 > 8 > 24 > 16 > 32.
4063	EDFh	Turns on for 127 GSCLK periods in the first to 31st display segments, but only turns on for 126 GSCLK periods in the 32nd display segment
4064	FE0h	Turns on for 127 GSCLK periods in all display segments (first to 32nd)
4065	FE1h	Turns on for 128 GSCLK periods in the first display period and for 127 GSCLK periods in the second to 32nd display segments
—	—	—
4094	FFEh	Turns on for 128 GSCLK periods in the first to 15th and 17th to 31st display segments; also turns on for 127 GSCLK periods in the 16th and 32nd display segments.
4095	FFFh	Turns on for 128 GSCLK periods in the first to 31st display segments but only turns on for 127 GSCLK periods in the 32nd display segment



(1) The internal signal is generated when LAT inputs GS data when the display timing reset bit (TMGRST) is set to '1'. This signal has the same function as BLANK = 1. Furthermore, the signal is generated at the 4096th GSKLK when the auto display repeat bit (DSPRPT) is set to '1'.

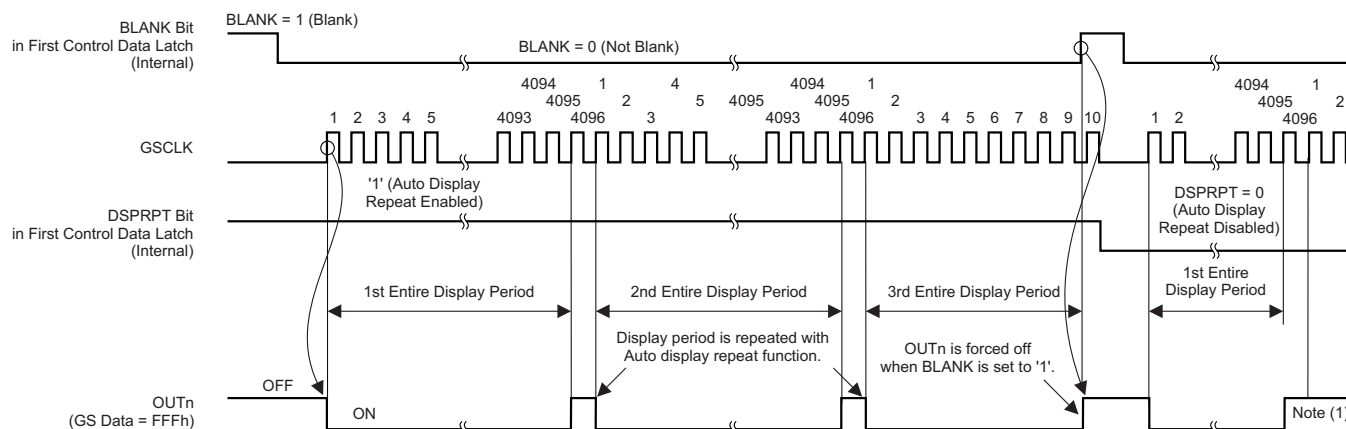
(2) When auto display repeat is on.

Figure 23. ES PWM Operation

Auto Display Repeat Function

This function can repeat the total display period as long as GSCLK is present, as shown in Figure 24. This function is switched on or off by the content of the DSPRPT bit in the first control data latch.

When the DSPRPT bit is '1', auto display repeat is enabled and the entire display period automatically repeats. When the DSPRPT bit is '0', the auto display repeat is disabled and the entire display period executes only one time after either the BLANK bit is changed from '1' to '0', or after a LAT signal rising edge for a GS data write is input when the display timing reset is enabled.

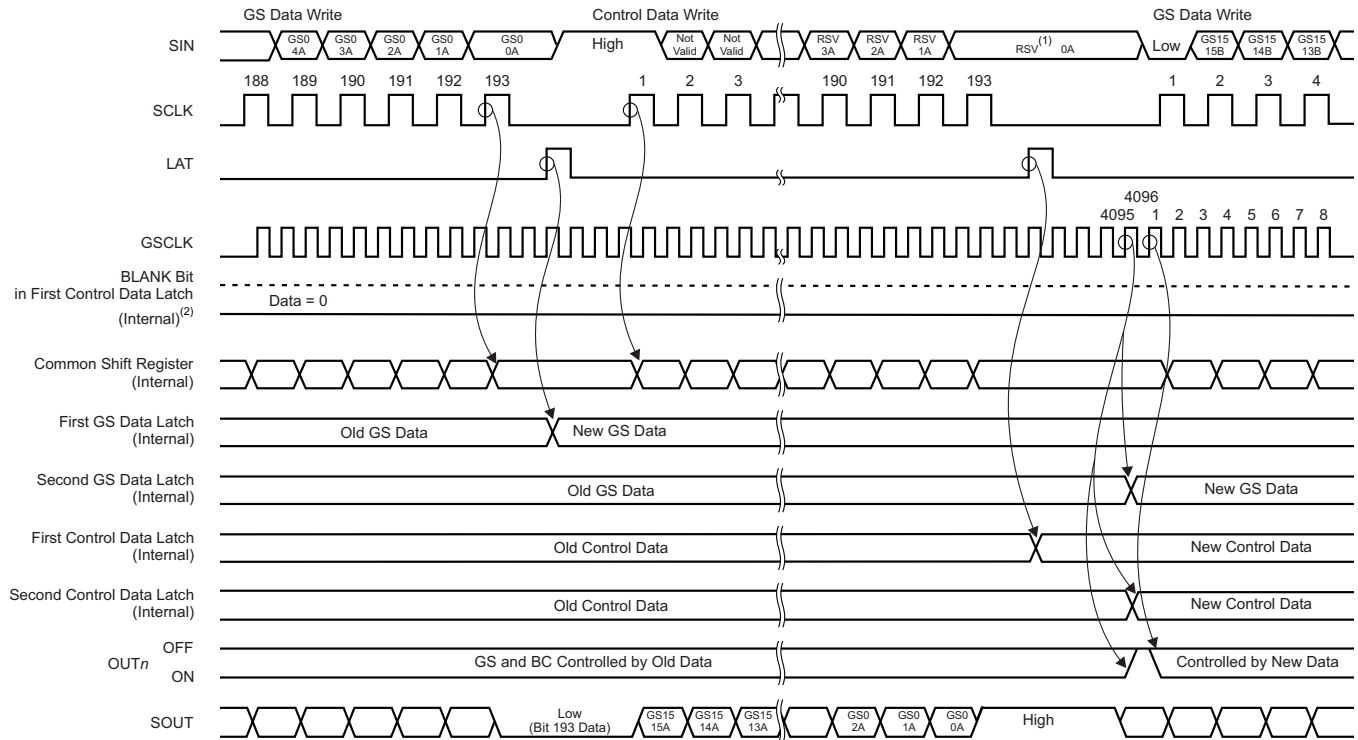


(1) OUTn is not turned on until BLANK changes from '1' to '0' or until LAT changes from low to high for a GS data write with TMGRST = 1.

Figure 24. Auto Display Repeat Function

Auto Data Refresh Function

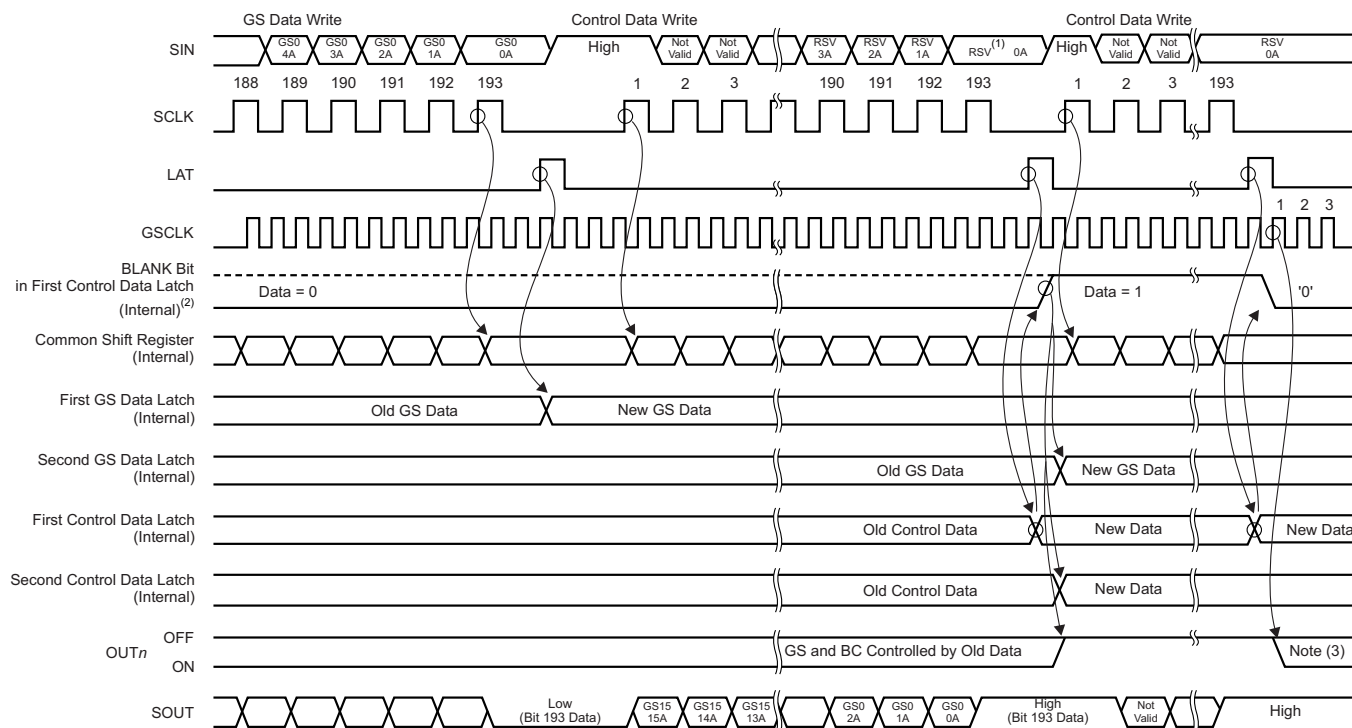
This function allows grayscale (GS) data and global brightness control (BC) data to be input at any time without synchronizing the input to the display timing. If GS and BC data are sent during a display period, the input data are held in the first latch for each data register. The data are then transferred to the second latch when the 4096th GSCLK occurs. The second latch data are used for the next display period. Refer to Figure 25 and Figure 26 for the auto data refresh function timing. However, when the BLANK bit in the first control data latch is set to '1' before the 4096th GSCLK occurs, the first latch data immediately upload to the second latch. Also, when a LAT rising edge occurs while the BLANK bit is '1', the selected shift register data are transferred to the first and second latch at the same time. The data of bits 119-136 (BLANK, DSPRPT, TMGRST, ESPWM, LODVLT, LSDVLT, LATTMG, IDMENA, IDMRPT, IDMCUR, OLDEN, and PSMODE) in the control data latch immediately update whenever the data are written into the first latch.



(1) RSV = reserved.

(2) BLANK data do not change with Auto Display Repeat enabled.

Figure 25. Auto Data Refresh Function 1



(1) RSV = reserved.

(2) The BLANK bit value is changed after the LAT rising edge.

(3) GS and BC are controlled by new data.

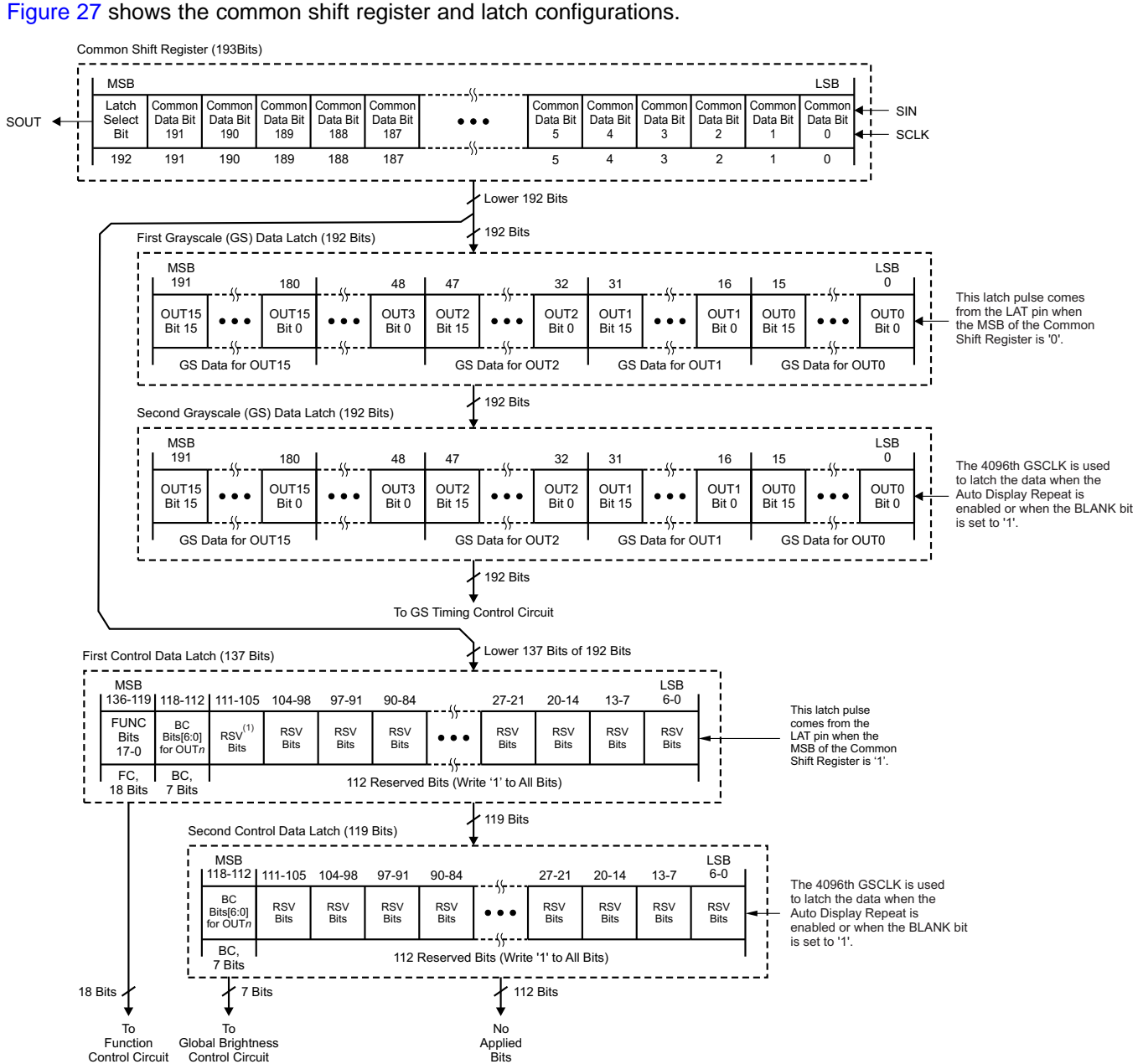
Figure 26. Auto Data Refresh Function 2

Display Timing Reset Function

The display timing reset function allows initializing the display timing with a LAT rising edge for a GS data write. This function can be switched on or off with the TMGRST bit in the first control data latch. When the TMGRST bit is '1', the GS counter is reset to '0' and all outputs are forced off at the LAT rising edge for a GS data write. Furthermore, the data in the 193-bit common shift register are copied to the first and second GS data latches at the same time. In addition, the BC data in the first control data latch are transferred to the second data latch simultaneously. This configuration is identical to the BLANK bit when it changes data from '0' to '1' and '1' to '0'. Therefore, the BLANK bit is not required to control the display reset. PWM control resumes from the next GSCLK rising edge. When the TMGRST bit is '0', the GS counter is not reset and the outputs are not forced off even with a LAT rising edge.

REGISTER AND DATA LATCH CONFIGURATION

The TLC5949 has one common shift register and two pairs of data latches: the first and second grayscale (GS) data latches and the first and second control data latches. The common shift register is 193 bits long and the GS data latches are 192 bits long in total. The first control data latch is 137 bits long and the second latch is 119 bits long. When the common shift register MSB is '0', the least significant 256 bits from the common shift register are latched into the first GS data latch. When the MSB is '1', the data are latched into the common control data latch. [Figure 27](#) shows the common shift register and latch configurations.



(1) RSV = reserved.

Figure 27. Common Shift Register and Control Data Latches Configuration

193-Bit Common Shift Register

The 193-bit common shift register is used to shift data from the SIN pin into the TLC5949. The data shifted into the register are used for GS and global BC functions. The common shift register LSB is connected to SIN and the MSB is connected to SOUT. On each SCLK rising edge, the data on SIN are shifted into the LSB and all 193 bits are shifted towards the MSB. The register MSB is always connected to SOUT. When the device is powered up, the data in the 193-bit common shift register are random.

First and Second Grayscale (GS) Data Latch

The first and second GS data latches are each 192 bits long, and set the PWM timing for each constant-current output. The on-time of all constant-current outputs is controlled by the data in the second GS data latch. A LAT rising edge when the common shift register MSB is '0' shifts the least significant 192 bits of the common shift register into the first GS latch. The GS data from the first latch are copied into the second latch either when the 4096th GSCLK occurs with the auto display repeat mode enabled, a LAT rising edge for a GS data write occurs with the display timing reset mode enabled, or the BLANK bit in the first control data latch is set to '1'.

When the device is powered up, the data in the first and second latches are random. Therefore, GS data must be written to the GS data latches before turning on the constant-current output. The first and second GS data latch configurations are shown in Figure 28. The data bit assignment is shown in Table 5.

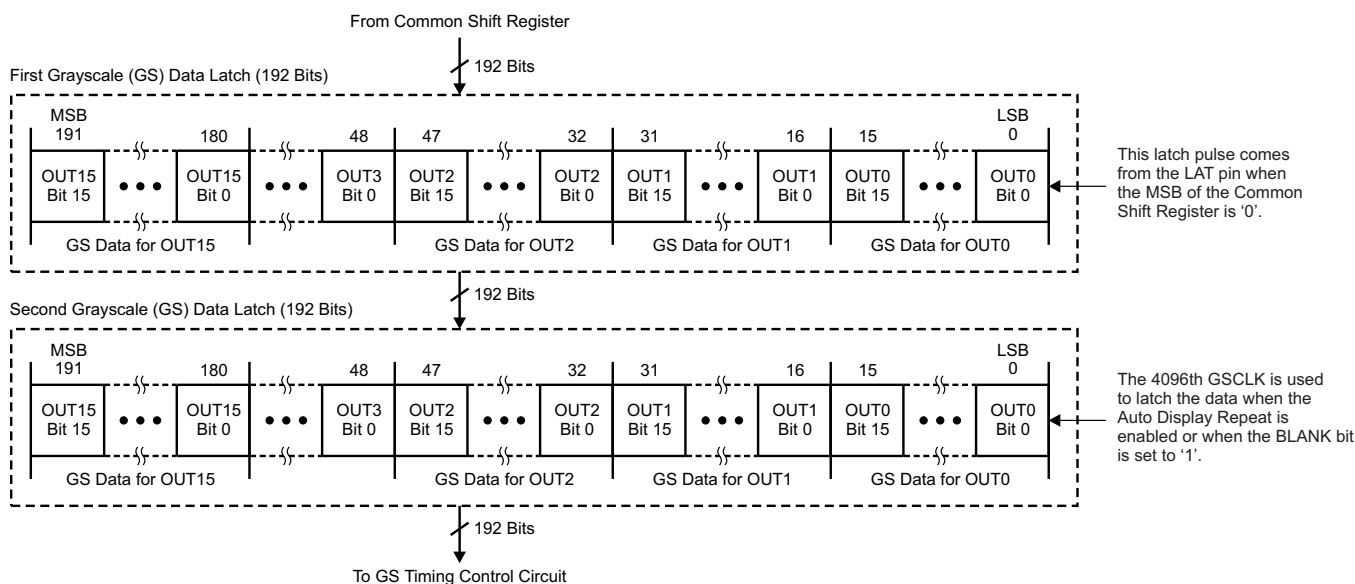


Figure 28. First and Second Grayscale Data Latch Configuration

Table 5. Grayscale Data Latch Bit Description

GS DATA LATCH BIT NUMBER	BIT NAME	CONTROLLED CHANNEL	GS DATA LATCH BIT NUMBER	BIT NAME	CONTROLLED CHANNEL
11-0	GSOUT0	Bits 11 to 0 for OUT0	107-96	GSOUT8	Bits 11 to 0 for OUT8
23-12	GSOUT1	Bits 11 to 0 for OUT1	119-108	GSOUT9	Bits 11 to 0 for OUT9
35-24	GSOUT2	Bits 11 to 0 for OUT2	131-120	GSOUT10	Bits 11 to 0 for OUT10
47-36	GSOUT3	Bits 11 to 0 for OUT3	143-132	GSOUT11	Bits 11 to 0 for OUT11
59-48	GSOUT4	Bits 11 to 0 for OUT4	155-144	GSOUT12	Bits 11 to 0 for OUT12
71-60	GSOUT5	Bits 11 to 0 for OUT5	167-156	GSOUT13	Bits 11 to 0 for OUT13
83-72	GSOUT6	Bits 11 to 0 for OUT6	179-168	GSOUT14	Bits 11 to 0 for OUT14
95-84	GSOUT7	Bits 11 to 0 for OUT7	191-180	GSOUT15	Bits 11 to 0 for OUT15

First and Second Control Data Latch

The first and second control data latches are 137 bits and 119 bits long, respectively. The first latch contains global brightness control (BC) data and function control (FC) data; the second latch contains global BC data. The DC for each constant-current output and the BC for all constant-current outputs are controlled by the second control data latch. The control data in the first latch are set by the least significant 137 bits from the common shift register at the LAT rising edge when the common shift register MSB is '1'. The 119 bits of BC data from the first control data latch are copied to the second latch when the 4096th GSCLK occurs or when the BLANK bit in the first control data latch is set to '1'.

When the device is powered up, the data in the first latch (except the BLANK and PSMODE bits of the FC bits) and second latch are random. Therefore, BC and FC data must be written to the first and second control data latches before turning on the constant-current outputs. The default value of the BLANK bit is '1'. The first and second control data latch configurations are shown in [Figure 29](#).

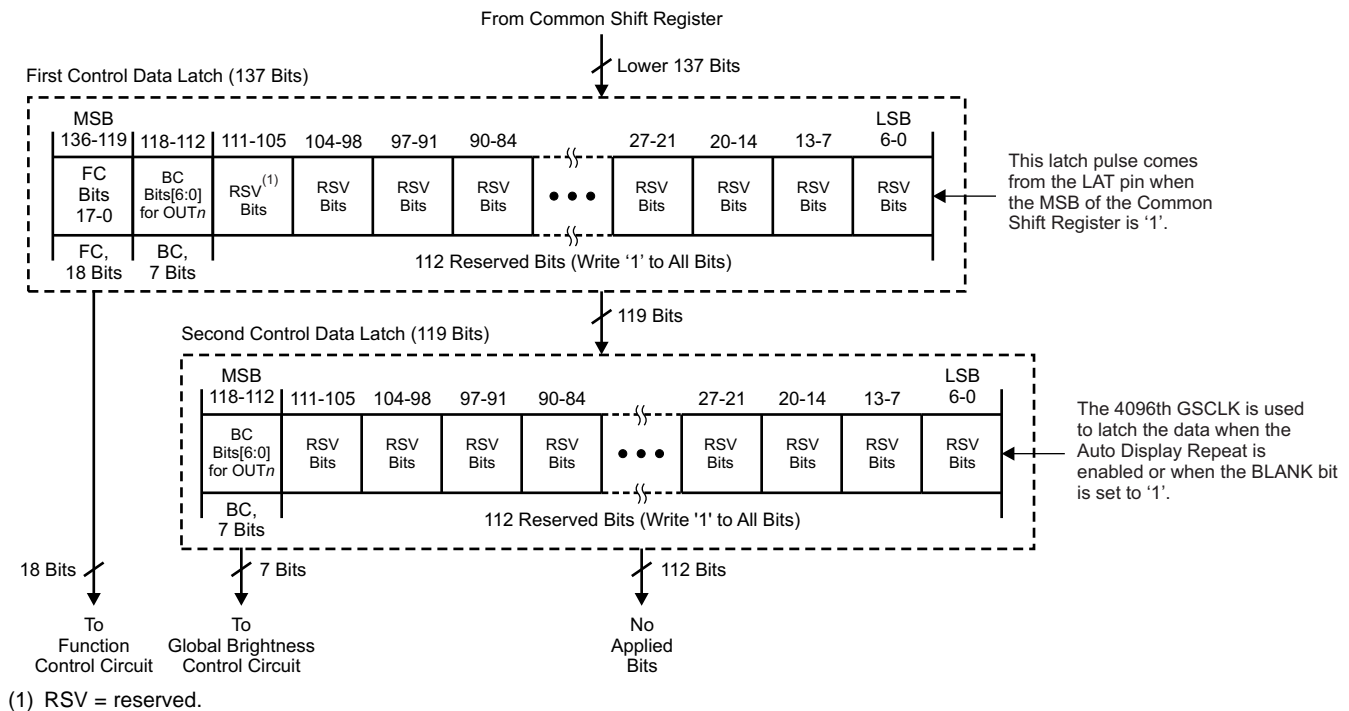


Figure 29. First and Second Control Data (BC and FC) Latch Configuration

Global Brightness Control (BC) Data

Global BC data are seven bits long. The global brightness for all outputs is controlled by the second control data latch. The data are used to adjust the constant-current values for the 16 constant-current outputs. As explained in the [Global Brightness Control \(BC\) Function](#) section, the BC values are used to adjust the output current from 25% to 100% of the maximum value. The global BC data bit assignment in the first and second latches is shown in [Table 6](#). [Table 2](#) summarizes the BC data value versus set current value.

Table 6. Global Brightness Control Data Bit Assignment in the Control Data Latch

BIT NUMBER	BIT NAME	CONTROLLED CHANNEL
118-112	BC	BC[6:0] bits for all channels (OUT0-OUT15)

Function Control (FC) Data Latch

The FC data latch is 13 bits long. This latch enables the constant-current outputs, enables the auto display repeat and display timing reset functions, and sets the PWM control mode and the LOD, LSD, and OLD data latch timing. Each function is selected by the first control data latch. When the device is powered on, the FC data in the first control data latch are random (except the BLANK and PSMODE bits) in order to disable all constant-current outputs. The FC data bit assignment in the first control data latch is shown in [Table 7](#).

Table 7. Function Control Data Latch Bit Description

BIT NUMBER	BIT NAME	DEFAULT VALUE (Binary)	DESCRIPTION
119	BLANK	1	Constant-current output blank bit 0 = On, 1 = Off When this bit is '0', all constant-current outputs (OUT0-OUT15) are controlled by the GS PWM timing controller. When this bit is '1', all constant-current outputs are forced off, the GS counter is reset to '0', and the GS PWM timing controller is initialized. When the device is powered on, this bit is set to '1'.
120	DSPRPT	—	Auto display repeat mode enable bit 0 = Disabled, 1 = Enabled When this bit is '0', the auto display repeat function is disabled. Each constant-current output is turned on and off for one display period after the BLANK bit is set to '0'. When this bit is '1', each output is repeated every 4096 GS clocks. When the device is powered on, this bit is random.
121	TMGRST	—	Display timing reset mode enable bit 0 = Disabled, 1 = Enabled When this bit is '0', the GS counter is not reset and the outputs are not forced off even with a LAT rising edge. When this bit is '1', the GS counter is reset to '0' and all outputs are forced off at the LAT rising edge for a GS data write. This function is identical to the BLANK bit. Therefore, a BLANK bit data change is not required to control the outputs from a controller. PWM control resumes from the next GSCLK rising edge. When the device is powered on, this bit is random.
122	ESPWM	—	ES-PWM mode enable bit 0 = Disabled, 1 = Enabled When this bit is '0', the conventional PWM control mode is selected. When this bit is '1', ES-PWM control mode is selected. If the TLC5949 is used for multiplexing a drive, the conventional PWM mode should be selected to prevent excess on/off switching. When the device is powered on, this bit is random.
123, 124	LODVLTL	—	LOD detection voltage selection bits LED open detection (LOD) detects a fault caused by an open LED by comparing the OUT _n voltage to the LOD detection threshold voltage. The threshold voltage is selected with these bits. Refer to Table 8 for the detect voltage truth table. When the device is powered on, this bit is random.
125, 126	LSDVLTL	—	LSD detection voltage selection bits LED short detection (LSD) detects a fault caused by a shorted LED by comparing the OUT _n voltage to the LSD detection threshold voltage. The threshold voltage is selected by these bits. Refer to Table 9 for the detect voltage truth table. When the device is powered on, this bit is random.
127, 128	LATTMG	—	LOD and LSD data reading timing selection bits The LOD and LSD data reading time is selected by these bits. When DSPRPT is '1' and IDMRPT is '0', LOD and LSD data are loaded to the LOD and LSD data latch one time only after new GS data are written into the second GS data latch. Refer to Table 10 for the data load timing truth table. When the device is powered on, this bit is random.

Table 7. Function Control Data Latch Bit Description (continued)

BIT NUMBER	BIT NAME	DEFAULT VALUE (Binary)	DESCRIPTION
129	IDMENA	—	<p>Invisible detection mode (IDM) enable bit 0 = Disabled, 1 = Enabled When this bit is '0', IDM is disabled. Therefore, LOD and LSD check LED status only at power-up. When this bit is '1', LOD and LSD check LED status with very small current sinking at OUT_n in a specific display segment. LOD and LSD can be checked even if OUT_n is off. The current value is set by the IDMCUR bits (bits 132, 131) and the time is set by the LATTMG bits (bits 128, 127) in the function control data latch. Furthermore, the IDM operation is repeated every display period with auto display mode enabled when the IDMRPT bit (bit 130) is set to '1'. When the device is powered on, this bit is random.</p>
130	IDMRPT	—	<p>Invisible detection mode (IDM) repeat bit 0 = Not repeated, 1 = Repeated When this bit is '0', IDM is not repeated. Therefore, LOD and LSD check LED status only one time after the BLANK bit is changed from '1' to '0'. Otherwise, LAT is input for a GS write when TMGRST is '1' or the GS counter is reset at power-up only one time at the time programmed by LATTMG. IDM is disabled when IDMENA is set to '0' even if this bit is '1'. When this bit is '1', IDM operation is repeated every display period with the auto display mode enabled. LOD and LSD check LED status at OUT_n every display period even if OUT_n is off. When the device is powered on, this bit is random.</p>
131, 132	IDMCUR	—	<p>Invisible detection mode (IDM) current select bits The OUT_n sink current for IDM can be selected with these bits. Refer to Table 11 for the IDM sink current truth table. When the device is powered on, these bits are random.</p>
133	OLDENA	—	<p>Output leak detection mode (OLD) enable bit 0 = Disabled, 1 = Enabled When this bit is '0', OLD is not checked and all OLD bits in the status information data (SID) are set to '0'. OLD data are loaded into the OLD data latch at the 4095th GS clock. OLD data in SID may show the result of the previous display period, depending on the LAT input timing. When this bit is '1', OLD checks the LED status with a small current sourced through OUT_n in a display segment. OLD only checks OUT_n with GS data set to '0'. When OUT_n current leakage is detected, the OLD bit that corresponds to the leaking output is set to '1' in the SID. When IDMENA is '1', OLD operation is disabled even if the OLDENA bit is set to '1' because OLD cannot obtain a correct result when IDM is enabled. When the device is powered on, this bit is random.</p>
134-136	PSMODE	111	<p>Power-save mode (PSM) selection bits The power-save mode is selected with these bits. Refer to Table 12 and Table 13 for the PSM truth tables. When the device is powered on, these bits are all set to '1'.</p>

Table 8. LOD Threshold Voltage Truth Table

LODVLT		LED OPEN DETECTION (LOD) THRESHOLD VOLTAGE
BIT 124	BIT 123	
0	0	VLOD0 (0.3 V, typ)
0	1	VLOD1 (0.6 V, typ)
1	0	VLOD2 (0.9 V, typ)
1	1	VLOD3 (1.2 V, typ)

Table 9. LSD Threshold Voltage Truth Table

LSDVLT		LED SHORT DETECTION (LSD) THRESHOLD VOLTAGE
BIT 126	BIT 125	
0	0	VLSD0 (0.35 × VCC, typ)
0	1	VLSD1 (0.45 × VCC, typ)
1	0	VLSD2 (0.55 × VCC, typ)
1	1	VLSD3 (0.65 × VCC, typ)

Table 10. LOD and LSD Data Latch Time Truth Table

LATMG		LOD and LSD DATA LATCH TIMING
BIT 128	BIT 127	
0	0	17th GSCLK after BLANK bit is changed to '0' or GS counter is reset. ⁽¹⁾
0	1	33rd GSCLK after BLANK bit is changed to '0' or GS counter is reset. ⁽¹⁾
1	0	65th GSCLK after BLANK bit is changed to '0' or GS counter is reset. ⁽¹⁾
1	1	129th GSCLK after BLANK bit is changed to '0' or GS counter is reset. ⁽¹⁾

- (1) When DSPRPT is '1' and IDMRPT is '0', the resulting LOD and LSD data are loaded to the LOD and LSD data latch only one time after new GS data are written into the second GS data latch.

Table 11. IDM Sink Current Truth Table

IDMCUR		INVISIBLE DETECTION MODE (IDM) SINK CURRENT
BIT 132	BIT 131	
0	0	2 μA (typ)
0	1	10 μA (typ)
1	0	20 μA (typ)
1	1	1 mA (typ)

Table 12. PSM Select Truth Table: Bits 135, 134

PSMODE		POWER-SAVE MODE (PSM) FUNCTION
BIT 135	BIT 134	
0	0	Power-save mode is disabled in every condition
0	1	When all '0's are written into the second GS data latch, the device goes into power-save mode. When an SCLK rising edge occurs, the device goes to normal operation and starts to control the output current. However, some recovery time (t_{D7}) is required to resume normal operation after an SCLK rising edge.
1	0	When all '0's are written into the second GS data latch, the device goes into power-save mode. When the data (except all '0's) are written into the second GS data latch, the device goes to normal operation and starts to control the output current. However, some recovery time (t_{D7}) is required to resume normal operation after the data changes.
1 (default)	1 (default)	Power-save mode is enabled in every condition. When the device is powered up, this mode is selected.

Table 13. PSM Select Truth Table: Bit 136

PSMODE	POWER-SAVE MODE (PSM) FUNCTION
BIT 136	
0	The GSCLK signal is used for GS timing control in the same manner as in normal mode even if the device is in power-save mode.
1 (default)	When the device is in power-save mode, the GSCLK signal is forced low internally and GS timing control logic is not operational in order to reduce power consumption. However, if the lower two bits of PSMODE (bits 135, 134) are set to '0', the GSCLK signal is not forced low because the PSM is disabled. When the device is powered up, this mode is selected.

STATUS INFORMATION DATA (SID)

The status information data (SID) contain the status of the LED open detection (LOD), LED short detection (LSD), output leakage detection (OLD), pre-thermal warning (PTW), thermal error flag (TEF), and IREF short flag (ISF). When the LAT rising edge for a GS data write is input, the SID overwrite the common shift register data after the data in the common shift register are copied to the GS latch. If the common shift register MSB is '1', the SID data are not copied to the common shift register.

After being copied into the common shift register, new SID data cannot be copied until at least one new bit of data is written into the common shift register. Otherwise, the LAT signal is ignored. To recheck SID without changing the GS data, reprogram the common shift register with the same data currently programmed into the GS latch. When LAT goes high, the GS data do not change, but the SID data are loaded into the common shift register. LOD, LSD, OLD, PTW, TEF, and ISF are shifted out of SOUT with each SCLK rising edge. The SID load configuration and SID read timing are shown in Figure 30 and Table 14, respectively.

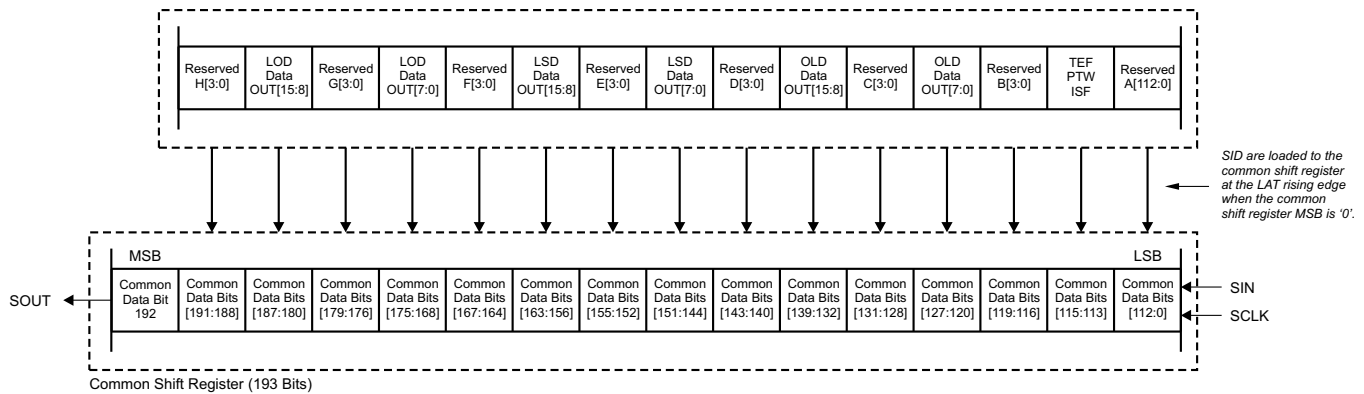


Figure 30. SID Load Configuration

Table 14. SID Load Description

COMMON SHIFT REGISTER BIT NUMBER	LOADED SID DESCRIPTION
Bits[112:0]	Reserved data. These 113 bits of data are not set and can be '0' or '1'.
Bit 113	IREF short flag (ISF) data; 1-bit data. 0 = Normal operation (default) 1 = IREF terminal connected to GND with low resistance
Bit 114	Pre-thermal warning (PTW) data; 1-bit data. 0 = Normal operation (default) 1 = Higher temperature condition than the detected PTW temperature range
Bit 115	Thermal error flag (TEF) data; 1-bit data. 0 = Normal operation (default) 1 = Higher temperature condition than the detected TEF temperature range
Bits[119:116]	Reserved data. These four bits of data are not set and can be either '0' or '1'.
Bits[127:120]	Output leakage detection (OLD) data bit for OUT0 to OUT7. The 8-bit data bit assignment of the output channel is: Bit 120 = OUT0 OLD Bit 121 = OUT1 OLD ... Bit 126 = OUT6 OLD Bit 127 = OUT7 OLD 0 = Normal operation (default) 1 = LED current leaks to GND when the output is off
Bits[131:128]	Reserved data. These four bits of data are not set and can be either '0' or '1'.

Table 14. SID Load Description (continued)

COMMON SHIFT REGISTER BIT NUMBER	LOADED SID DESCRIPTION
Bits[139:132]	Output leakage detection (OLD) data bit for OUT8 to OUT15. The 8-bit data bit assignment of the output channel is: Bit 132 = OUT8 OLD Bit 133 = OUT9 OLD ... Bit 138 = OUT14 OLD Bit 139 = OUT15 OLD 0 = Normal operation (default) 1 = Output current leaks to GND when the output is off
Bits[143:140]	Reserved data. These four bits of data are not set and can be either '0' or '1'.
Bits[151:144]	LED short detection (LSD) data bit for OUT0 to OUT7. The 8-bit data bit assignment of the output channel is: Bit 144 = OUT0 LSD Bit 145 = OUT1 LSD ... Bit 150 = OUT6 LSD Bit 151 = OUT7 LSD 0 = Normal operation (default) 1 = LED is shorted
Bits[155:152]	Reserved data. These four bits of data are not set and can be either '0' or '1'.
Bits[163:156]	LED short detection (LSD) data bit for OUT8 to OUT15. The 8-bit data bit assignment of the output channel is: Bit 156 = OUT8 LSD Bit 157 = OUT9 LSD ... Bit 162 = OUT14 LSD Bit 163 = OUT15 LSD 0 = Normal operation (default) 1 = LED is shorted
Bits[167:164]	Reserved data. These four bits of data are not set and can be either '0' or '1'.
Bits[175:168]	LED open detection (LOD) data bit for OUT0 to OUT7. The 8-bit data bit assignment of the output channel is: Bit 168 = OUT0 LOD Bit 169 = OUT1 LOD ... Bit 174 = OUT6 LOD Bit 175 = OUT7 LOD 0 = Normal operation (default) 1 = LED is open or connected to GND with low resistance
Bits[179:176]	Reserved data. These four bits of data are not set and can be either '0' or '1'.
Bits[187:180]	LED open detection (LOD) data bit for OUT8 to OUT15. The 8-bit data bit assignment of the output channel is: Bit 180 = OUT8 LOD Bit 181 = OUT9 LOD ... Bit 186 = OUT14 LOD Bit 187 = OUT15 LOD 0 = Normal operation (default) 1 = LED is open or connected to GND with low resistance
Bits[191:188]	Reserved data. These four bits of data are not set and can be either '0' or '1'.
Bit 192	No data loaded

LED OPEN DETECTION (LOD)

LOD detects a fault caused by an LED open circuit or a short from OUT_n to ground with low resistance by comparing the OUT_n voltage to the LOD detection threshold voltage. If the OUT_n voltage is lower than the threshold voltage (set by the LODVLT bits in the first control data latch) when OUT_n is on, that output LOD bit is set to '1' to indicate an open LED. Otherwise, the LOD bit is set to '0'. LOD data are only valid for outputs that are programmed to be on during the LOD data read selected by the LATTMG bits in the first control data latch. LOD data are latched into the LOD data latch when LOD data are read, as selected by LATTMG. LOD data for outputs programmed to be off at the LOD latch timing are always '0' when IDM is not enabled.

LED SHORT DETECTION (LSD)

LSD data detect a fault caused by a shorted LED by comparing the OUT_n voltage to the LSD detection threshold voltage level set by LSDVLT in the first control data latch. If the OUT_n voltage is higher than the programmed voltage when OUT_n is on, the corresponding output LSD bit is set to '1' to indicate a shorted LED. Otherwise, the LSD bit is set to '0'. LSD data are only valid for outputs that are programmed to be on when the LSD data are read, as selected by the LATTMG bits in the first control data latch. LSD data are latched into the LSD data latch when the LSD data are read, as selected by LATTMG. LSD data for outputs programmed to be off at the LSD latch timing are always '0' when IDM is not enabled.

OUTPUT LEAKAGE DETECTION (OLD)

OLD detects a fault caused by a short with high resistance from OUT_n to GND by comparing the OUT_n voltage to the LSD detection threshold voltage when the output is off. A small current is sourced from OUT_n to detect LED leakage. OLD operation can be disabled by the OLDENA bit. Also, OLD is disabled when the invisible detection mode (IDM) is enabled (see the [Invisible Detection Mode](#) section). If the OUT_n voltage is lower than the programmed LSD threshold voltage, the corresponding output OLD bit is set to '1' to indicate a leaking LED. Otherwise, the OLD bit is set to '0'. The OLD result is valid for disabled outputs only. The OLD data are latched into the OLD data latch at the end of the display period or when BLANK is changed to '1'. Also, the OLD data are latched when the GS data are written if the display timing reset is enabled. OLD data always read '0' when the output GS is not '0', or when OLD is disabled.

INVISIBLE DETECTION MODE (IDM)

IDM can detect LOD and LSD without dependency upon GS data. When the IDM bit in the function control data latch is set, OUT_n starts sinking the current set by the IDMCUR bits in the function control latch at the first GSCLK; the IDM sink current is turned off at the GSCLK programmed by LATTMG. When the IDM current is turned off, LOD and LSD data are latched into the LOD and LSD data latch. During the IDM timing, the original PWM control continues. When the IDM bit in the control data latch is set to '0', the OUT_n on/off timing is only controlled by GS data.

LOD and LSD data are not valid for approximately 1 μ s after the constant-current output turns on. Therefore, GS data must be set to turn on the output for at least 1 μ s. Furthermore, the LOD and LSD latch timing bits (LATTMG) should be set as shown in [Equation 4](#):

The number of GSCLKs required to obtain a valid LOD and LSD = $1 \mu\text{s} / t_{\text{GSCLK}}$

where:

$$t_{\text{GSCLK}} = \text{one GSCLK period} \quad (4)$$

If the GSCLK frequency is 33 MHz, the outputs must be on for 33 GSCLK periods or more. Therefore, the LATTMG bits can only be set to '01', '10', or '11'. If the GSCLK frequency is 2 MHz, the outputs must be on for two or more GSCLK periods. In this case, the LATTMG bits can be set to any pattern.

When LOD and LSD data must be read with invisible brightness, the LATTMG bits should be set to the minimum data larger than the calculated number of GCLK periods defined by Equation 4. IDM does not work in power-save mode. Figure 31 shows the LOD, LSD, OLD, and IDM circuit and Table 15 shows a truth table for LOD, LSD, OLD, and IDM. Refer to Figure 32 for the PWM operation timing.

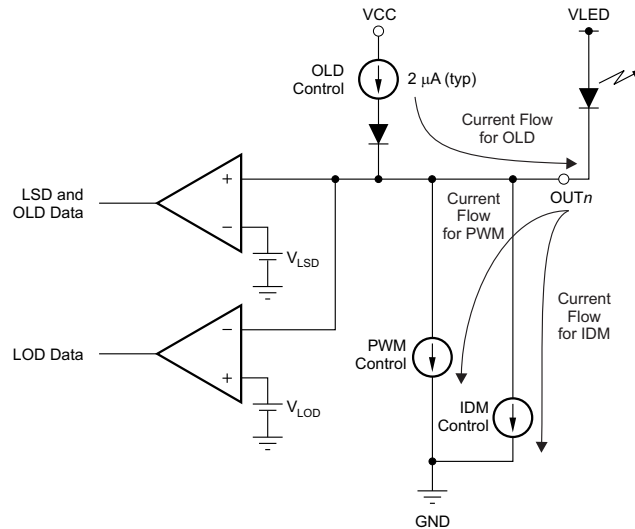
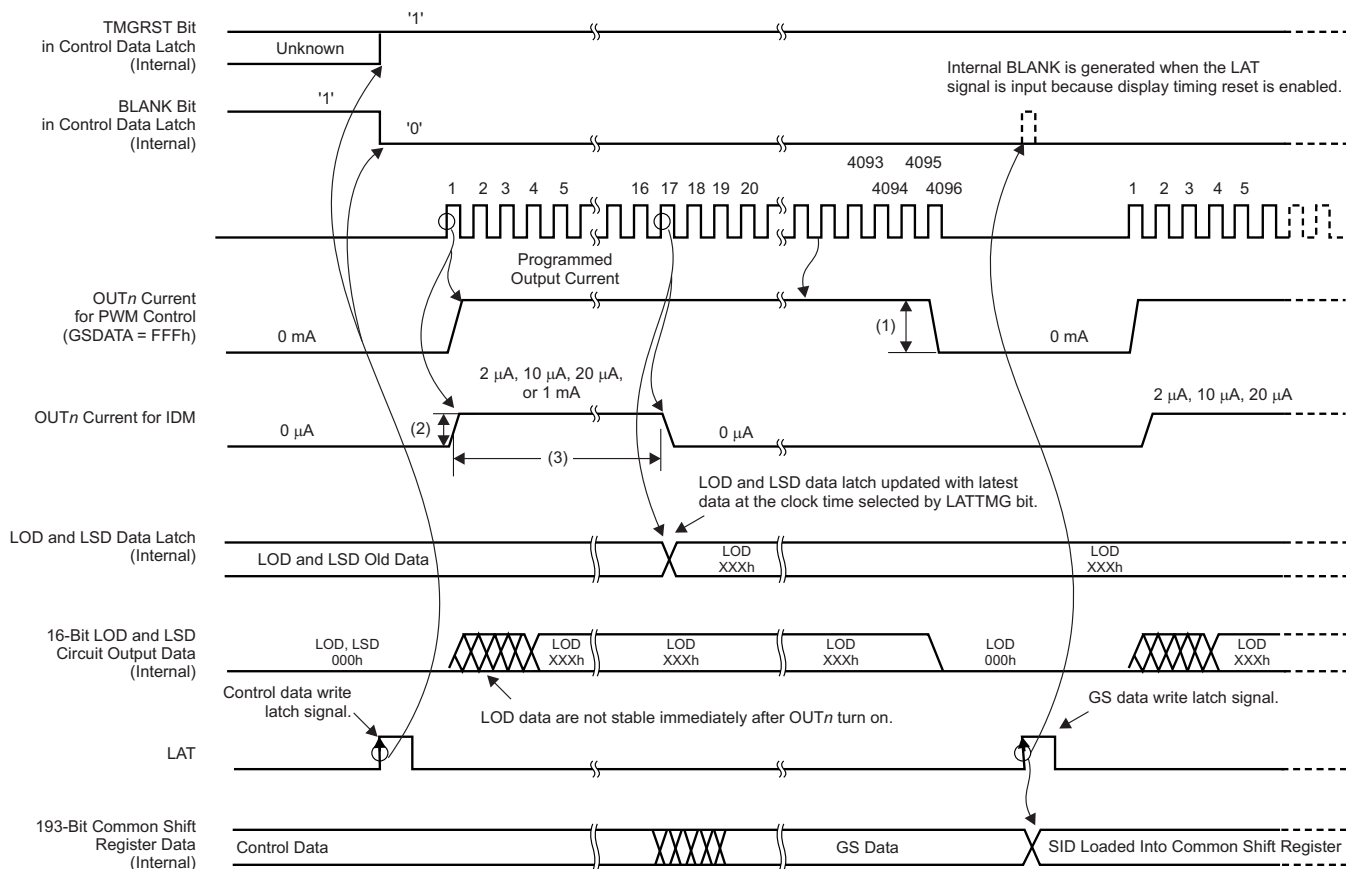


Figure 31. LOD, LSD, and OLD Circuit

Table 15. LOD, LSD, OLD, ISF, PTW, and TEF Truth Table

SID DATA	CONDITION					
	LOD	LSD	OLD	ISF	PTW	TEF
0	LED is not opened ($V_{OUTn} > V_{LOD}$)	LED is not shorted ($V_{OUTn} \leq V_{LSD}$)	OUTn does not leak to GND ($V_{OUTn} > V_{LSD}$ when constant-current output off and OUTn source current on)	IREF terminal is not shorted	Device temperature is lower than pre-thermal warning temperature (temperature $\leq T_{PTW}$)	Device temperature is lower than thermal shutdown threshold temperature (temperature $\leq T_{TEF}$)
1	LED is open or shorted to GND ($V_{OUTn} \leq V_{LOD}$)	LED is shorted between anode and cathode, or shorted to higher voltage side ($V_{OUTn} > V_{LSD}$)	Current leaks from OUTn to internal GND, or OUTn is shorted to external GND with high impedance ($V_{OUTn} \leq V_{LSD}$ when constant-current output off and OUTn source current on)	IREF terminal is shorted to GND with low impedance and OUTn are forced off	Device temperature is higher than pre-thermal warning temperature (temperature $> T_{PTW}$)	Device temperature is higher than thermal shutdown threshold temperature and driver is forced off (temperature $> T_{TEF}$)



- (1) Set the current with the external resistor and BC data.
- (2) Select the output current with the IDMCUR bit in the control data latch.
- (3) Select clock time with the LATTMG bit in the control data latch.

Figure 32. PWM Operation Timing

POWER-SAVE MODE (PSM)

The power-save mode control bits are assigned in the function control data latch. The device dissipation current becomes 10 μA (typ) in this mode. When the two lower bits in PSMODE are '01', '10', or '11', the power-save mode is enabled. When the lower two bits are '01' or '10', and if all '0' data are written in the second GS data latch, the TLC5949 goes into power-save mode. When an SCLK rising edge is generated with the lower two PSMODE bits (bits 135, 134) set to '01', the device leaves PSM for normal operation. OUT_n are turned on at the first GSCLK of the next display period after the device has left PSM. Figure 33 shows the power-save mode timing diagram.

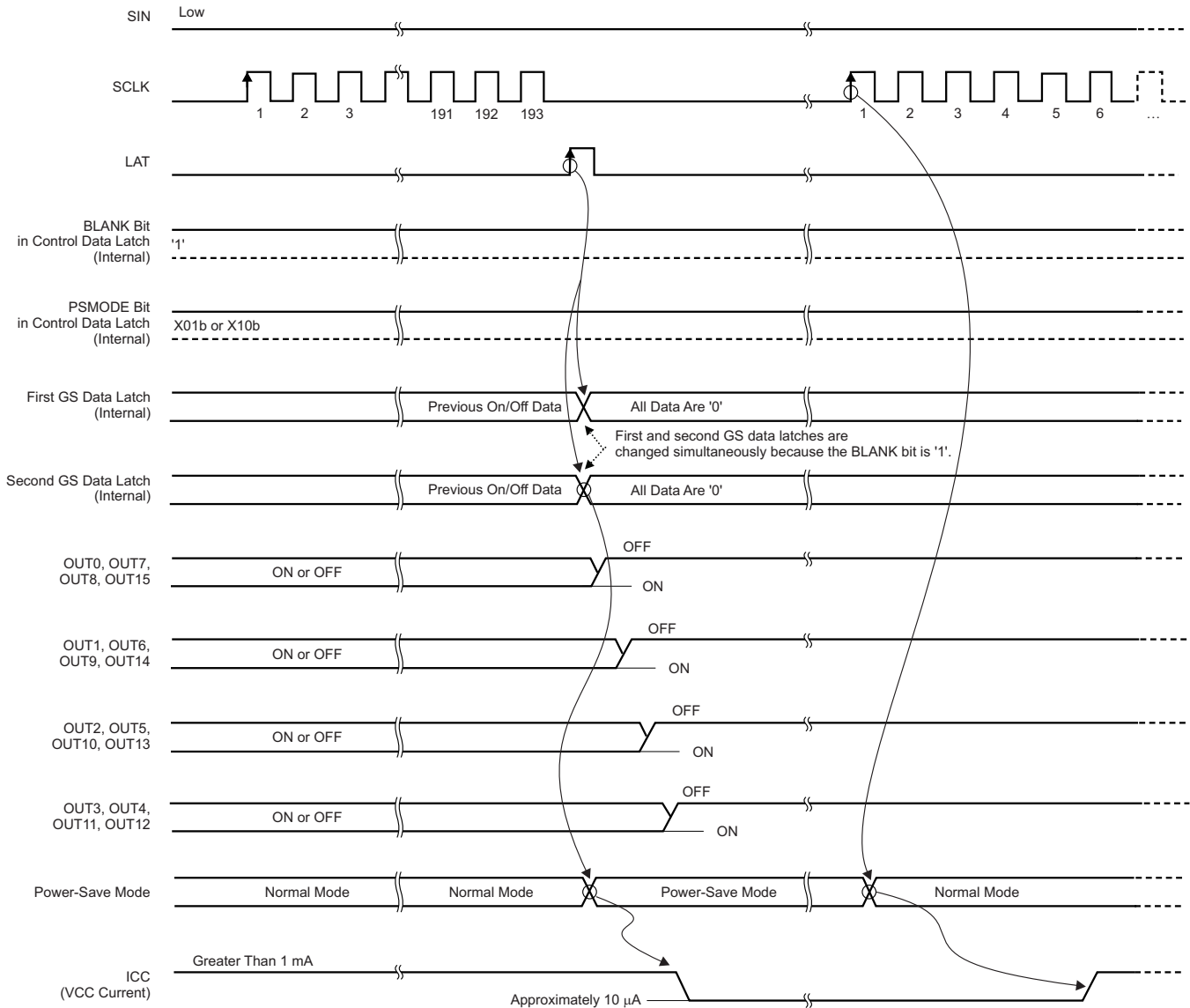


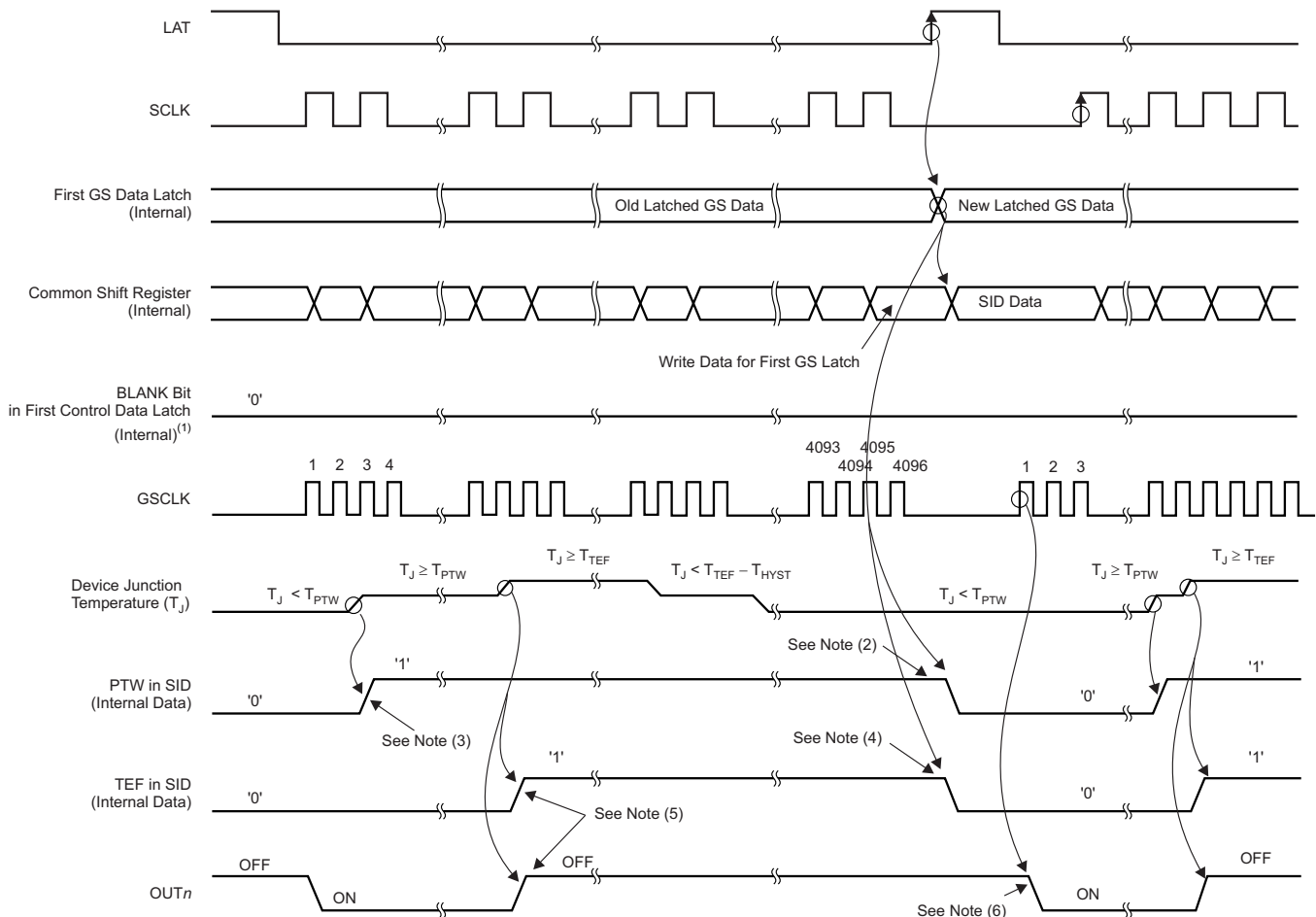
Figure 33. Power-Save Mode Timing (Bits 135 and 134 = 01)

CURRENT REFERENCE (IREF PIN) SHORT FLAG (ISF)

The ISF function indicates that the IREF terminal is shorted with low impedance to GND. The ISF bit in the SID is set to '1' during this condition. Then all outputs, OUT_n , are forced off. See Table 15 for the ISF truth table.

PRE-THERMAL WARNING (PTW)

The PTW function indicates that the device junction temperature is high. The PTW in the SID is set to '1' while the device junction temperature exceeds the temperature threshold ($T_{PTW} = +138^{\circ}\text{C}$, typ); however, the outputs are not forced off. When the PTW is set, the device temperature should be reduced by lowering the power dissipated in it to avoid a forced shutdown by the thermal shutdown circuit. This reduction can be accomplished by lowering the GS or BC data values. When the device junction temperature drops below the T_{PTW} temperature, the PTW bit in the SID is set to '0'. Figure 34 shows a timing diagram; see Table 15 for the PTW truth table.



- (1) This internal signal is reset when LAT is input for a GS write with the display timing reset enabled.
- (2) The PTW bit in SID is reset to '0' at the LAT rising edge for a GS data write if the device junction temperature is below t_{PTW} .
- (3) The PTW bit is set to '1' when the device junction temperature is greater than t_{PTW} .
- (4) The TEF bit in SID is reset to '0' at the LAT rising edge for a GS data write if the device junction temperature is below t_{TEF} .
- (5) OUT_0 to OUT_{15} are forced off when T_J exceeds t_{TEF} . Furthermore, the TEF bit is set to '1' at the same time.
- (6) OUT_0 to OUT_{15} are turned on at the first GSCLK rising edge if the device junction temperature is below t_{TEF} with BLANK set to '0'.

Figure 34. PTW, TEF, and TSD Timing

THERMAL SHUTDOWN (TSD) AND THERMAL ERROR FLAG (TEF)

The TSD function turns off all constant-current outputs on the device when the junction temperature (T_J) exceeds the threshold ($T_{TEF} = +165^{\circ}\text{C}$, typ) and sets TEF to '1'. All outputs are latched off when TEF is set to '1' and remain off at least until the next GS cycle starts and the junction temperature drops below ($T_{TEF} - T_{HYST}$). TEF remains '1' until a LAT rising edge occurs and the temperature is reduced. TEF is set to '0' when the junction temperature drops below ($T_{TEF} - T_{HYST}$), but the output does not turn on until the first GSCLK in the next display period occurs even if TEF is set to '0'. See [Figure 34](#) for a timing diagram; refer to [Table 15](#) for the TEF truth table.

NOISE REDUCTION

Large surge currents may flow through the device and the board on which the device is mounted if all 16 outputs turn on simultaneously at the start of each GS cycle. These large current surges could introduce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC5949 independently turns the outputs on with a delay for each group to provide a soft-start feature. The output current sinks are grouped into four groups in each color group. The first output group that is turned on/off are OUT0, OUT7, OUT8, and OUT15; the second output group is OUT1, OUT6, OUT9, and OUT14; the third output group is OUT2, OUT5, OUT10, and OUT13; and the fourth output group is OUT3, OUT4, OUT11, and OUT12. Each output group is turned on and off sequentially with a small delay between the groups. However, each output on/off is controlled by the GS clock.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2012) to Revision A	Page
• Changed product status from mixed status to production data	1
• Deleted footnote 1 and gray shading from DBQ rows in Package and Ordering Information table	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5949DBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5949	Samples
TLC5949PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5949	Samples
TLC5949PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5949	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5949DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5949PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

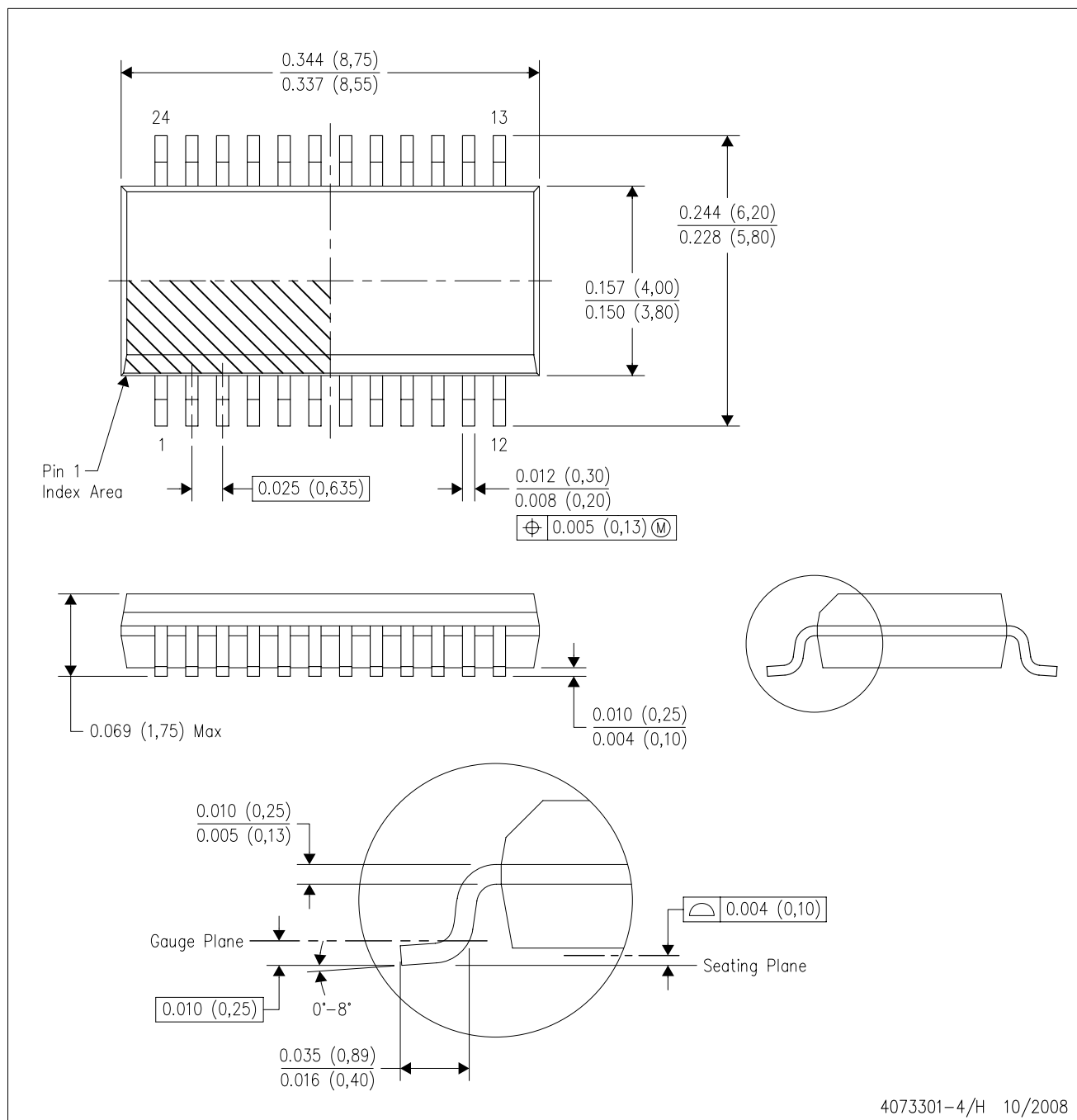


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5949DBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
TLC5949PWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0

DBQ (R-PDSO-G24)

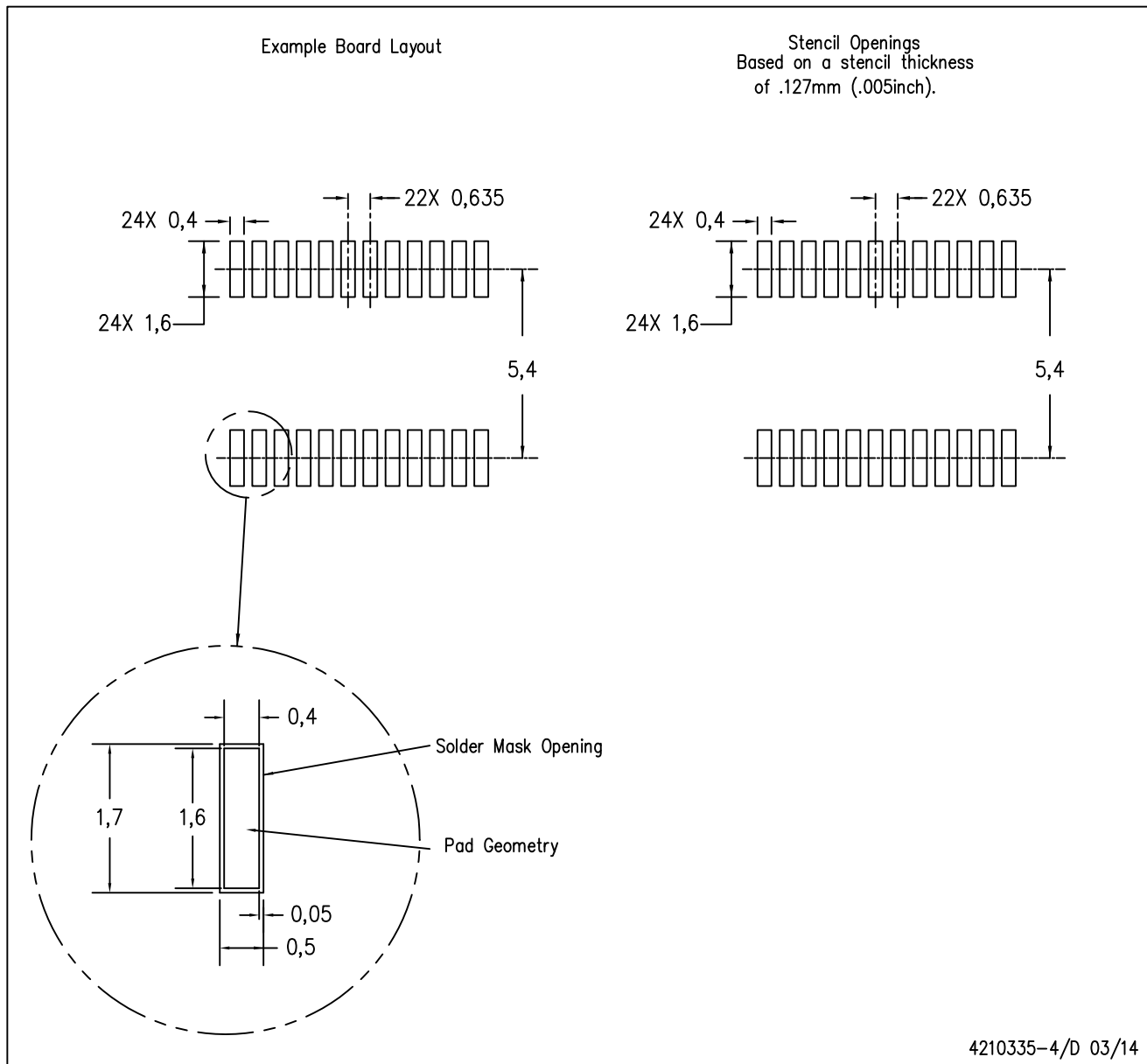
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.

DBQ (R-PDSO-G24)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

GENERIC PACKAGE VIEW

PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

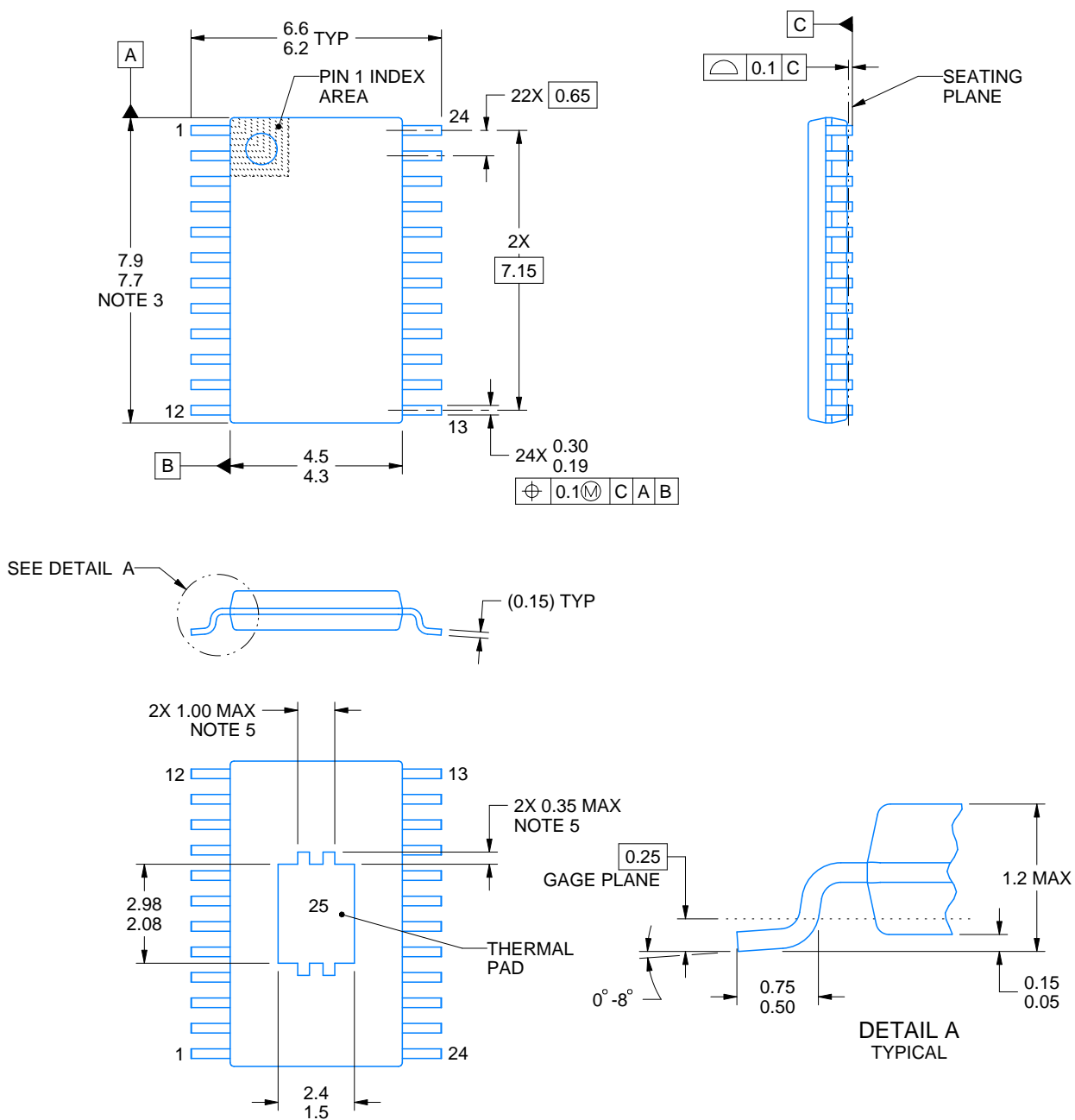
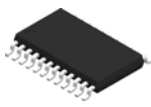
4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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4224478/A 10/2018

NOTES:

PowerPAD is a trademark of Texas Instruments.

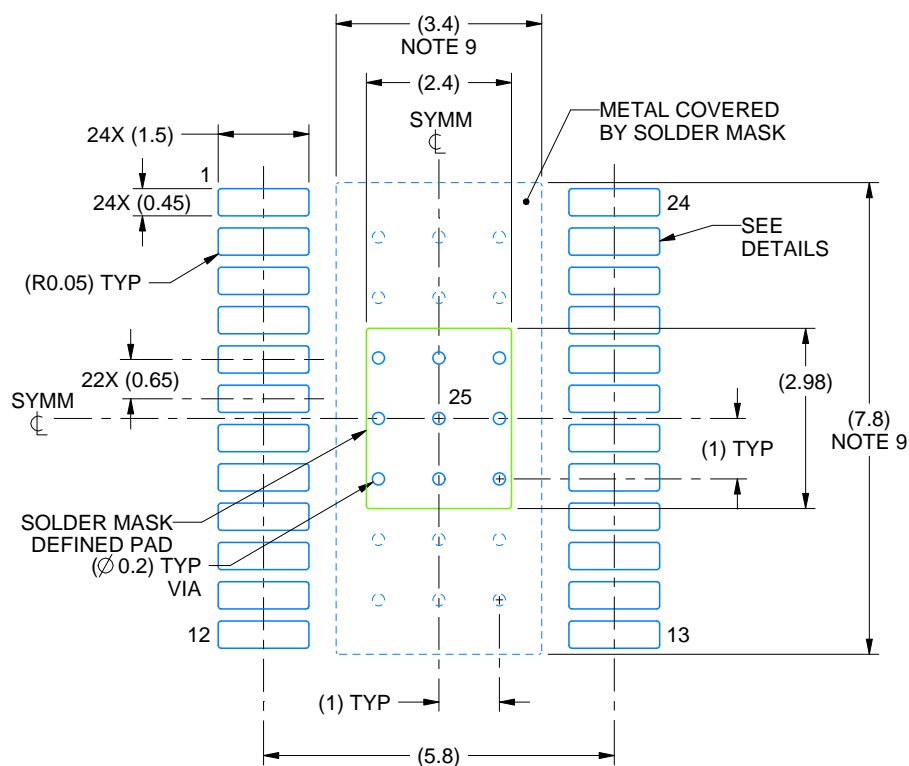
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

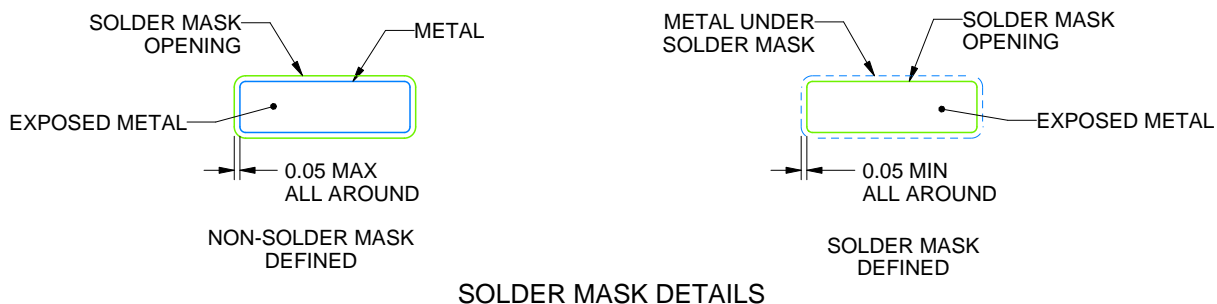
PWP0024P

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

4224478/A 10/2018

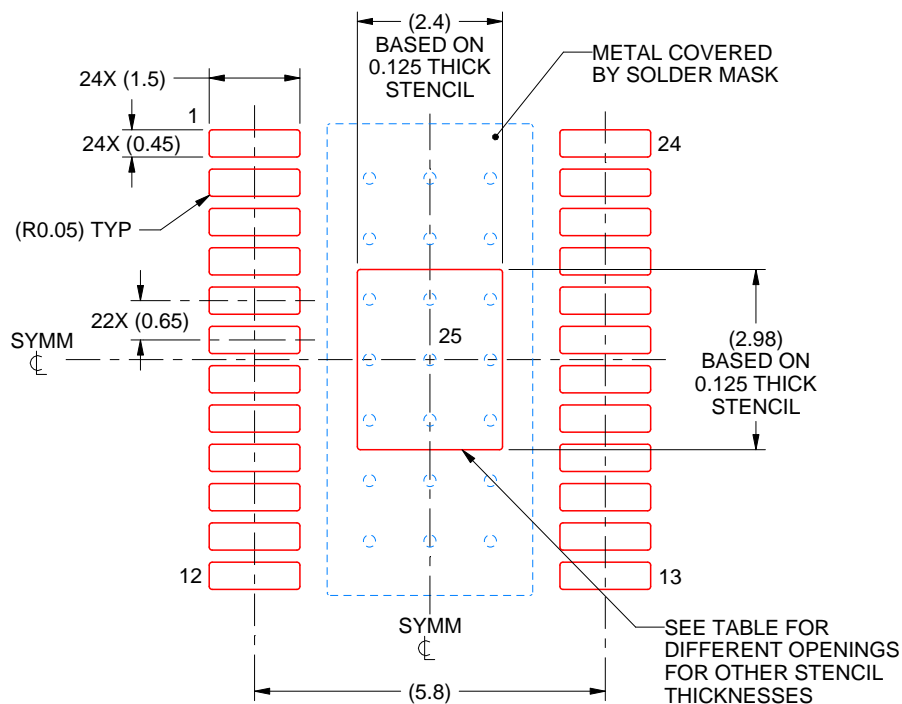
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

PWP0024P

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 3.33
0.125	2.40 X 2.98 (SHOWN)
0.15	2.19 X 2.72
0.175	2.03 X 2.52

4224478/A 10/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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