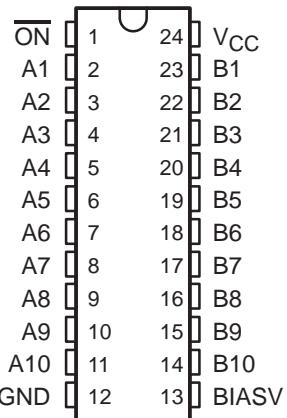


- 5- Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Power Off Disables Outputs, Permitting Live Insertion
- Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion
- Active-Clamp Undershoot-Protection Circuit on the I/Os Clamps Undershoots Down to -2 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBTK6800 device provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The A and B ports have an active-clamp undershoot-protection circuit. When there is an undershoot, the active-clamp circuit is enabled and current from V_{CC} is supplied to clamp the output, preventing the pass transistor from turning on.

The SN74CBTK6800 is organized as one 10-bit switch with a single enable ($\overline{\text{ON}}$) input. When $\overline{\text{ON}}$ is low, the switch is on, and port A is connected to port B. When $\overline{\text{ON}}$ is high, the switch between port A and port B is open. When $\overline{\text{ON}}$ is high or V_{CC} is 0 V, B port is precharged to BIASV through the equivalent of a 10-k Ω resistor.

ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – DW	Tube	SN74CBTK6800DW	CBTK6800
		Tape and reel	SN74CBTK6800DWR	
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBTK6800DBQR	CBTK6800
	TSSOP – PW	Tape and reel	SN74CBTK6800PWR	BK6800
	TVSOP – DGV	Tape and reel	SN74CBTK6800DGVR	BK6800

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

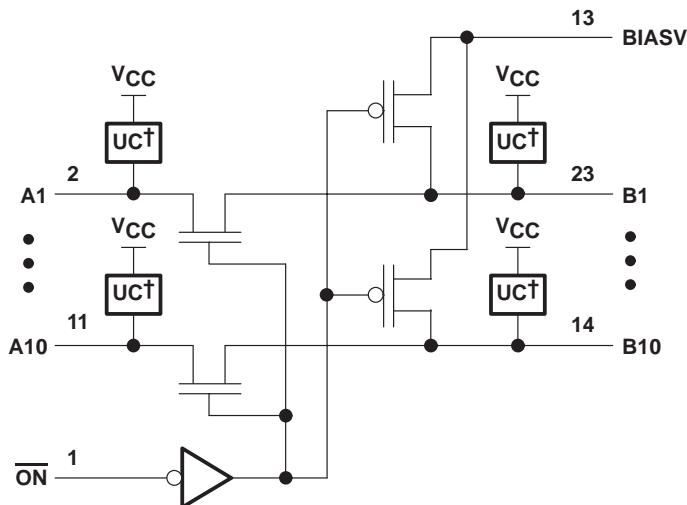
FUNCTION TABLE

INPUT $\overline{\text{ON}}$	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic diagram (positive logic)



† Undershoot clamp

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V _{CC}	-0.5 V to 7 V
Bias voltage range, BIASV	-0.5 V to 7 V
Input voltage range, V _I (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I _{IK} (V _I < 0)	-50 mA
Package thermal impedance, θ _{JA} (see Note 2):	
DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T _{stg}	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V _{CC} Supply voltage	4	5.5	V
BIAV Supply voltage	1.3	V _{CC}	V
V _{IH} High-level control input voltage	2		V
V _{IL} Low-level control input voltage		0.8	V
T _A Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$					-1.2	V
V_{IKU}		$V_{CC} = 5.5 \text{ V}$, $0 \text{ mA} \geq I_I \geq -50 \text{ mA}$, $\overline{OE} = 5.5 \text{ V}$					-2	V
I_I		$V_{CC} = 5.5 \text{ V}$, $V_I = 5.5 \text{ V}$ or GND					± 5	μA
I_{off}		$V_{CC} = 0$, V_I or $V_O = 0$ to 5.5 V , BIASV = Open					20	μA
I_O		$V_{CC} = 4.5 \text{ V}$, $V_O = 0$, BIASV = 2.4 V			0.25			mA
I_{CC}		$V_{CC} = 5.5 \text{ V}$, $V_I = V_{CC}$ or GND, $I_O = 0$					20	μA
ΔI_{CC}^\ddagger	Control inputs	$V_{CC} = 5.5 \text{ V}$, One input at 3.4 V , Other inputs at V_{CC} or GND					2.5	mA
C_i	Control inputs	$V_I = 3 \text{ V}$ or 0			3			pF
$C_o(\text{OFF})$		$V_O = 3 \text{ V}$ or 0, Switch off			8.5			pF
r_{on}^\S		$V_{CC} = 4 \text{ V}$, TYP at $V_{CC} = 4 \text{ V}$	$V_I = 2.4 \text{ V}$,	$I_I = 15 \text{ mA}$		11	20	Ω
		$V_{CC} = 4.5 \text{ V}$	$V_I = 0$	$I_I = 64 \text{ mA}$		3	7	
				$I_I = 30 \text{ mA}$		3	7	
			$V_I = 2.4 \text{ V}$,	$I_I = 15 \text{ mA}$		6	15	

† All typical values are at $V_{CC} = 5 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL-voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC} = 4 \text{ V}$		$V_{CC} = 5 \text{ V}$ $\pm 0.5 \text{ V}$		UNIT
				MIN	MAX	MIN	MAX	
				0.35		0.25		
t_{pd}^\dagger	A or B	B or A						ns
t_{PZH}	ON	A or B	BIASV = GND	6	2	5.1		ns
t_{PZL}			BIASV = 3 V	6	2	5.6		
t_{PHZ}	ON	A or B	BIASV = GND	5.5	1	5		ns
t_{PLZ}			BIASV = 3 V	5.5	2	5.9		

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V_{OUTU}	See Figures 1 and 2, and Table 1	2	$V_{OH}-0.3$	3	V

[†] All typical values are at $V_{CC} = 5$ V (unless otherwise noted), $T_A = 25^\circ\text{C}$.

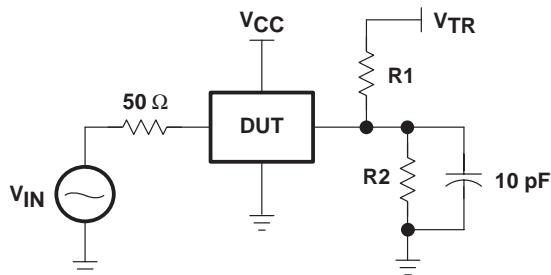


Figure 1. Device Test Setup

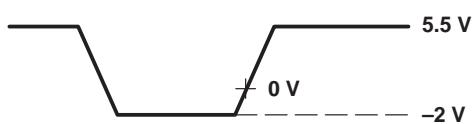


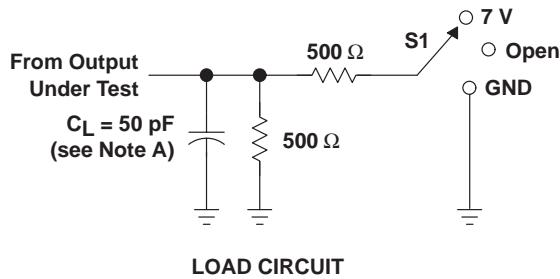
Figure 2. Transient Input Voltage Waveform

Table 1. Device Test Conditions

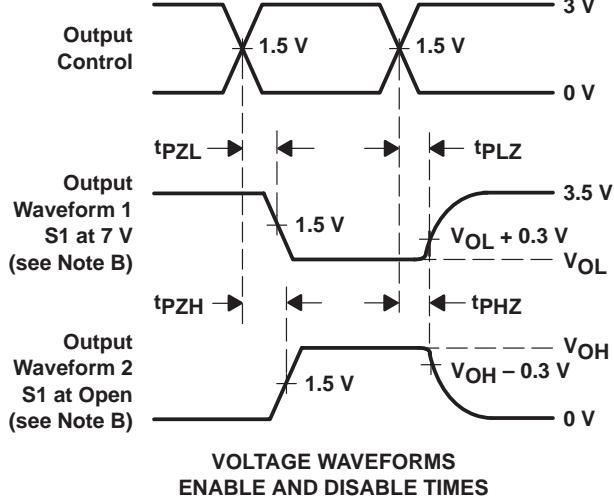
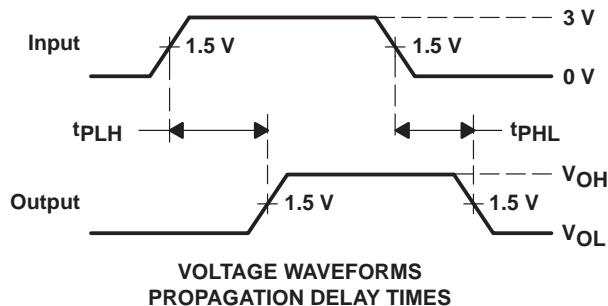
PARAMETER	VALUE	UNIT
B port under test [‡]	See Figure 1	
V_{IN}	See Figure 2	V
t_w	20	ns
t_r	2	ns
t_f	2	ns
$R1 = R2$	100	kΩ
V_{TR}	11	V
V_{CC}	5.5	V
BIASV	Open	

[‡] Other B-port outputs are open.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBTK6800DBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTK6800	Samples
SN74CBTK6800PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BK6800	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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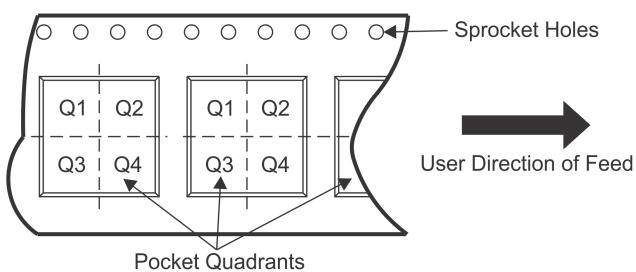
PACKAGE OPTION ADDENDUM

6-Feb-2020

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTK6800DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTK6800PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

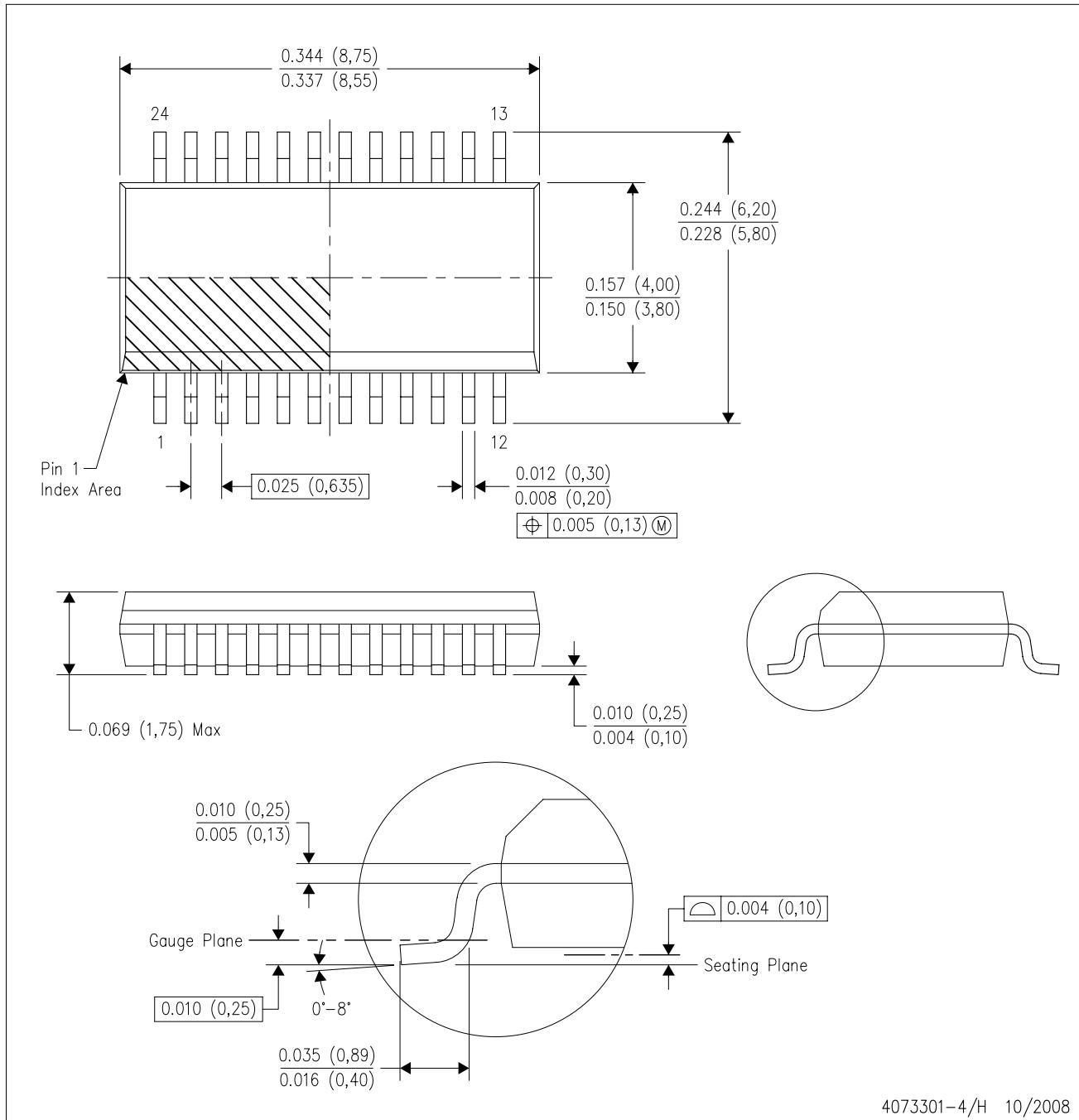
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTK6800DBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
SN74CBTK6800PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



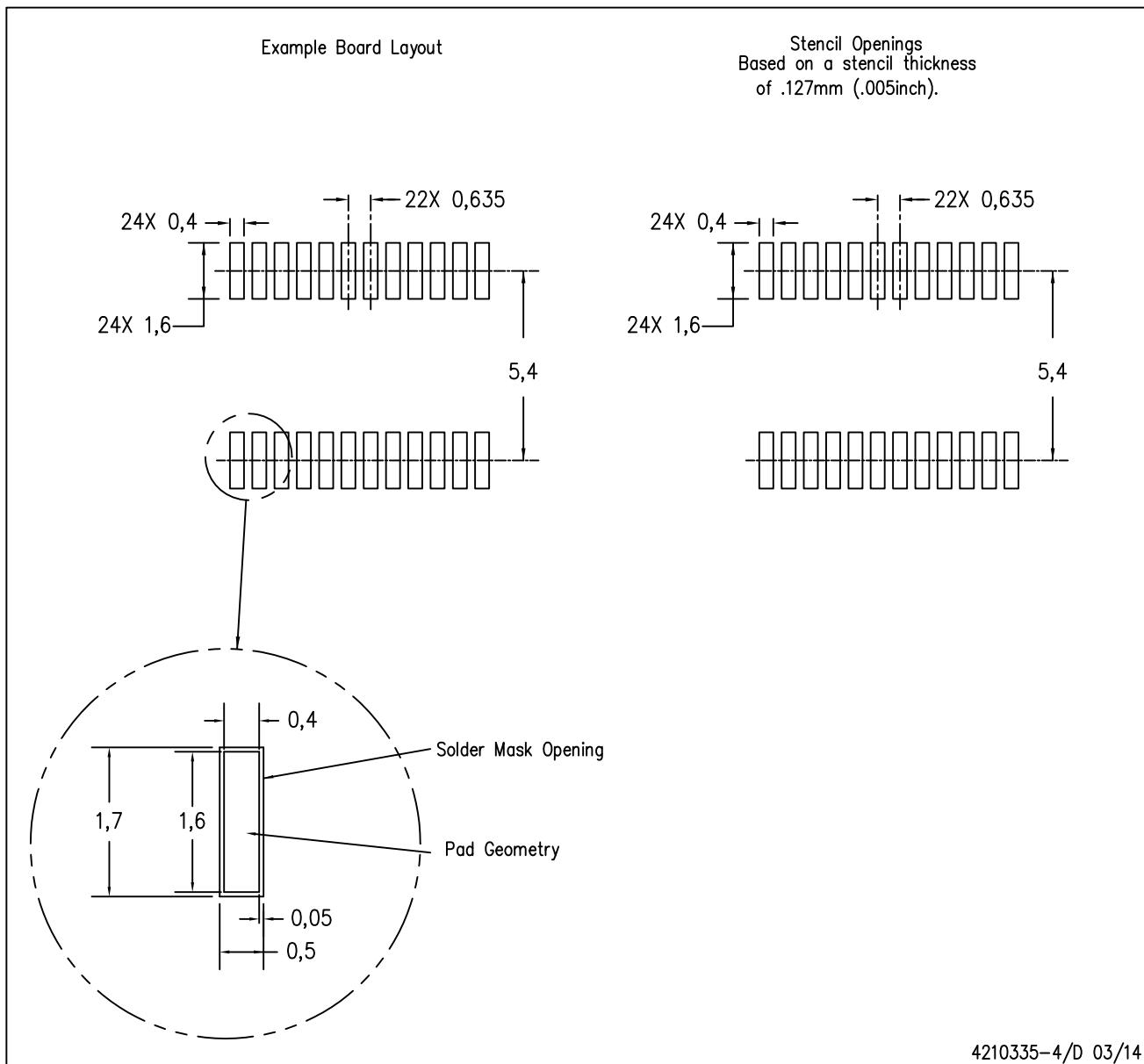
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- Falls within JEDEC MO-137 variation AE.

LAND PATTERN DATA

DBQ (R-PDSO-G24)

PLASTIC SMALL OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

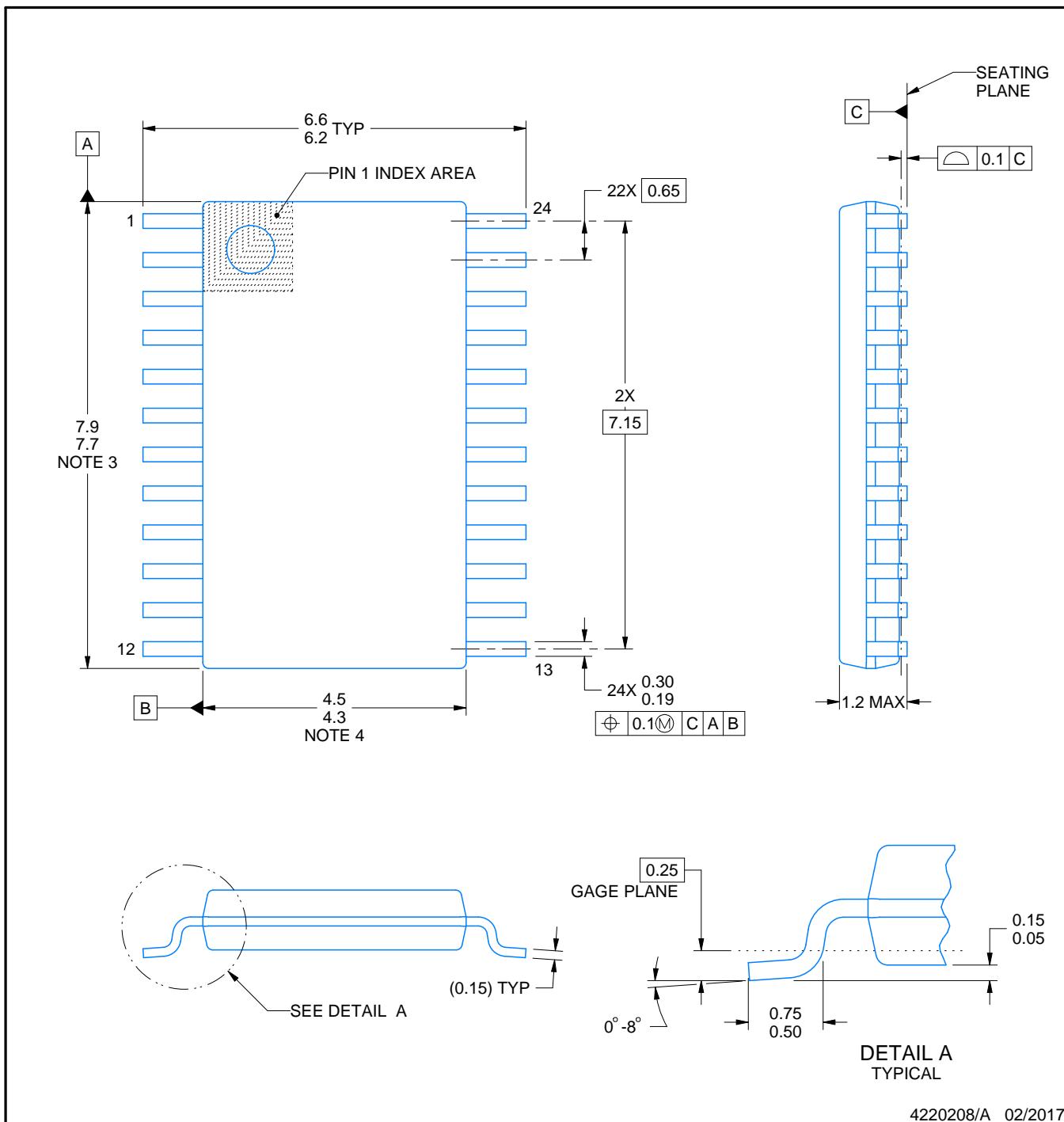
PACKAGE OUTLINE

PW0024A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

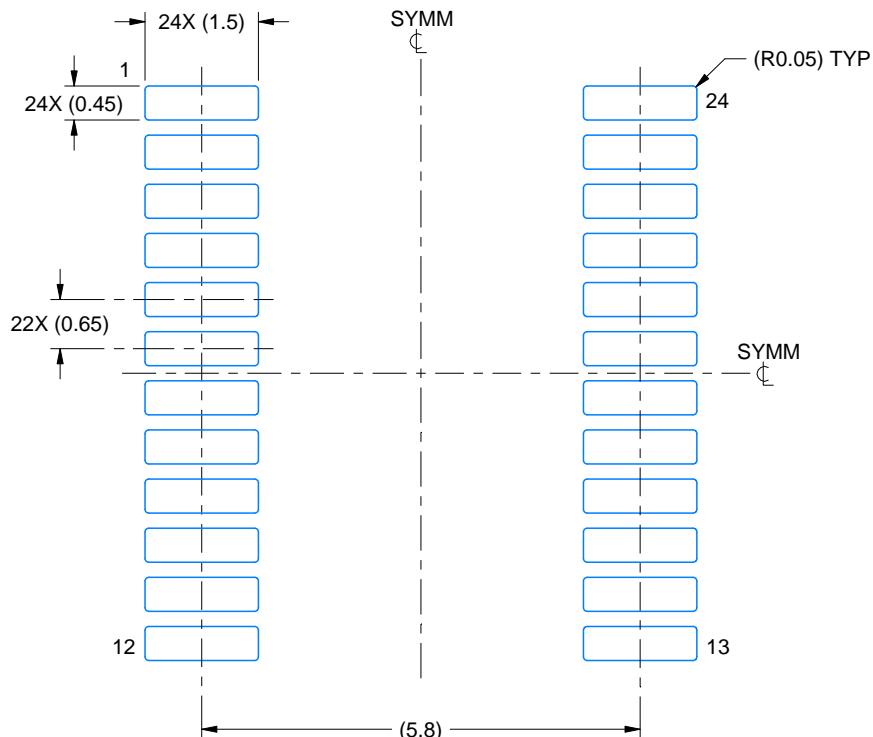
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

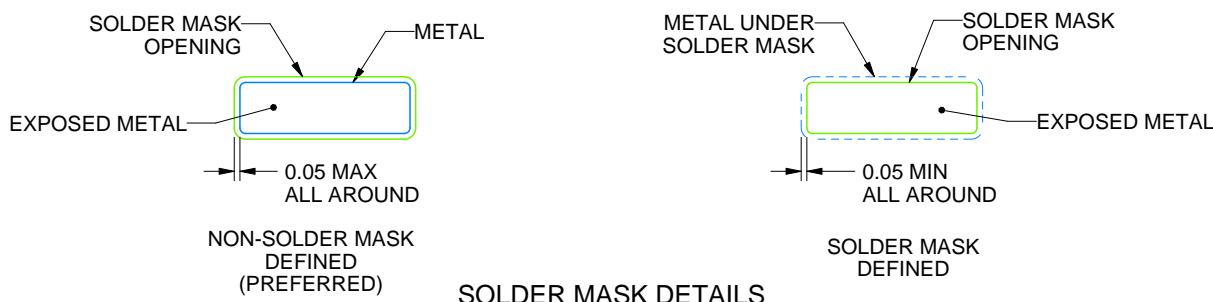
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

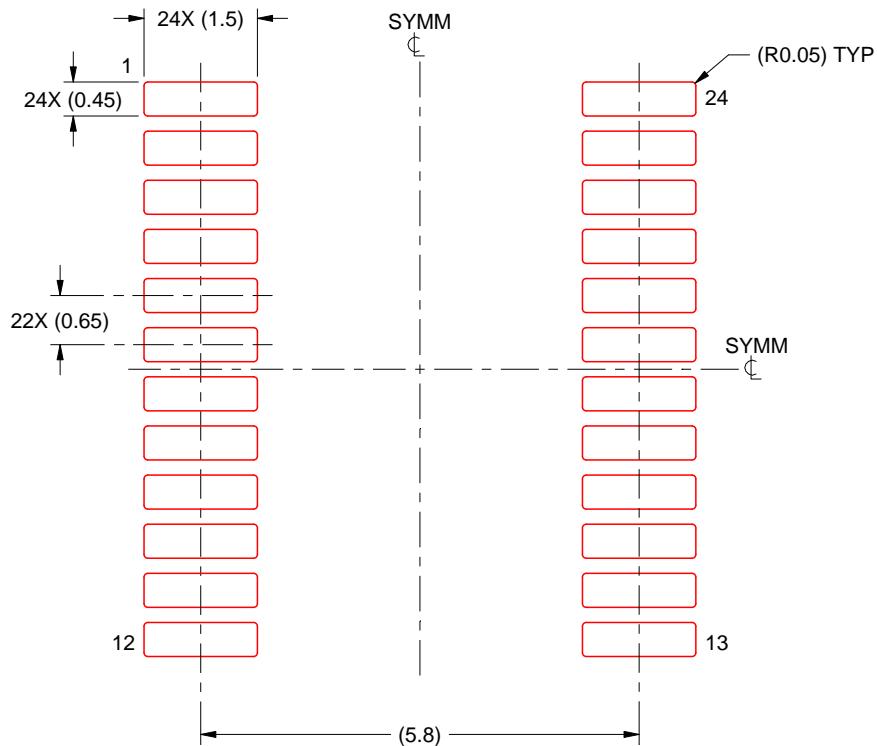
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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