



2Mb Ultra-Low Power Asynchronous CMOS SRAM

128K × 16 bit

Overview

The N02L63W2A is an integrated memory device containing a 2 Mbit Static Random Access Memory organized as 131,072 words by 16 bits. The device is designed and fabricated using ON Semiconductor's advanced CMOS technology to provide both high-speed performance and ultra-low power. The device operates with two chip enable ($\overline{CE1}$ and $\overline{CE2}$) controls and output enable (\overline{OE}) to allow for easy memory expansion. Byte controls (\overline{UB} and \overline{LB}) allow the upper and lower bytes to be accessed independently and can also be used to deselect the device. The N02L63W2A is optimal for various applications where low-power is critical such as battery backup and hand-held devices. The device can operate over a very wide temperature range of -40°C to $+85^{\circ}\text{C}$ and is available in JEDEC standard packages compatible with other standard 128Kb x 16 SRAMs.

Product Family

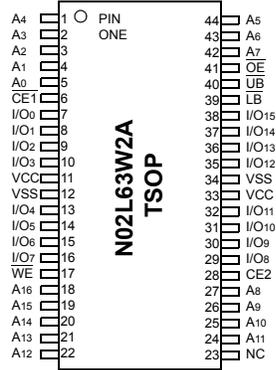
Part Number	Package Type	Operating Temperature	Power Supply (Vcc)	Speed	Standby Current (I_{SB}), Typical	Operating Current (I_{CC}), Typical
N02L63W2AB	48 - BGA	-40°C to $+85^{\circ}\text{C}$	2.3V - 3.6V	55ns @ 2.7V 70ns @ 2.3V	2 μA	2 mA @ 1MHz
N02L63W2AT	44 - TSOP II					
N02L63W2AB2	48 - BGA Green					
N02L63W2AT2	44 - TSOP II Green					

Features

- **Single Wide Power Supply Range**
2.3 to 3.6 Volts
- **Very low standby current**
2.0 μA at 3.0V (Typical)
- **Very low operating current**
2.0mA at 3.0V and 1 μs (Typical)
- **Very low Page Mode operating current**
0.8mA at 3.0V and 1 μs (Typical)
- **Simple memory control**
Dual Chip Enables ($\overline{CE1}$ and $\overline{CE2}$)
Byte control for independent byte operation
Output Enable (\overline{OE}) for memory expansion
- **Low voltage data retention**
 $V_{CC} = 1.8\text{V}$
- **Very fast output enable access time**
30ns \overline{OE} access time
- **Automatic power down to standby mode**
- **TTL compatible three-state output driver**
- **Compact space saving BGA package available**

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Pin Configuration



	1	2	3	4	5	6
A	$\overline{\text{LB}}$	$\overline{\text{OE}}$	A ₀	A ₁	A ₂	CE2
B	I/O ₈	$\overline{\text{UB}}$	A ₃	A ₄	$\overline{\text{CE1}}$	I/O ₀
C	I/O ₉	I/O ₁₀	A ₅	A ₆	I/O ₁	I/O ₂
D	V _{SS}	I/O ₁₁	NC	A ₇	I/O ₃	V _{CC}
E	V _{CC}	I/O ₁₂	NC	A ₁₆	I/O ₄	V _{SS}
F	I/O ₁₄	I/O ₁₃	A ₁₄	A ₁₅	I/O ₅	I/O ₆
G	I/O ₁₅	NC	A ₁₂	A ₁₃	$\overline{\text{WE}}$	I/O ₇
H	NC	A ₈	A ₉	A ₁₀	A ₁₁	NC

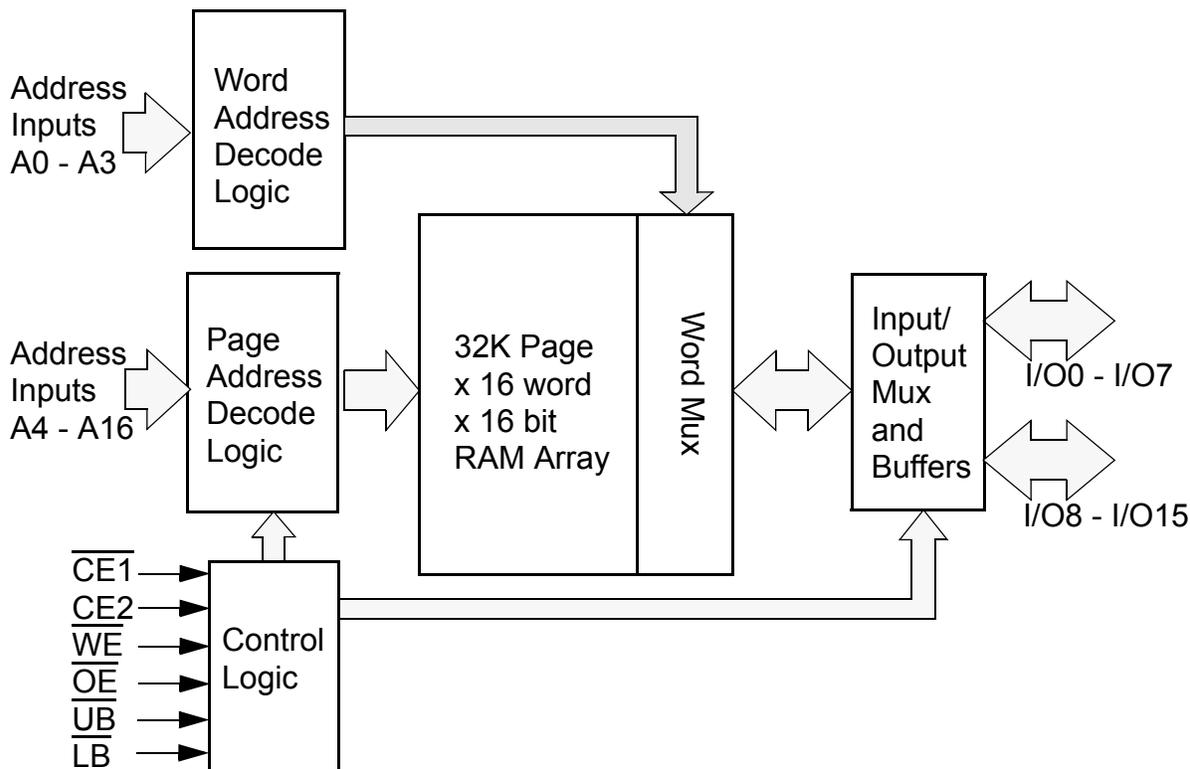
48 Pin BGA (top)
6 x 8 mm

Pin Descriptions

Pin Name	Pin Function
A ₀ -A ₁₆	Address Inputs
$\overline{\text{WE}}$	Write Enable Input
CE1, CE2	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{LB}}$	Lower Byte Enable Input
$\overline{\text{UB}}$	Upper Byte Enable Input
I/O ₀ -I/O ₁₅	Data Inputs/Outputs
V _{CC}	Power
V _{SS}	Ground
NC	Not Connected

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Functional Block Diagram



Functional Description

$\overline{\text{CE1}}$	$\overline{\text{CE2}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{UB}}$	$\overline{\text{LB}}$	$\text{I/O}_0 - \text{I/O}_{15}^1$	MODE	POWER
H	X	X	X	X	X	High Z	Standby ²	Standby
X	L	X	X	X	X	High Z	Standby ²	Standby
L	H	X	X	H	H	High Z	Standby	Standby
L	H	L	X ³	L ¹	L ¹	Data In	Write ³	Active
L	H	H	L	L ¹	L ¹	Data Out	Read	Active
L	H	H	H	L ¹	L ¹	High Z	Active	Active

1. When $\overline{\text{UB}}$ and $\overline{\text{LB}}$ are in select mode (low), $\text{I/O}_0 - \text{I/O}_{15}$ are affected as shown. When $\overline{\text{LB}}$ only is in the select mode only $\text{I/O}_0 - \text{I/O}_7$ are affected as shown. When $\overline{\text{UB}}$ is in the select mode only $\text{I/O}_8 - \text{I/O}_{15}$ are affected as shown.

2. When the device is in standby mode, control inputs ($\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{UB}}$, and $\overline{\text{LB}}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.

3. When $\overline{\text{WE}}$ is invoked, the $\overline{\text{OE}}$ input is internally disabled and has no effect on the circuit.

Capacitance¹

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{\text{IN}} = 0\text{V}$, $f = 1\text{ MHz}$, $T_{\text{A}} = 25^\circ\text{C}$		8	pF
I/O Capacitance	$C_{\text{I/O}}$	$V_{\text{IN}} = 0\text{V}$, $f = 1\text{ MHz}$, $T_{\text{A}} = 25^\circ\text{C}$		8	pF

1. These parameters are verified in device characterization and are not 100% tested

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Absolute Maximum Ratings¹

Item	Symbol	Rating	Unit
Voltage on any pin relative to V _{SS}	V _{IN,OUT}	-0.3 to V _{CC} +0.3	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-0.3 to 4.5	V
Power Dissipation	P _D	500	mW
Storage Temperature	T _{STG}	-40 to 125	°C
Operating Temperature	T _A	-40 to +85	°C
Soldering Temperature and Time	T _{SOLDER}	260°C, 10sec	°C

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Test Conditions	Min.	Typ ¹	Max	Unit
Supply Voltage	V _{CC}		2.3	3.0	3.6	V
Data Retention Voltage	V _{DR}	Chip Disabled ³	1.8		3.6	V
Input High Voltage	V _{IH}		1.8		V _{CC} +0.3	V
Input Low Voltage	V _{IL}		-0.3		0.6	V
Output High Voltage	V _{OH}	I _{OH} = 0.2mA	V _{CC} -0.2			V
Output Low Voltage	V _{OL}	I _{OL} = -0.2mA			0.2	V
Input Leakage Current	I _{LI}	V _{IN} = 0 to V _{CC}			0.5	μA
Output Leakage Current	I _{LO}	\overline{OE} = V _{IH} or Chip Disabled			0.5	μA
Read/Write Operating Supply Current @ 1 μs Cycle Time ²	I _{CC1}	V _{CC} =3.6 V, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0		2.0	4.0	mA
Read/Write Operating Supply Current @ 70 ns Cycle Time ²	I _{CC2}	V _{CC} =3.6 V, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0		12.0	16.0	mA
Page Mode Operating Supply Current @ 70ns Cycle Time ² (Refer to Power Savings with Page Mode Operation diagram)	I _{CC3}	V _{CC} =3.6 V, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0		4.0		mA
Read/Write Quiescent Operating Supply Current ³	I _{CC4}	V _{CC} =3.6 V, V _{IN} =V _{IH} or V _{IL} Chip Enabled, I _{OUT} = 0, f = 0			3.0	mA
Maximum Standby Current ³	I _{SB1}	V _{IN} = V _{CC} or 0V Chip Disabled t _A = 85°C, V _{CC} = 3.6 V		2.0	20.0	μA
Maximum Data Retention Current ³	I _{DR}	V _{CC} = 1.8V, V _{IN} = V _{CC} or 0 Chip Disabled, t _A = 85°C			10.0	μA

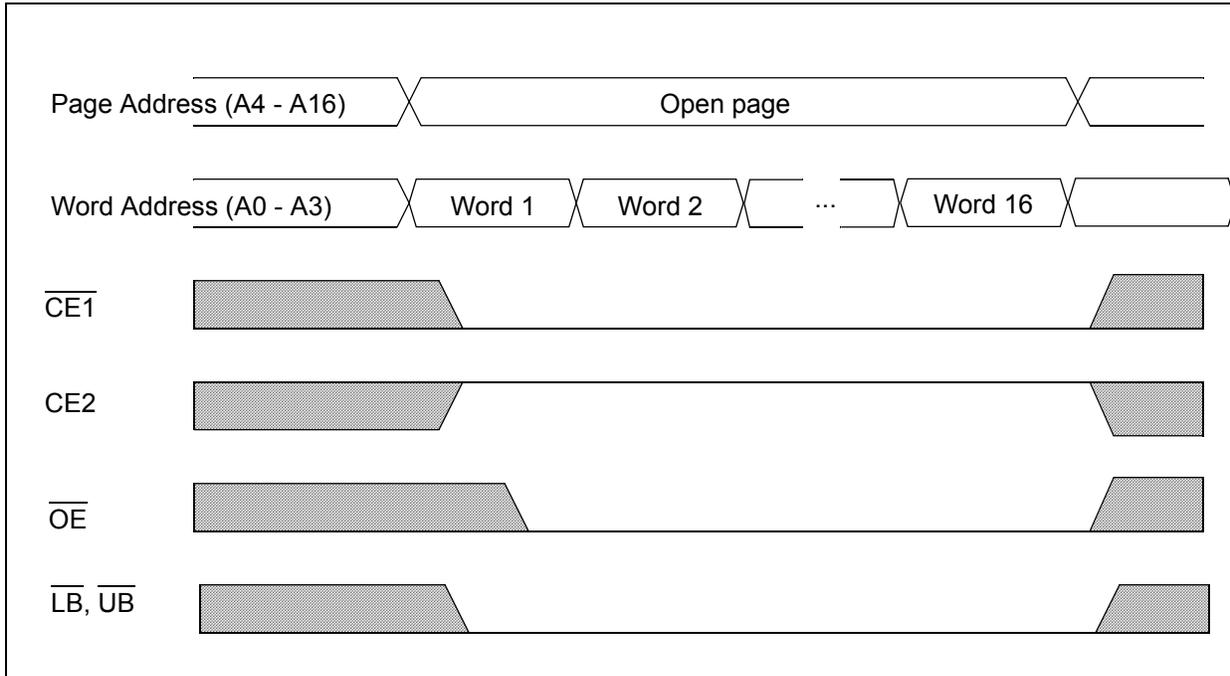
1. Typical values are measured at V_{CC}=V_{CC} Typ., T_A=25°C and not 100% tested.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

3. This device assumes a standby mode if the chip is disabled ($\overline{CE1}$ high or CE2 low). In order to achieve low standby current all inputs must be within 0.2 volts of either V_{CC} or V_{SS}.

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Power Savings with Page Mode Operation ($\overline{WE} = V_{IH}$)



Note: Page mode operation is a method of addressing the SRAM to save operating current. The internal organization of the SRAM is optimized to allow this unique operating mode to be used as a valuable power saving feature.

The only thing that needs to be done is to address the SRAM in a manner that the internal page is left open and 16-bit words of data are read from the open page. By treating addresses A0-A3 as the least significant bits and addressing the 16 words within the open page, power is reduced to the page mode value which is considerably lower than standard operating currents for low power SRAMs.

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Timing Test Conditions

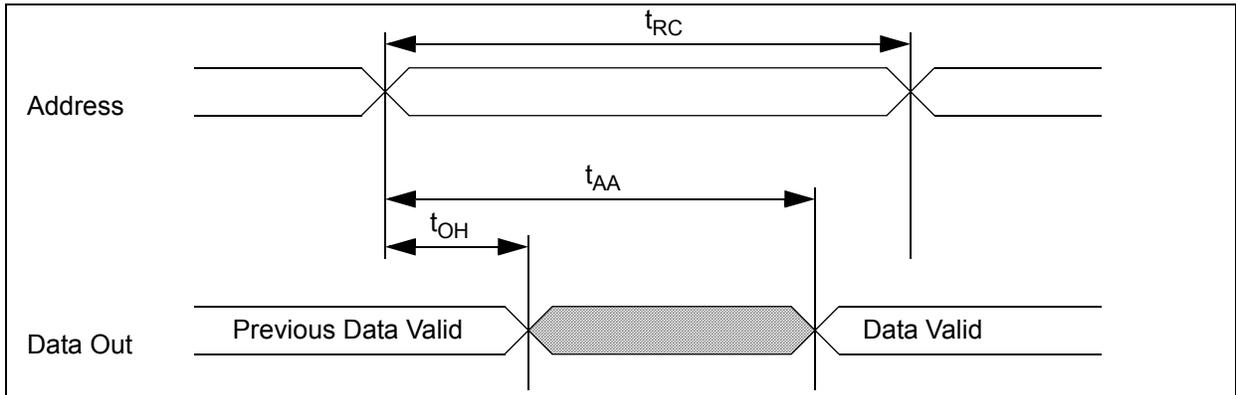
Item	
Input Pulse Level	0.1V _{CC} to 0.9 V _{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V _{CC}
Output Load	CL = 30pF
Operating Temperature	-40 to +85 °C

Timing

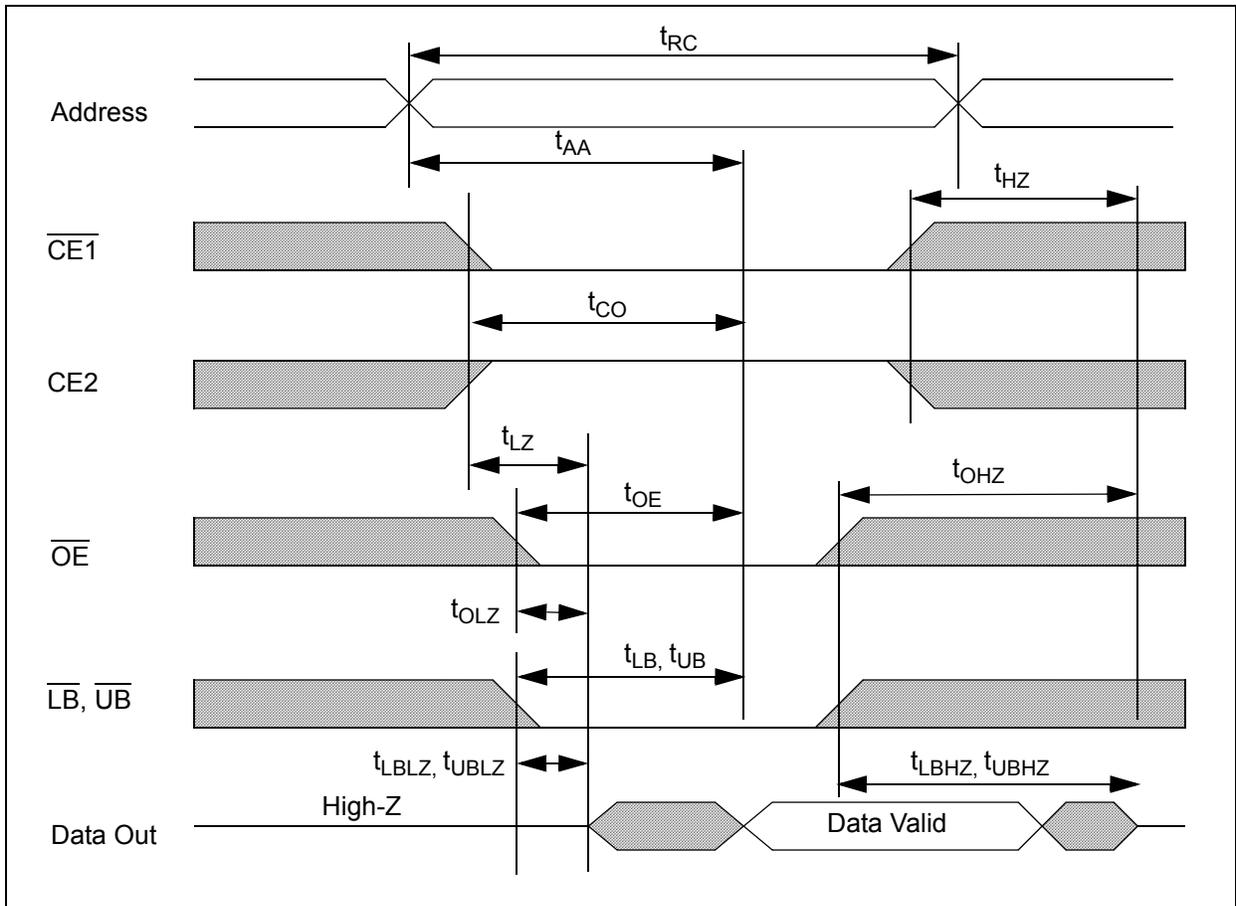
Item	Symbol	2.3 - 3.6 V		2.7 - 3.6 V		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t _{RC}	70		55		ns
Address Access Time	t _{AA}		70		55	ns
Chip Enable to Valid Output	t _{CO}		70		55	ns
Output Enable to Valid Output	t _{OE}		35		30	ns
Byte Select to Valid Output	t _{LB} , t _{UB}		70		55	ns
Chip Enable to Low-Z output	t _{LZ}	10		10		ns
Output Enable to Low-Z Output	t _{OLZ}	5		5		ns
Byte Select to Low-Z Output	t _{LBZ} , t _{UBZ}	10		10		ns
Chip Disable to High-Z Output	t _{HZ}	0	20	0	20	ns
Output Disable to High-Z Output	t _{OHZ}	0	20	0	20	ns
Byte Select Disable to High-Z Output	t _{LBHZ} , t _{UBHZ}	0	20	0	20	ns
Output Hold from Address Change	t _{OH}	10		10		ns
Write Cycle Time	t _{WC}	70		55		ns
Chip Enable to End of Write	t _{CW}	50		40		ns
Address Valid to End of Write	t _{AW}	50		40		ns
Byte Select to End of Write	t _{LBW} , t _{UBW}	50		40		ns
Write Pulse Width	t _{WP}	40		40		ns
Address Setup Time	t _{AS}	0		0		ns
Write Recovery Time	t _{WR}	0		0		ns
Write to High-Z Output	t _{WHZ}		20		20	ns
Data to Write Time Overlap	t _{DW}	40		35		ns
Data Hold from Write Time	t _{DH}	0		0		ns
End Write to Low-Z Output	t _{OW}	10		10		ns

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Timing of Read Cycle ($\overline{CE1} = \overline{OE} = V_{IL}, \overline{WE} = CE2 = V_{IH}$)

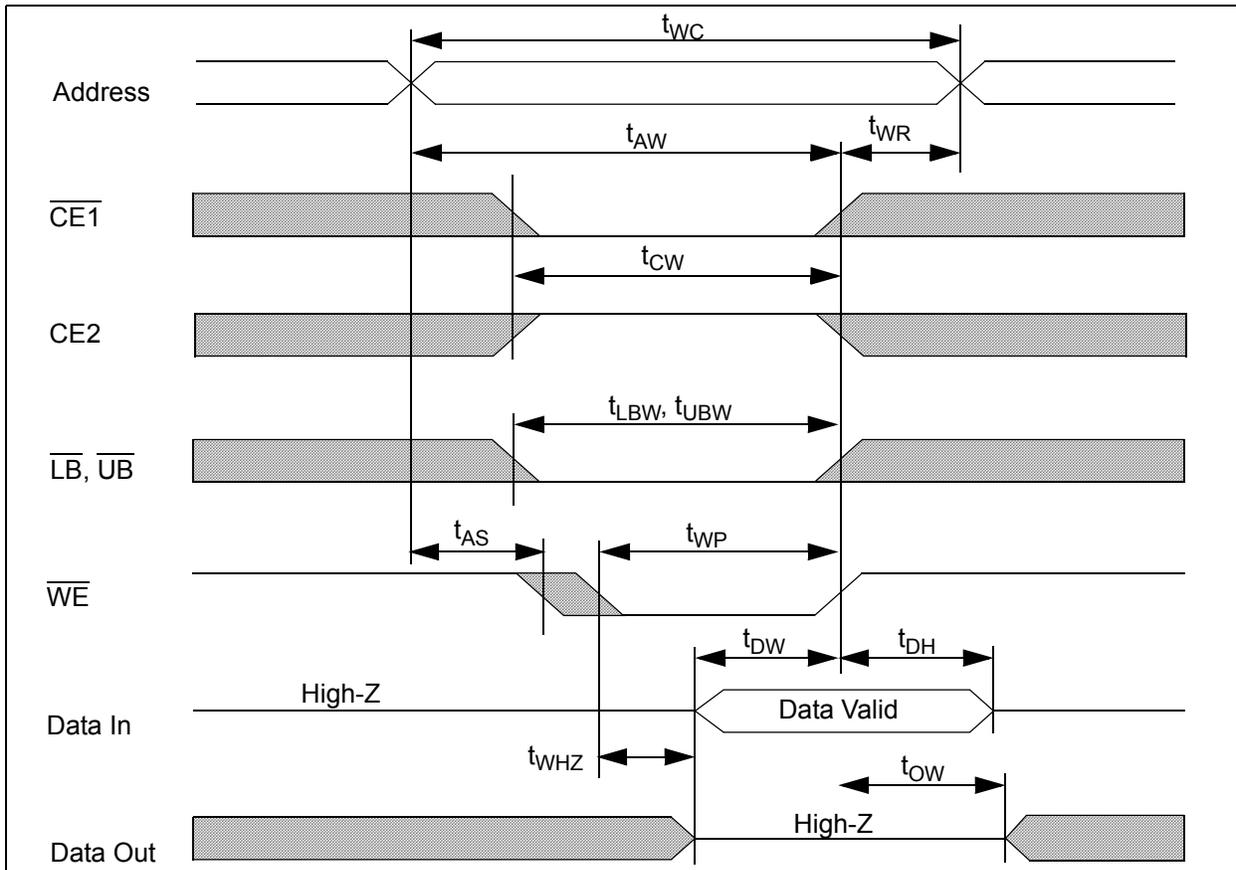


Timing Waveform of Read Cycle ($\overline{WE} = V_{IH}$)

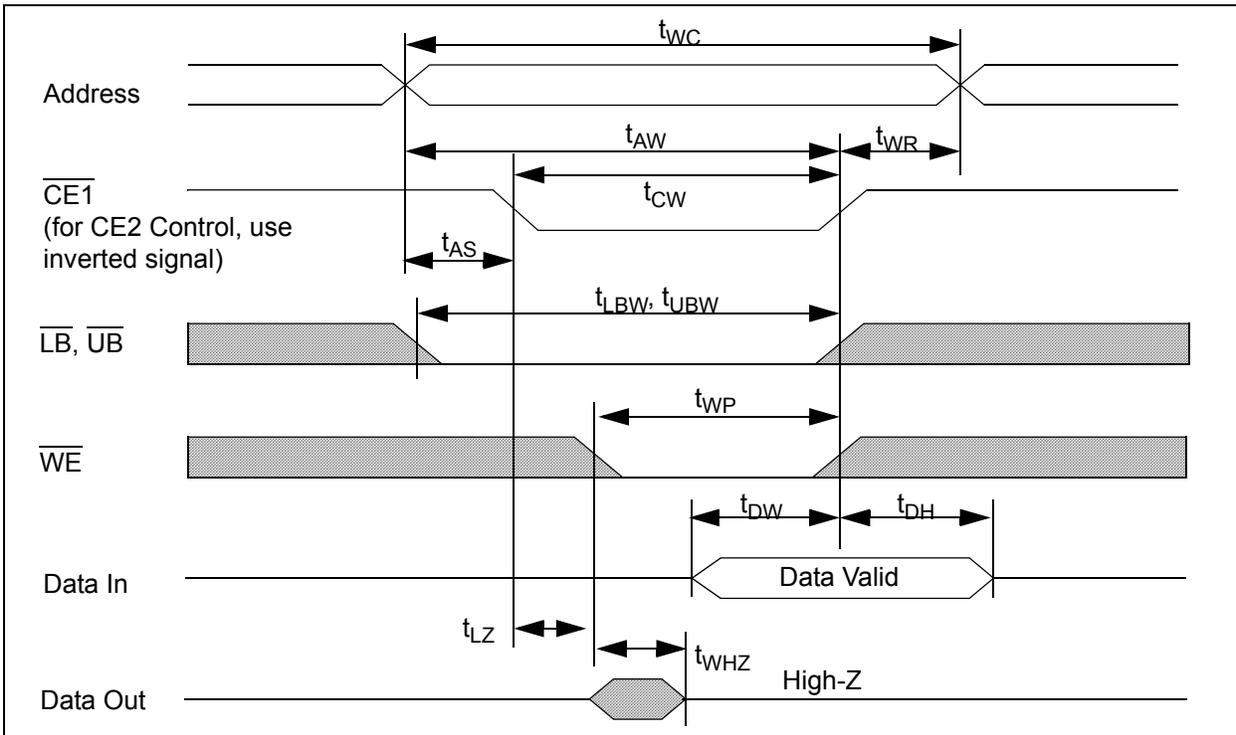


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Timing Waveform of Write Cycle (\overline{WE} control)

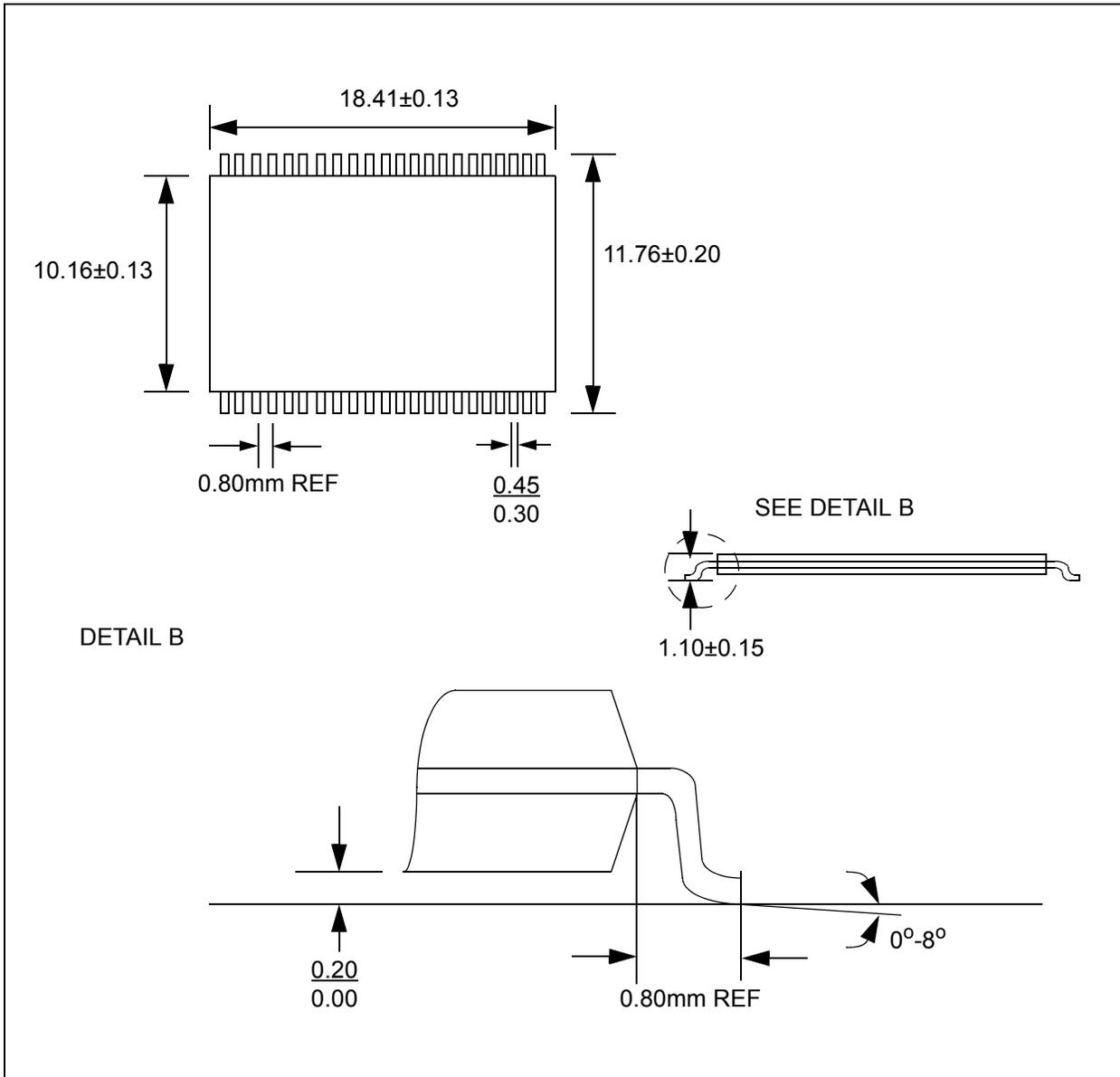


Timing Waveform of Write Cycle (CE1 Control)



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44-Lead TSOP II Package (T44)

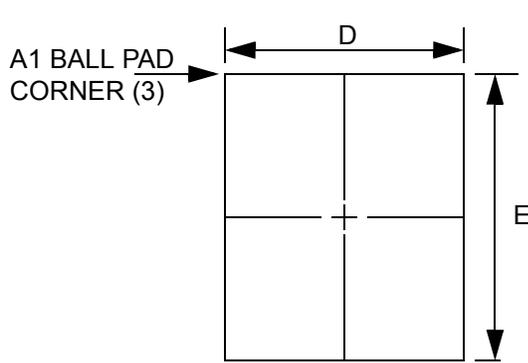


Note:

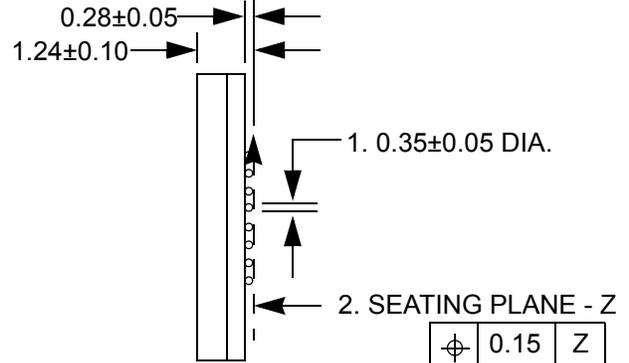
1. All dimensions in inches (Millimeters)
2. Package dimensions exclude molding flash

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Ball Grid Array Package

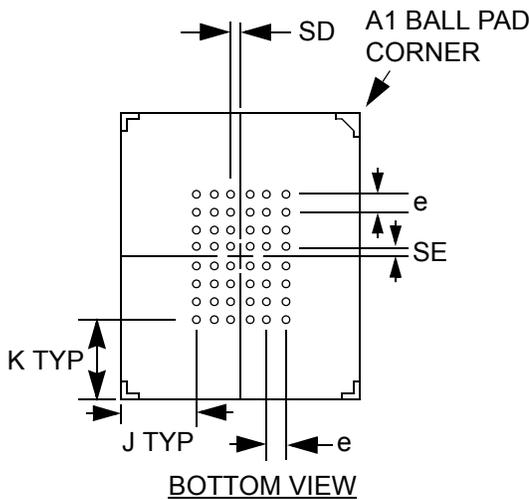


TOP VIEW



SIDE VIEW

ϕ	0.15	Z
ϕ	0.05	Z



BOTTOM VIEW

1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

Dimensions (mm)

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL

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Ordering Information

Part Number	Package	Shipping Method
N02L63W2AT5I	Leaded 44-TSOP II	Tray
N02L63W2AT25I	Green 44-TSOP II (RoHS Compliant)	Tray
N02L63W2AB5I	Leaded 48-BGA	Tray
N02L63W2AB25I	Green 48-BGA (RoHS Compliant)	Tray
N02L63W2AT5IT	Leaded 44-TSOP II	Tape & Reel
N02L63W2AT25IT	Green 44-TSOP II (RoHS Compliant)	Tape & Reel
N02L63W2AB5IT	Leaded 48-BGA	Tape & Reel
N02L63W2AB25IT	Green 48-BGA (RoHS Compliant)	Tape & Reel

Revision History

Revision	Date	Change Description
A	Jan. 2001	Initial Preliminary Release
B	May 2001	Changed access time to 55 ns
C	Sept. 2001	Minor parametric modifications. Full production release.
D	Dec. 2001	Part number change from EM128J16, modified Overview and Features, added Page Mode Operation diagram, revised Operating Characteristics table, Package diagram, Functional Description table and Ordering Information diagram
E	Nov. 2002	Replaced Isb and Icc on Product Family table with typical values
F	Oct. 2004	Added Pb-Free and Green Package Option
G	Nov. 2005	Removed Pb-Free Pkg., added Green Pkg, RoHS compliant
H	September 2006	Converted to AMI Semiconductor
9	July 2008	Converted to ON Semiconductor and new part numbers

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