

NHD-320240WG-BxTFH-VZ#

Graphic Liquid Crystal Display Module

NHD-	Newhaven Display
320240-	320 x 240 Pixels
WG-	Display Type: Graphic
Bx-	Model
T-	White LED Backlight
F-	FSTN (+)
H-	Transflective, 6:00 Optimal View, Wide Temperature
VZ-	Built-in Negative Voltage
#-	RoHS Compliant

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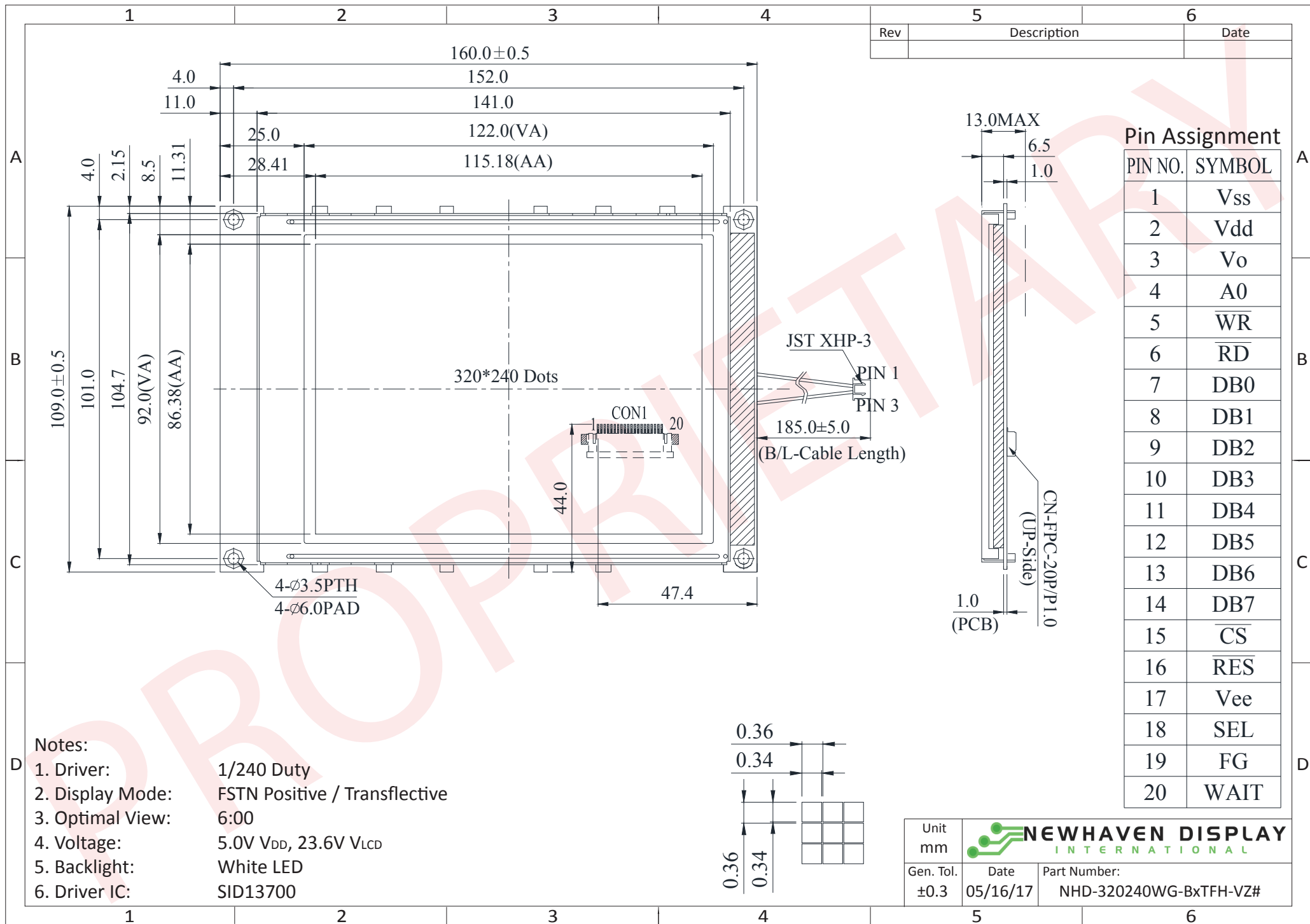
Document Revision History

Revision	Date	Description	Changed by
0	6/7/07	Initial Release	-
1	4/20/10	User guide reformat	MC
2	9/22/11	Electrical characteristics updated	AK
3	10/7/13	Mechanical Drawing, Pin Description, Wiring Diagram, and Timing Characteristics updated	ML
4	6/1/16	Electrical characteristics, Pin description, Quality Info updated	TM
5	8/3/16	Electrical and Optical characteristics updated	TM
6	5/16/17	Mechanical & Electrical Characteristics Updated	SB

Functions and Features

- 320 x 240 pixels
- +5.0V or +3.3V power supply
- Built-in S1D13700 Controller
- Default 8080 mode
- 8-bit Parallel interface

Mechanical Drawing

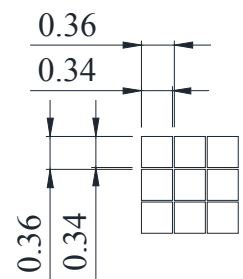


Rev	Description	Date

Pin Assignment

PIN NO.	SYMBOL
1	V _{SS}
2	V _{DD}
3	V _O
4	A0
5	\overline{WR}
6	\overline{RD}
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	\overline{CS}
16	\overline{RES}
17	V _{EE}
18	SEL
19	FG
20	WAIT

- Notes:
1. Driver: 1/240 Duty
 2. Display Mode: FSTN Positive / Transflective
 3. Optimal View: 6:00
 4. Voltage: 5.0V V_{DD}, 23.6V V_{LCD}
 5. Backlight: White LED
 6. Driver IC: SID13700



Unit mm	NEWHAVEN DISPLAY INTERNATIONAL	
Gen. Tol. ±0.3	Date 05/16/17	Part Number: NHD-320240WG-BxTFH-VZ#

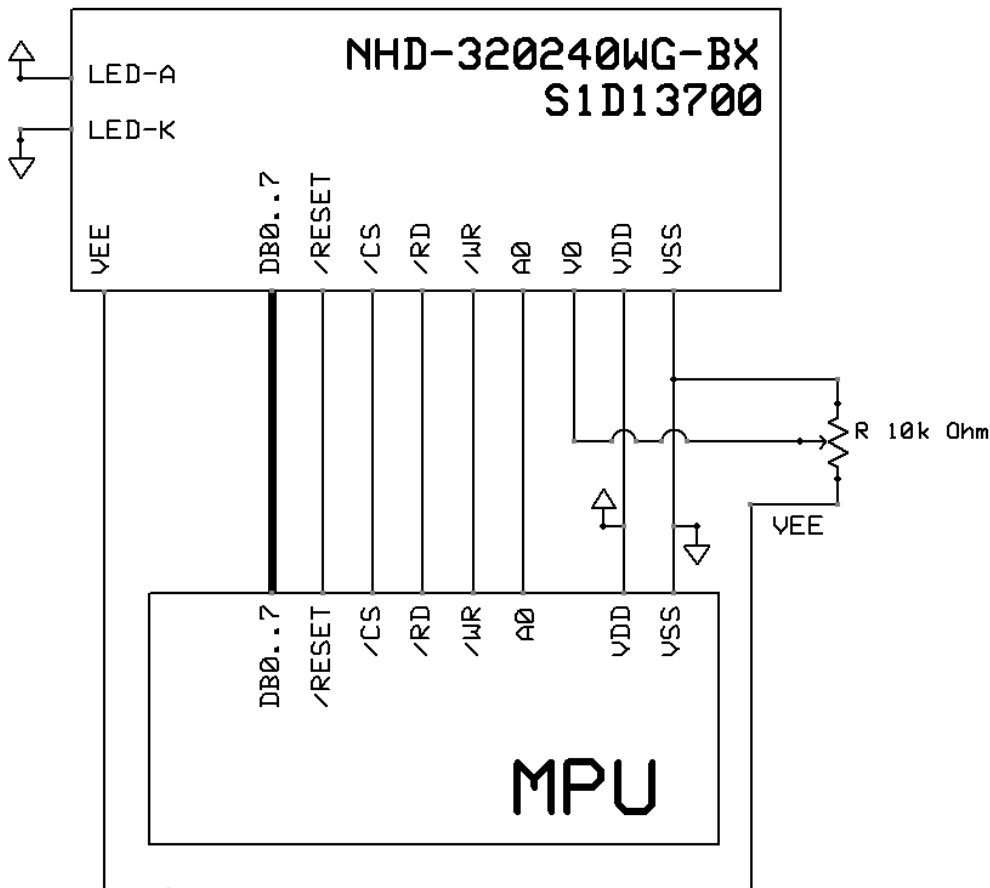
Pin Description and Wiring Diagram

Pin No.	Symbol	External Connection	Function Description
1	V _{SS}	Power Supply	Ground
2	V _{DD}	Power Supply	Supply Voltage (+5.0V)
3	V ₀	Adj. Power Supply	Supply Voltage for Contrast (approx. -18.8V)
4	A0	MPU	Register Select signal. A0=1: Command, A0=0: Data
5	/WR R/W	MPU	8080: Active LOW Write signal 6800: Read/Write select signal, R/W=1: Read R/W=0: Write
6	/RD E	MPU	8080: Active LOW Read signal 6800: Operation Enable signal. Falling edge triggered.
7-14	DB0-DB7	MPU	8-bit bi-directional data bus
15	/CS	MPU	Active LOW Chip Select signal
16	/RESET	MPU	Active LOW Reset signal
17	V _{EE}	Power Supply	Negative voltage output (-25V)
18	NC	-	No Connect
19	NC	-	No Connect
20	NC	-	No Connect
A	LED+	Power Supply	Backlight Anode (130mA @ 3.5V)
K	LED-	Power Supply	Backlight Cathode (Ground)

Recommended LCD connector: 1.0mm pitch, 20-pos FFC connector

Backlight connector: JST p/n: XHP-3

Mates with: JST p/n: B 3B-XH-A



Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	T_{OP}	Absolute Max	-20	-	+70	°C
Storage Temperature Range	T_{ST}	Absolute Max	-30	-	+80	°C
Supply Voltage	V_{DD}	-	3.3	5.0	5.5	V
Supply Current	I_{DD}	$V_{DD}=5.0V$	35	65	110	mA
Supply for LCD (contrast)	V_{LCD}	$T_{OP}=25^{\circ}C$	23.0	23.6	24.2	V
“H” Level input	V_{IH}	$V_{DD}=5.0V$	3.5	-	V_{DD}	V
		$V_{DD}=3.3V$	2.0	-	V_{DD}	V
“L” Level input	V_{IL}	$V_{DD}=5.0V$	V_{SS}	-	1.0	V
		$V_{DD}=3.3V$	V_{SS}	-	0.8	V
“H” Level output	V_{OH}	$V_{DD}=5.0V$	$V_{DD}-0.4$	-	V_{DD}	V
		$V_{DD}=3.3V$	$V_{DD}-0.4$	-	V_{DD}	V
“L” Level output	V_{OL}	$V_{DD}=5.0V$	V_{SS}	-	0.4	V
		$V_{DD}=3.3V$	V_{SS}	-	0.4	V
Backlight Supply Current	I_{LED}	-	-	130	160	mA
Backlight Supply Voltage	V_{LED}	$I_{LED}=130mA$	3.3	3.5	3.7	V

*The LED of the backlight is driven by current drain; drive voltage is for reference only. Drive voltage must be selected to ensure backlight current drain is below MAX level stated.

Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Optimal Viewing Angles	Top	$\phi Y+$	-	30	-	°
	Bottom	$\phi Y-$	-	60	-	°
	Left	$\theta X-$	-	45	-	°
	Right	$\theta X+$	-	45	-	°
Contrast Ratio	Cr	-	-	5	-	-
Response Time	Rise	T_r	-	200	300	ms
	Fall	T_f	-	250	350	ms

Jumper Selection



Note: This display is pre-configured for 5V and 8080 mode.

Controller Information

Built-in S1D13700 controller.

Please download specification at http://www.newhavendisplay.com/app_notes/S1D13700.pdf

Table of Commands

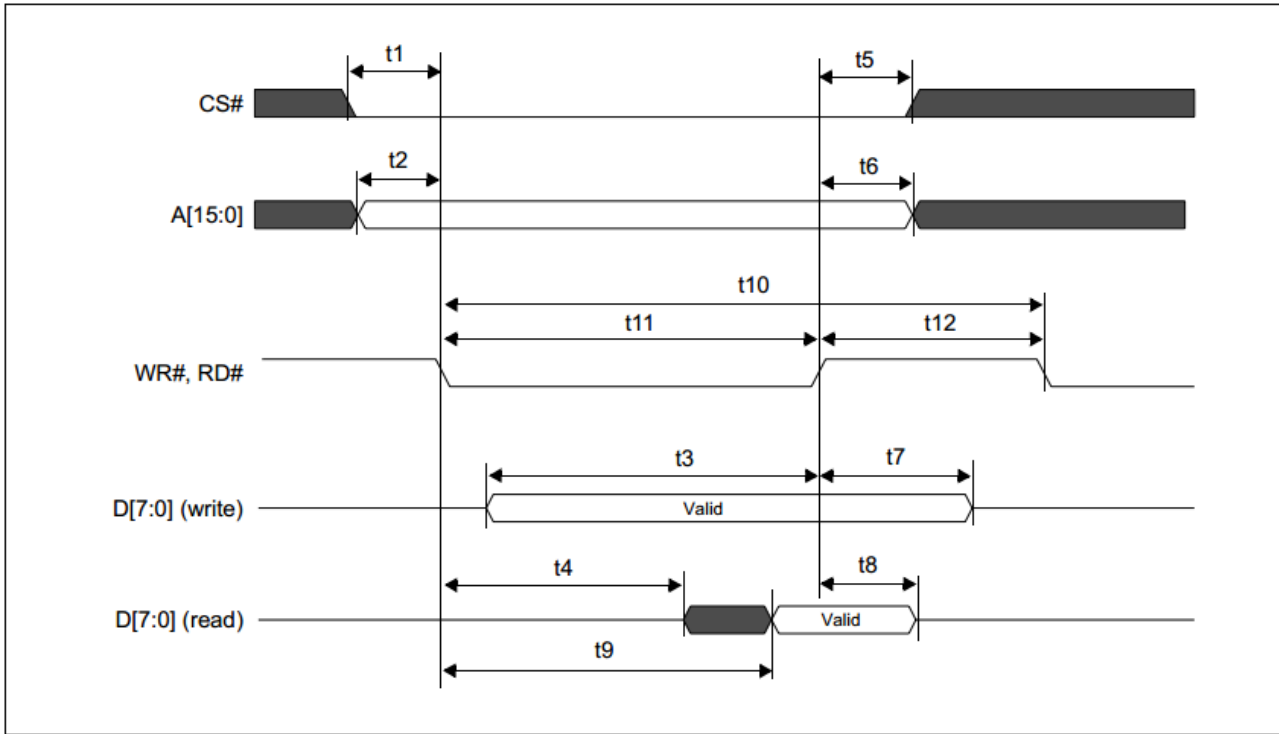
REG[01h] Horizontal Character Size Register							
Address = 8001h Default = 00h							Read/Write
MOD	n/a			Horizontal Character Size bits 3-0			
7	6	5	4	3	2	1	0
REG[02h] Vertical Character Size Register							
Address = 8002h Default = 00h							Read/Write
n/a			Vertical Character Size bits 3-0				
7	6	5	4	3	2	1	0
REG[03h] Character Bytes Per Row Register							
Address = 8003h Default = 00h							Read/Write
Character Bytes Per Row bits 7-0							
7	6	5	4	3	2	1	0
REG[04h] Total Character Bytes Per Row Register							
Address = 8004h Default = 00h							Read/Write
Total Character Bytes Per Row bits 7-0							
7	6	5	4	3	2	1	0
REG[05h] Frame Height Register							
Address = 8005h Default = 00h							Read/Write
Frame Height bits 7-0							
7	6	5	4	3	2	1	0
REG[06h] Horizontal Address Range Register 0							
Address = 8006h Default = 00h							Read/Write
Horizontal Address Range bits 7-0							
7	6	5	4	3	2	1	0
REG[07h] Horizontal Address Range Register 1							
Address = 8007h Default = 00h							Read/Write
Horizontal Address Range bits 15-8							
7	6	5	4	3	2	1	0
REG[08h] Power Save Mode Register							
Address = 8008h Default = 01h							Read/Write
n/a						Power Save Mode Enable	
7	6	5	4	3	2	1	0
REG[09h] Display Enable Register							
Address = 8009h Default = 00h							Read/Write
n/a						Display Enable	
7	6	5	4	3	2	1	0
REG[0Ah] Display Attribute Register							
Address = 800Ah Default = 00h							Read/Write
SAD3 Attribute bits 1-0		SAD2 Attribute bits 1-0		SAD1 Attribute bits 1-0		Cursor Attribute bits 1-0	
7	6	5	4	3	2	1	0
REG[0Bh] Screen Block 1 Start Address Register 0							
Address = 800Bh Default = 00h							Read/Write
Screen Block 1 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0
REG[0Ch] Screen Block 1 Start Address Register 1							
Address = 800Ch Default = 00h							Read/Write
Screen Block 1 Start Address bits 15-8 (MSB)							
7	6	5	4	3	2	1	0
REG[0Dh] Screen Block 1 Size Register							
Address = 800Dh Default = 00h							Read/Write
Screen Block 1 Size bits 7-0							
7	6	5	4	3	2	1	0

REG[0Eh] Screen Block 2 Start Address Register 0								Read/Write
Address = 800Eh Default = 00h								
Screen Block 2 Start Address bits 7-0 (LSB)								
7	6	5	4	3	2	1	0	
REG[0Fh] Screen Block 2 Start Address Register 1								Read/Write
Address = 800Fh Default = 00h								
Screen Block 2 Start Address bits 15-8 (MSB)								
7	6	5	4	3	2	1	0	
REG[10h] Screen Block 2 Size Register								Read/Write
Address = 8010h Default = 00h								
Screen Block 2 Size bits 7-0								
7	6	5	4	3	2	1	0	
REG[11h] Screen Block 3 Start Address Register 0								Read/Write
Address = 8011h Default = 00h								
Screen Block 3 Start Address bits 7-0 (LSB)								
7	6	5	4	3	2	1	0	
REG[12h] Screen Block 3 Start Address Register 1								Read/Write
Address = 8012h Default = 00h								
Screen Block 3 Start Address bits 15-8 (MSB)								
7	6	5	4	3	2	1	0	
REG[13h] Screen Block 4 Start Address Register 0								Read/Write
Address = 8013h Default = 00h								
Screen Block 4 Start Address bits 7-0 (LSB)								
7	6	5	4	3	2	1	0	
REG[14h] Screen Block 4 Start Address Register 1								Read/Write
Address = 8014h Default = 00h								
Screen Block 4 Start Address bits 15-8 (MSB)								
7	6	5	4	3	2	1	0	
REG[15h] Cursor Width Register								Read/Write
Address = 8015h Default = 00h								
n/a				Cursor Width bits 3-0				
7	6	5	4	3	2	1	0	
REG[16h] Cursor Height Register								Read/Write
Address = 8016h Default = 00h								
Cursor Mode	n/a				Cursor Height bits 3-0			
7	6	5	4	3	2	1	0	
REG[17h] Cursor Shift Direction Register								Read/Write
Address = 8017h Default = 00h								
n/a					Cursor Shift Direction bits 1-0			
7	6	5	4	3	2	1	0	
REG[18h] Overlay Register								Read/Write
Address = 8018h Default = 00h								
n/a			3 Layer Overlay Select	Screen Block 3 Display Mode	Screen Block 1 Display Mode	Layer Composition Method bits 1-0		
7	6	5	4	3	2	1	0	
REG[19h] Character Generator RAM Start Address Register 0								Read/Write
Address = 8019h Default = 00h								
CGRAM Start Address bits 7-0 (LSB)								
7	6	5	4	3	2	1	0	
REG[1Ah] Character Generator RAM Start Address Register 1								Read/Write
Address = 801Ah Default = 00h								
CGRAM Start Address bits 15-8 (MSB)								
7	6	5	4	3	2	1	0	
REG[1Bh] Horizontal Pixel Scroll Register								Read/Write
Address = 801Bh Default = 00h								
n/a				Horizontal Pixel Scroll bits 2-0				
7	6	5	4	3	2	1	0	

REG[1Ch] Cursor Write Register 0								Write Only
Address = 801Ch Default = 00h								
Cursor Write bits 7-0 (LSB)								
7	6	5	4	3	2	1	0	
REG[1Dh] Cursor Write Register 1								Write Only
Address = 801Dh Default = 00h								
Cursor Write bits 15-8 (MSB)								
7	6	5	4	3	2	1	0	
REG[1Eh] Cursor Read Register 0								Read Only
Address = 801Eh Default = 00h								
Cursor Read bits 7-0 (LSB)								
7	6	5	4	3	2	1	0	
REG[1Fh] Cursor Read Register 1								Read Only
Address = 801Fh Default = 00h								
Cursor Read bits 15-8 (MSB)								
7	6	5	4	3	2	1	0	
REG[20h] Bit-Per-Pixel Select Register								Read/Write
Address = 8020h Default = 00h								
n/a					Bit-Per-Pixel Select bits 1-0			
7	6	5	4	3	2	1	0	

Timing Characteristics

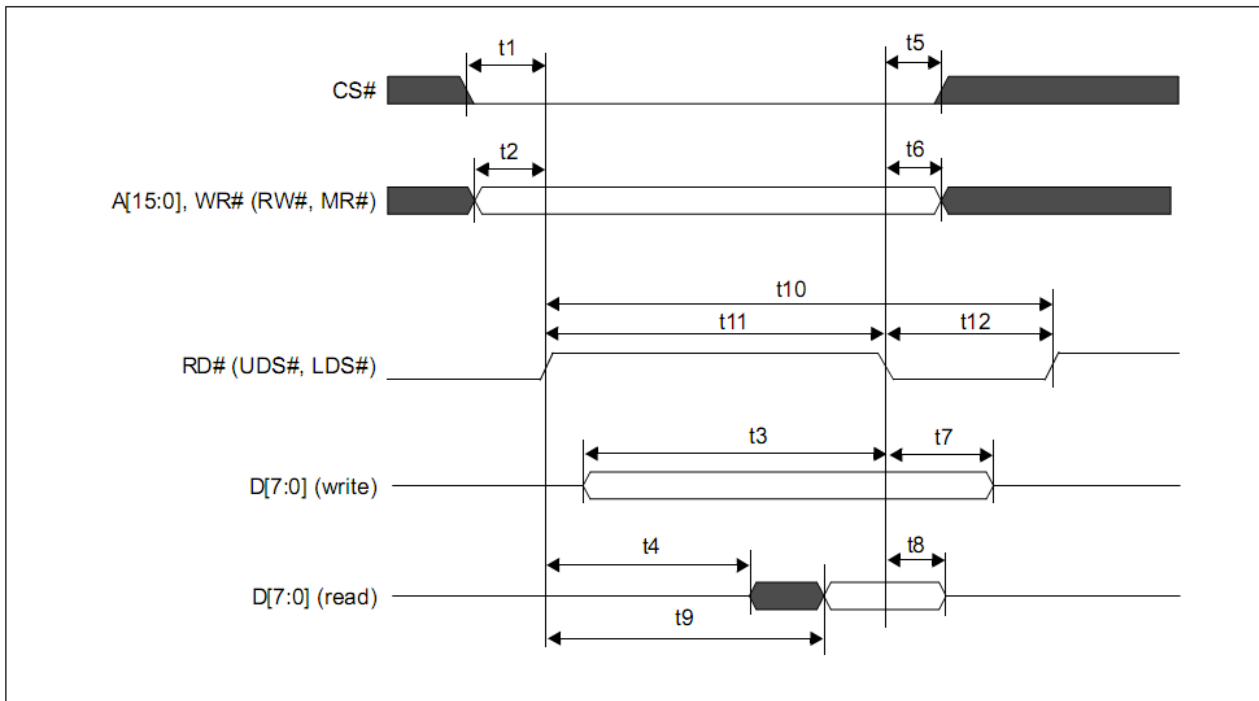
8080 Family Bus Interface Timing



Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	D[7:0] setup time to WR# rising edge (write cycle)	Note 2	—	Note 2	—	ns
t4	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t5	CS# hold time	7	—	7	—	ns
t6	A[15:0] hold time	7	—	7	—	ns
t7	D[7:0] hold time from WR# rising edge (write cycle)	5	—	5	—	ns
t8	D[7:0] hold time from RD# rising edge (read cycle)	3	14	3	14	ns
t9	RD# falling edge to valid Data (read cycle)	—	Note 3	—	Note 3	ns
t10	RD#, WR# cycle time	Note 4	—	Note 4	—	ns
t11	RD#, WR# pulse active time	5	—	5	—	Ts
t12	RD#, WR# pulse inactive time	Note 5	—	Note 5	—	ns

1. T_s = System clock period
2. t_{3min} = $2T_s + 5$
3. t_{9max} = $4T_s + 18$ (for 3.3V)
= $4T_s + 20$ (for 5.0V)
4. t_{10min} = $6T_s$ (for a read cycle followed by a read or write cycle)
= $7T_s + 2$ (for a write cycle followed by a write cycle)
= $10T_s + 2$ (for a write cycle followed by a read cycle)
5. t_{12min} = $1T_s$ (for a read cycle followed by a read or write cycle)
= $2T_s + 2$ (for a write cycle followed by a write cycle)
= $5T_s + 2$ (for a write cycle followed by a read cycle)

6800 Family Bus Interface Timing



Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	D[7:0] setup time to RD# falling edge (write cycle)	Note 2	—	Note 2	—	ns
t4	RD# rising edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t5	CS# hold time	7	—	7	—	ns
t6	A[15:0] hold time	7	—	7	—	ns
t7	D[7:0] hold time from RD# falling edge (write cycle)	5	—	5	—	ns
t8	D[7:0] hold time from RD# falling edge (read cycle)	2	55	2	55	ns
t9	RD# rising edge to valid Data	—	Note 3	—	Note 3	ns
t10	RD# cycle time	Note 4	—	Note 4	—	ns
t11	RD# pulse active time	5	—	5	—	Ts
t12	RD# pulse inactive time	Note 5	—	Note 5	—	ns

1. T_s = System clock period
2. t_{3min} = $2T_s + 5$
3. t_{9max} = $4T_s + 18$ (for 3.3V)
= $4T_s + 20$ (for 5.0V)
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= $10T_s + 2$ (for a write cycle followed by a read cycle)
5. t_{12min} = $1T_s$ (for a read cycle followed by a read or write cycle)
= $2T_s + 2$ (for a write cycle followed by a write cycle)
= $5T_s + 2$ (for a write cycle followed by a read cycle)

Example Initialization Code

```
//-----  
Sub Writecom  
  Set P3.0  
  P1 = A  
  Reset P3.1  
  Reset P3.7  
  Set P3.4  
  Reset P3.4  
  Set P3.7  
  Set P3.1  
End Sub  
  
Sub Writedata  
  Reset P3.0  
  P1 = A  
  Reset P3.1  
  Reset P3.7  
  Set P3.4  
  Reset P3.4  
  Set P3.7  
  Set P3.1  
End Sub  
  
//-----  
Sub Init  
  Reset P3.6  
  Waitms 10  
  Set P3.6  
  Waitms 100  
  
  A = &H40  
  Call Writecom  
  A = &H30  
  Call Writedata  
  A = &H87  
  Call Writedata  
  A = &H07  
  Call Writedata  
  A = &H27  
  Call Writedata  
  A = &H50  
  Call Writedata  
  A = &HEF  
  Call Writedata  
  A = &H28  
  Call Writedata  
  A = &H00  
  Call Writedata  
  A = &H44  
  Call Writecom  
  A = &H00  
  Call Writedata  
  A = &H00  
  Call Writedata  
  A = &HEF  
  Call Writedata  
  A = &HB0  
  Call Writedata  
  A = &H04  
  Call Writedata  
  A = &HEF  
  
  'A0 = H = Write command  
  'move data to P1  
  'chip select  
  'R/W  
  'E  
  'E  
  'R/W  
  'CS  
  
  'A0 = L = Write data  
  
  'RESET  
  'wait  
  'RESET done  
  'wait  
  
  'system set command  
  'set parameters  
  'horizontal character size=8  
  'vertical character size=8  
  'display addresses per line  
  'total address range per line  
  '240 display lines  
  'virtual address1  
  'virtual address2  
  'scroll  
  'start address1  
  'start address2  
  '240 lines  
  '2nd screen start1  
  '2nd screen start2  
  '2nd screen 240 lines
```

```

Call Writedata
A = &H00
Call Writedata
A = &H00
Call Writedata
A = &H00
Call Writedata
A = &H00
Call Writedata
A = &H5A
Call Writecom
A = &H00
Call Writedata
A = &H5B
Call Writecom
A = &H00
Call Writedata
A = &H5D
Call Writecom
A = &H04
Call Writedata
A = &H86
Call Writedata
A = &H4C
Call Writecom

Call Clr

A = &H59
Call Writecom
A = &H14
Call Writedata
End Sub
//-----

```

```

'3rd screen address1
'3rd screen address2
'4th screen address1
'4th screen address2
'hdot scr
'horizontal pixel shift=0
'overlay
'OR
'cursor form
'5 pixels
'by 7 pixels
'cursor direction = right

'clear the screen

```

```

'disp on/off
'on

```

Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	+80°C , 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C , 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time.	+70°C, 200hrs	2
Low Temperature Operation	Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time.	-20°C , 200hrs	1,2
High Temperature / Humidity Operation	Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time.	+60°C , 90% RH , 96hrs	1,2
Thermal Shock resistance	Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress.	-20°C, 30min -> 25°C, 5min -> 70°C, 30min = 1 cycle 10 cycles	
Vibration test	Endurance test applying vibration to simulate transportation and use.	10-55Hz, 15mm amplitude. 60 sec in each of 3 directions X,Y,Z For 15 minutes	3
Static electricity test	Endurance test applying electric static discharge.	VS=800V, RS=330Ω, CS=150pF 10 times	

Note 1: No condensation to be observed.

Note 2: Conducted after 4 hours of storage at 25°C, 0%RH.

Note 3: Test performed on product itself, not inside a container.

Precautions for using LCDs/LCMs

See Precautions at www.newhavendisplay.com/specs/precautions.pdf

Warranty Information

See Terms & Conditions at http://www.newhavendisplay.com/index.php?main_page=terms

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