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FDMS86103L

N-Channel Shielded Gate PowerTrench[®] MOSFET

100 V, 81 A, 8 mΩ

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 8 mΩ at $V_{GS} = 10$ V, $I_D = 12$ A
- Max $r_{DS(on)}$ = 11 mΩ at $V_{GS} = 4.5$ V, $I_D = 10$ A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

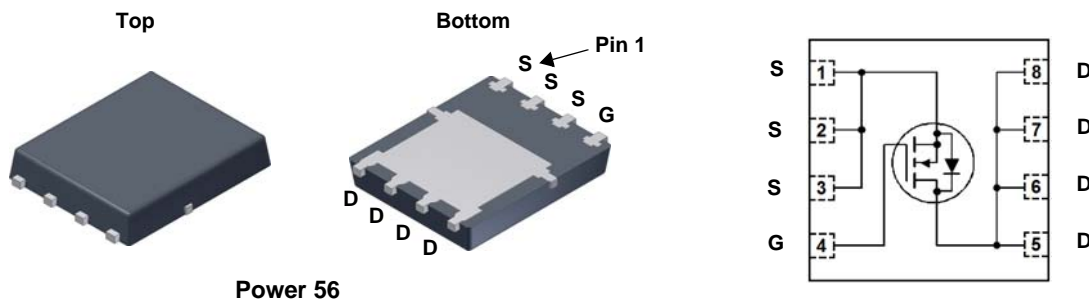


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench[®] process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Application

- DC-DC Conversion



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous	$T_C = 25$ °C (Note 5)	81
	Drain Current -Continuous	$T_C = 100$ °C (Note 5)	51
	-Continuous	$T_A = 25$ °C	12
	-Pulsed	(Note 4)	414
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	312
P_D	Power Dissipation	$T_C = 25$ °C	104
	Power Dissipation	$T_A = 25$ °C	2.5
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86103L	FDMS86103L	Power 56	13"	12 mm	3000 units

FDMS86103L N-Channel Shielded Gate PowerTrench[®] MOSFET

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		68		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	1.0	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 12\text{ A}$		6.4	8	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 10\text{ A}$		8.4	11	
		$V_{GS} = 10\text{ V}$, $I_D = 12\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		10.6	14	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 12\text{ A}$		59		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		2790	3710	pF
C_{oss}	Output Capacitance			469	625	pF
C_{rss}	Reverse Transfer Capacitance			22	35	pF
R_g	Gate Resistance			1.3		Ω

Switching Characteristics

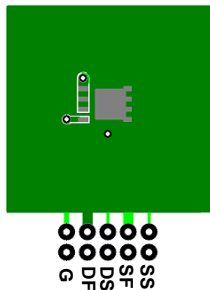
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$, $I_D = 12\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		13	23	ns	
t_r	Rise Time			7.2	15	ns	
$t_{d(off)}$	Turn-Off Delay Time			35	57	ns	
t_f	Fall Time			6	13	ns	
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V}$ to 10 V		43	60	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to 5 V	$V_{DD} = 50\text{ V}$, $I_D = 12\text{ A}$		23	32	nC
Q_{gs}	Gate to Source Charge				7.5		nC
Q_{gd}	Gate to Drain "Miller" Charge				7		nC

Drain-Source Diode Characteristics

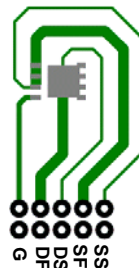
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2\text{ A}$ (Note 2)		0.70	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = 12\text{ A}$ (Note 2)		0.78	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		57	90	ns
Q_{rr}	Reverse Recovery Charge			68	108	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $125\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.

3. Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1\text{ mH}$, $I_{AS} = 25\text{ A}$, $V_{DD} = 90\text{ V}$, $V_{GS} = 10\text{ V}$

4. Pulsed Id please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

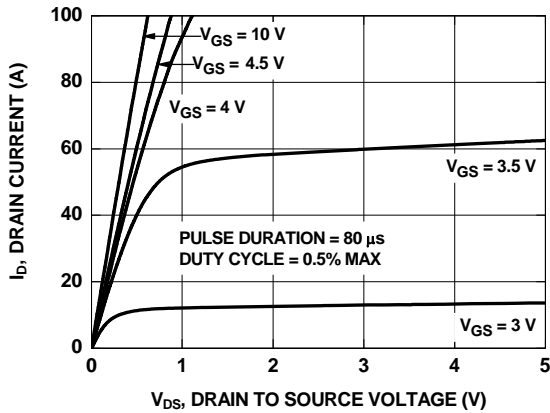


Figure 1. On-Region Characteristics

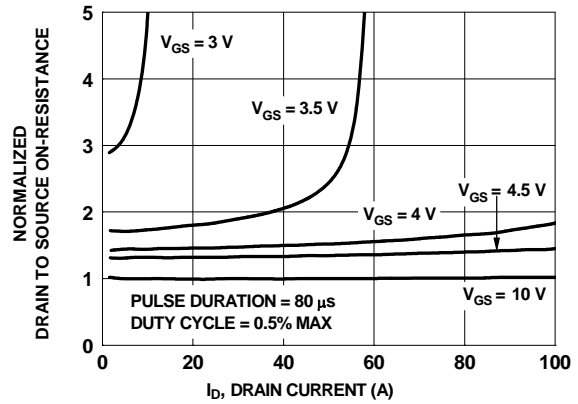


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

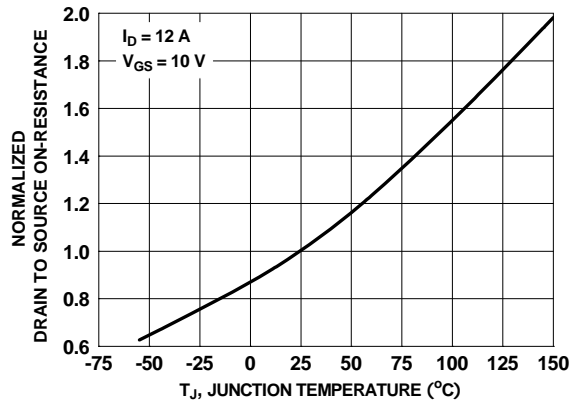


Figure 3. Normalized On-Resistance vs Junction Temperature

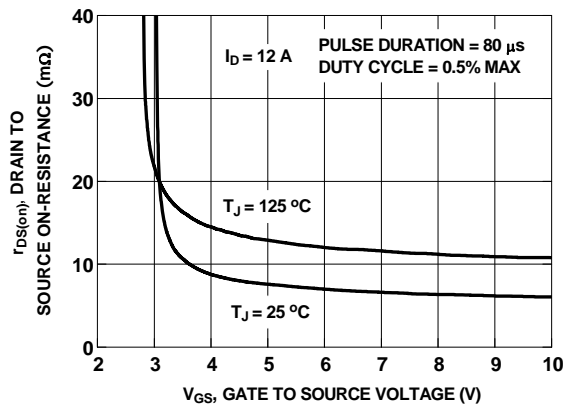


Figure 4. On-Resistance vs Gate to Source Voltage

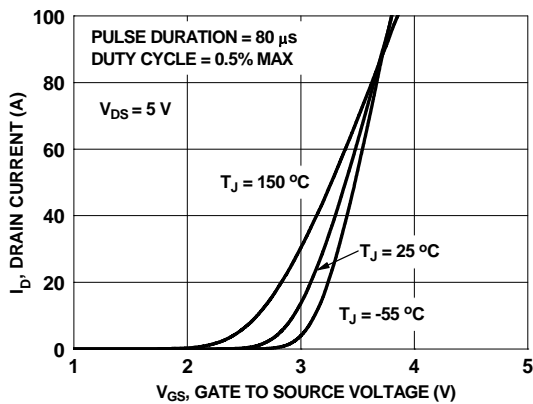


Figure 5. Transfer Characteristics

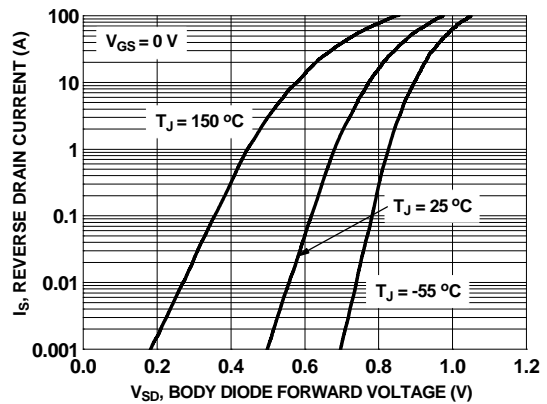


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

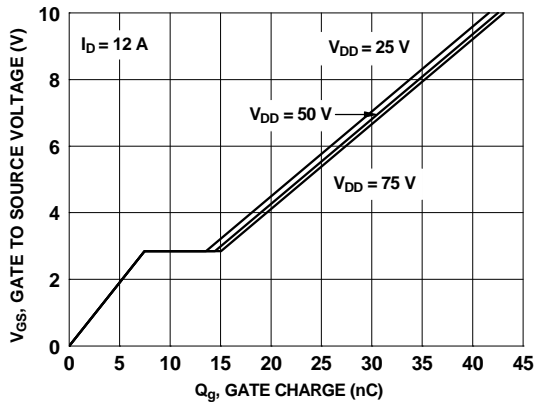


Figure 7. Gate Charge Characteristics

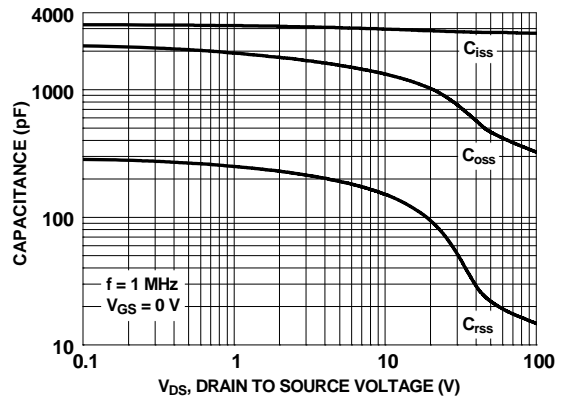


Figure 8. Capacitance vs Drain to Source Voltage

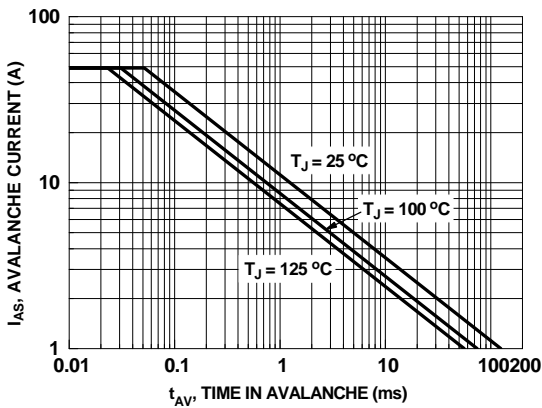


Figure 9. Unclamped Inductive Switching Capability

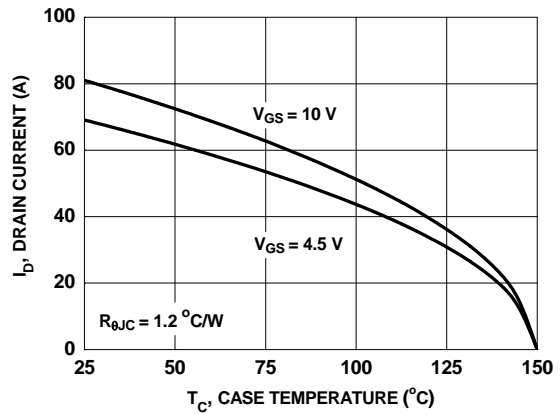


Figure 10. Maximum Continuous Drain Current vs Case Temperature

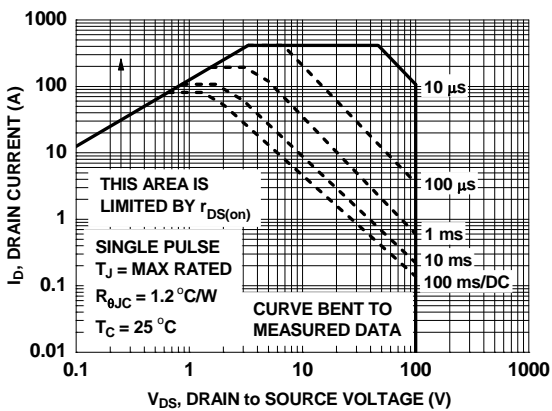


Figure 11. Forward Bias Safe Operating Area

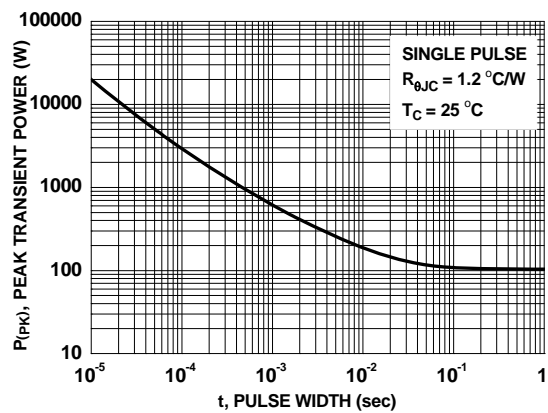


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

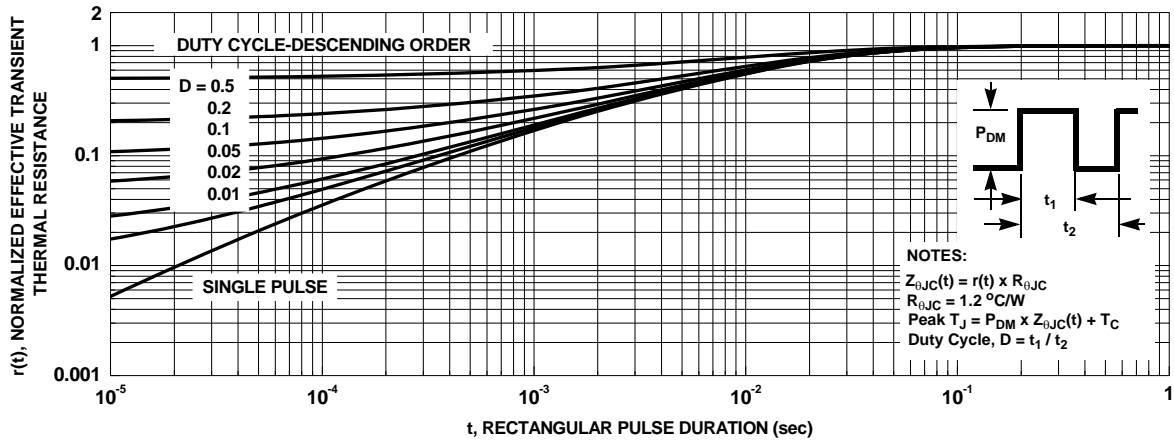


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

PQFN8 5X6, 1.27P
CASE 483AE
ISSUE A



TOP VIEW



LAND PATTERN RECOMMENDATION

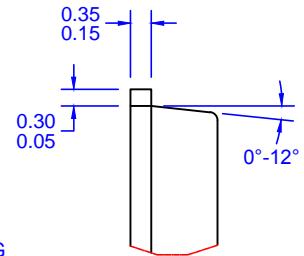


SIDE VIEW

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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