# ISL6594A, ISL6594B

Advanced Synchronous Rectified Buck MOSFET Drivers with Protection Features

FN9157
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The ISL6594A and ISL6594B are high frequency MOSFET drivers specifically designed to drive upper and lower power N-Channel MOSFETs in a synchronous rectified buck converter topology. These drivers combined with the ISL6592 Digital Multi-Phase Buck PWM controller and N-Channel MOSFETs form a complete core-voltage regulator solution for advanced microprocessors.

The ISL6594A drives the upper gate to 12V, while the lower gate can be independently driven over a range from 5V to 12V. The ISL6594B drives both upper and lower gates over a range of 5V to 12V. This drive-voltage provides the flexibility necessary to optimize applications involving trade-offs between gate charge and conduction losses.

An adaptive zero shoot-through protection is integrated to prevent both the upper and lower MOSFETs from conducting simultaneously and to minimize the dead time. These products add an overvoltage protection feature operational before VCC exceeds its turn-on threshold, at which the PHASE node is connected to the gate of the low side MOSFET (LGATE). The output voltage of the converter is then limited by the threshold of the low side MOSFET, which provides some protection to the microprocessor if the upper MOSFET(s) is shorted during initial start-up.

These drivers also feature a three-state PWM input which, working together with Intersil's multi-phase PWM controllers, prevents a negative transient on the output voltage when the output is shut down. This feature eliminates the Schottky diode that is used in some systems for protecting the load from reversed output voltage events.

## Features

- Dual MOSFET Drives for Synchronous Rectified Bridge
- Adjustable Gate Voltage (5V to 12V) for Optimal Efficiency
- 36V Internal Bootstrap Schottky Diode
- Bootstrap Capacitor Overcharging Prevention
- Supports High Switching Frequency (up to 2MHz)
  - 3A Sinking Current Capability
  - Fast Rise/Fall Times and Low Propagation Delays
- Three-State PWM Input for Output Stage Shutdown
- Three-State PWM Input Hysteresis for Applications with Power Sequencing Requirement
- Pre-POR Overvoltage Protection
- VCC Undervoltage Protection
- Expandable Bottom Copper Pad for Enhanced Heat Sinking
- Dual Flat No-Lead (DFN) Package
  - Near Chip-Scale Package Footprint; Improves PCB Efficiency and Thinner in Profile
- Pb-Free Available (RoHS Compliant)

## Applications

- Core Regulators for Intel® and AMD® Microprocessors
- High Current DC/DC Converters
- High Frequency and High Efficiency VRM and VRD

## Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- Technical Brief TB417 for Power Train Design, Layout Guidelines, and Feedback Compensation Design

## Ordering Information

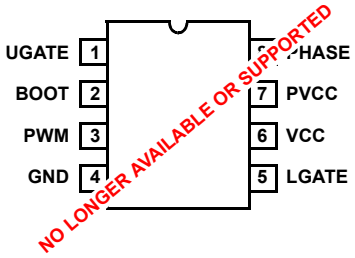
| PART NUMBER | PART MARKING | TEMP. RANGE (°C) | PACKAGE (RoHS Compliant) | PKG. DWG. # |
|---|---|---|---|---|
| ISL6594ACRZ* (Note) | 94AZ | 0 to +85 | 10 Ld 3x3 DFN | L10.3x3 |
| ISL6594BCBZ* (Note) **(No longer available, recommended replacement: ISL6594ACRZ-T)** | 6594 BCBZ | 0 to +85 | 8 Ld SOIC | M8.15 |

*Please refer to TB347 for details on reel specifications.

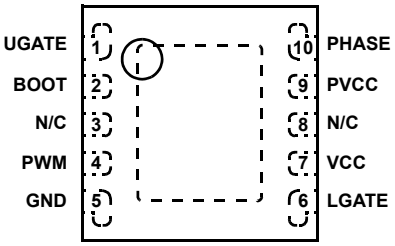
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Pinouts

**ISL6594ACB, ISL6594BCB**
**(8 LD SOIC)**
TOP VIEW

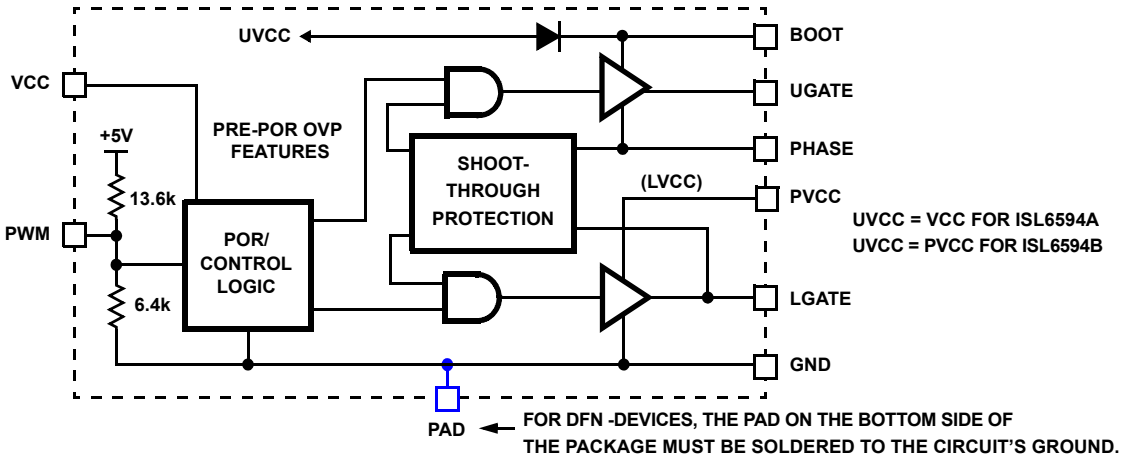



**ISL6594ACR, ISL6594BCR**
**(10 LD 3x3 DFN)**
TOP VIEW

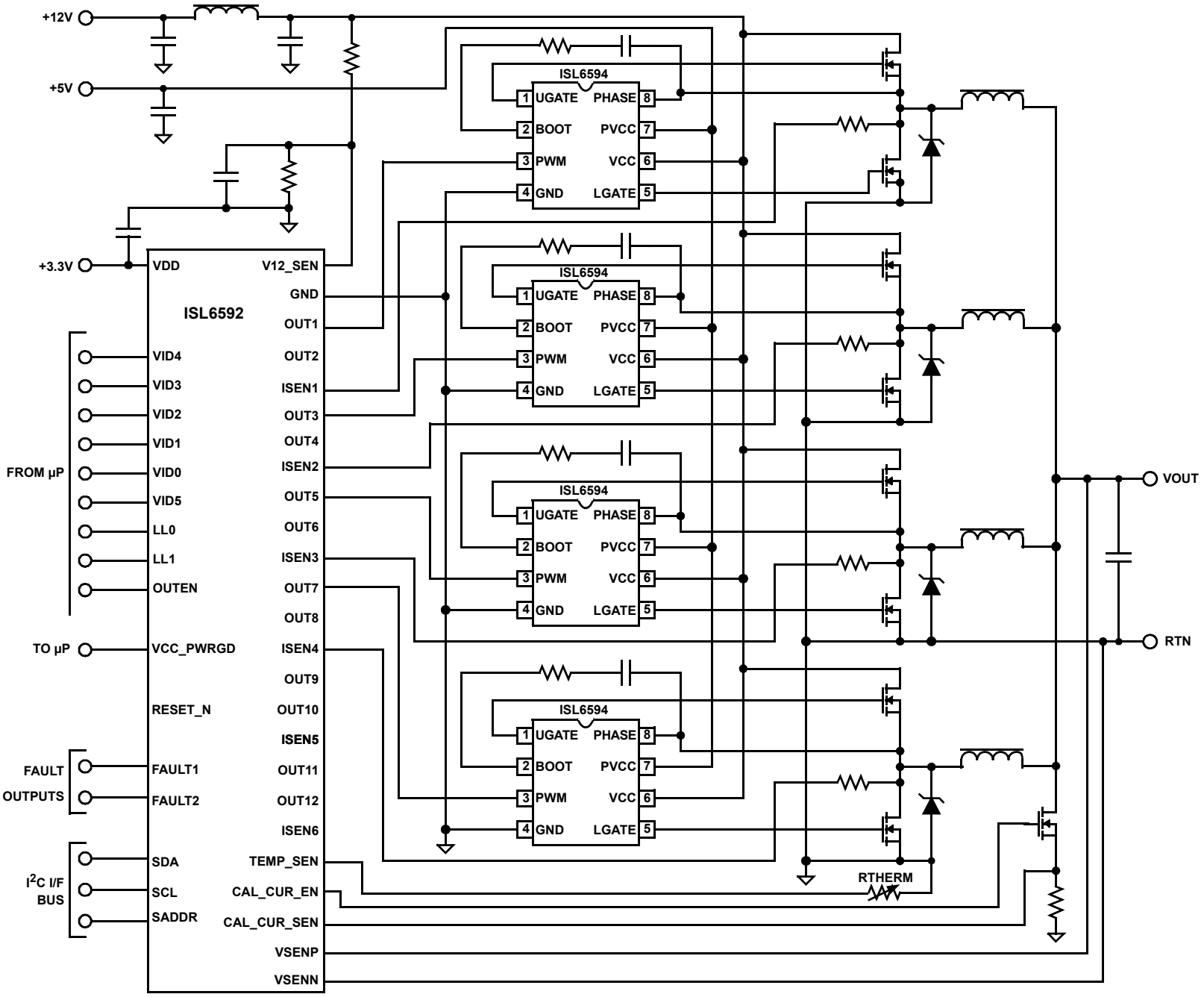



## Block Diagram

**ISL6594A AND ISL6594B**



## Typical Application - 4-Channel Converter Using ISL6592 and ISL6594A Gate Drivers



## Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . .15V
Supply Voltage (PVCC) . . . . . VCC + 0.3V
BOOT Voltage ($V_{BOOT}$) . . . . . .36V
Input Voltage ($V_{PWM}$) . . . . . GND - 0.3V to 7V
UGATE . . . . . $V_{PHASE}$ - 0.3$V_{DC}$ to $V_{BOOT}$ + 0.3V
$V_{PHASE}$ - 3.5V (<100ns Pulse Width, 2µJ) to $V_{BOOT}$ + 0.3V
LGATE . . . . . GND - 0.3$V_{DC}$ to $V_{PVCC}$ + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to $V_{PVCC}$ + 0.3V
PHASE . . . . . GND - 0.3$V_{DC}$ to 15$V_{DC}$ ($V_{PVCC}$ = 12V)
GND - 8V (<400ns, 20µJ) to 30V (<200ns, VBOOT - GND < 36V)
ESD Rating
Human Body Model . . . . . Class I JEDEC STD

## Thermal Information

| Thermal Resistance | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| SOIC Package (Note 1) . . . . . | 100 | N/A |
| DFN Package (Notes 2, 3) . . . . . | 48 | 7 |

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Recommended Operating Conditions

Ambient Temperature Range . . . . . 0°C to +85°C
Maximum Operating Junction Temperature . . . . . +125°C
Supply Voltage, $V_{CC}$ . . . . . 12V ±10%
Supply Voltage Range, PVCC . . . . . 5V to 12V ±10%

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

1. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air.
2. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For $\theta_{JC}$, the “case temp” location is the center of the exposed metal pad on the package underside.

## Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **VCC SUPPLY CURRENT** | | | | | | |
| Bias Supply Current | $I_{VCC}$ | ISL6594A, $f_{PWM}$ = 300kHz, $V_{VCC}$ = 12V | - | 8 | - | mA |
| | | ISL6594B, $f_{PWM}$ = 300kHz, $V_{VCC}$ = 12V | - | 4.5 | - | mA |
| | $I_{VCC}$ | ISL6594A, $f_{PWM}$ = 1MHz, $V_{VCC}$ = 12V | - | 10.5 | - | mA |
| | | ISL6594B, $f_{PWM}$ = 1MHz, $V_{VCC}$ = 12V | - | 5 | - | mA |
| Gate Drive Bias Current | $I_{PVCC}$ | ISL6594A, $f_{PWM}$ = 300kHz, $V_{PVCC}$ = 12V | - | 4 | - | mA |
| | | ISL6594B, $f_{PWM}$ = 300kHz, $V_{PVCC}$ = 12V | - | 7.5 | - | mA |
| | $I_{PVCC}$ (Note 4) | ISL6594A, $f_{PWM}$ = 1MHz, $V_{PVCC}$ = 12V | - | 5 | - | mA |
| | | ISL6594B, $f_{PWM}$ = 1MHz, $V_{PVCC}$ = 12V | - | 8.5 | - | mA |
| **POWER-ON RESET AND ENABLE** | | | | | | |
| VCC Rising Threshold | | | 9.35 | 9.8 | 10.0 | V |
| VCC Falling Threshold | | | 7.35 | 7.6 | 8.0 | V |
| **PWM INPUT (See Timing Diagram on page 6)** | | | | | | |
| Input Current | $I_{PWM}$ | $V_{PWM}$ = 3.3V | - | 505 | - | µA |
| | | $V_{PWM}$ = 0V | - | -460 | - | µA |
| PWM Rising Threshold (Note 4) | | $V_{CC}$ = 12V | - | 1.70 | - | V |
| PWM Falling Threshold (Note 4) | | $V_{CC}$ = 12V | - | 1.30 | - | V |
| Typical Three-State Shutdown Window | | $V_{CC}$ = 12V | 1.23 | - | 1.82 | V |
| Three-State Lower Gate Falling Threshold | | $V_{CC}$ = 12V | - | 1.18 | - | V |
| Three-State Lower Gate Rising Threshold | | $V_{CC}$ = 12V | - | 0.76 | - | V |
| Three-State Upper Gate Rising Threshold | | $V_{CC}$ = 12V | - | 2.36 | - | V |
| Three-State Upper Gate Falling Threshold | | $V_{CC}$ = 12V | - | 1.96 | - | V |
| Shutdown Hold-off Time | $t_{TSSHD}$ | | - | 245 | - | ns |
| UGATE Rise Time | $t_{RU}$ | $V_{PVCC}$ = 12V, 3nF Load, 10% to 90% | - | 26 | - | ns |

**Electrical Specifications** Recommended Operating Conditions, Unless Otherwise Noted. **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| LGATE Rise Time | $t_{RL}$ | $V_{PVCC}$ = 12V, 3nF Load, 10% to 90% | - | 18 | - | ns |
| UGATE Fall Time (Note 4) | $t_{FU}$ | $V_{PVCC}$ = 12V, 3nF Load, 90% to 10% | - | 18 | - | ns |
| LGATE Fall Time (Note 4) | $t_{FL}$ | $V_{PVCC}$ = 12V, 3nF Load, 90% to 10% | - | 12 | - | ns |
| UGATE Turn-On Propagation Delay (Note 4) | $t_{PDHU}$ | $V_{PVCC}$ = 12V, 3nF Load, Adaptive | - | 10 | - | ns |
| LGATE Turn-On Propagation Delay (Note 4) | $t_{PDHL}$ | $V_{PVCC}$ = 12V, 3nF Load, Adaptive | - | 10 | - | ns |
| UGATE Turn-Off Propagation Delay (Note 4) | $t_{PDLU}$ | $V_{PVCC}$ = 12V, 3nF Load | - | 10 | - | ns |
| LGATE Turn-Off Propagation Delay (Note 4) | $t_{PDLL}$ | $V_{PVCC}$ = 12V, 3nF Load | - | 10 | - | ns |
| LG/UG Three-State Propagation Delay (Note 4) | $t_{PDTS}$ | $V_{PVCC}$ = 12V, 3nF Load | - | 10 | - | ns |
| **OUTPUT** | | | | | | |
| Upper Drive Source Current (Note 4) | $I_{U\_SOURCE}$ | $V_{PVCC}$ = 12V, 3nF Load | - | 1.25 | - | A |
| Upper Drive Source Impedance | $R_{U\_SOURCE}$ | 150mA Source Current | 1.4 | 2.0 | 3.0 | Ω |
| Upper Drive Sink Current (Note 4) | $I_{U\_SINK}$ | $V_{PVCC}$ = 12V, 3nF Load | - | 2 | - | A |
| Upper Drive Sink Impedance | $R_{U\_SINK}$ | 150mA Sink Current | 0.9 | 1.65 | 3.0 | Ω |
| Lower Drive Source Current (Note 4) | $I_{L\_SOURCE}$ | $V_{PVCC}$ = 12V, 3nF Load | - | 2 | - | A |
| Lower Drive Source Impedance | $R_{L\_SOURCE}$ | 150mA Source Current | 0.85 | 1.3 | 2.2 | Ω |
| Lower Drive Sink Current (Note 4) | $I_{L\_SINK}$ | $V_{PVCC}$ = 12V, 3nF Load | - | 3 | - | A |
| Lower Drive Sink Impedance | $R_{L\_SINK}$ | 150mA Sink Current | 0.60 | 0.94 | 1.35 | Ω |

NOTE:

4. Limits should be considered typical and are not production tested.

## *Functional Pin Description*

| PACKAGE PIN # | | PIN SYMBOL | FUNCTION |
|---|---|---|---|
| SOIC | DFN | | |
| 1 | 1 | UGATE | Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET. |
| 2 | 2 | BOOT | Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See “Internal Bootstrap Device” on page 7 for guidance in choosing the capacitor value. |
| - | 3, 8 | N/C | No Connection. |
| 3 | 4 | PWM | The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see “Three-State PWM Input” on page 6 for further details. Connect this pin to the PWM output of the controller. |
| 4 | 5 | GND | Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver. |
| 5 | 6 | LGATE | Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET. |
| 6 | 7 | VCC | Connect this pin to a +12V bias supply. Place a high quality low ESR ceramic capacitor from this pin to GND. |
| 7 | 9 | PVCC | This pin supplies power to both upper and lower gate drives in ISL6594B; only the lower gate drive in ISL6594A. Its operating range is +5V to 12V. Place a high quality low ESR ceramic capacitor from this pin to GND. |
| 8 | 10 | PHASE | Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive. |
| 9 | 11 | PAD | Connect this pad to the power ground plane (GND) via thermally enhanced connection. |

## Description

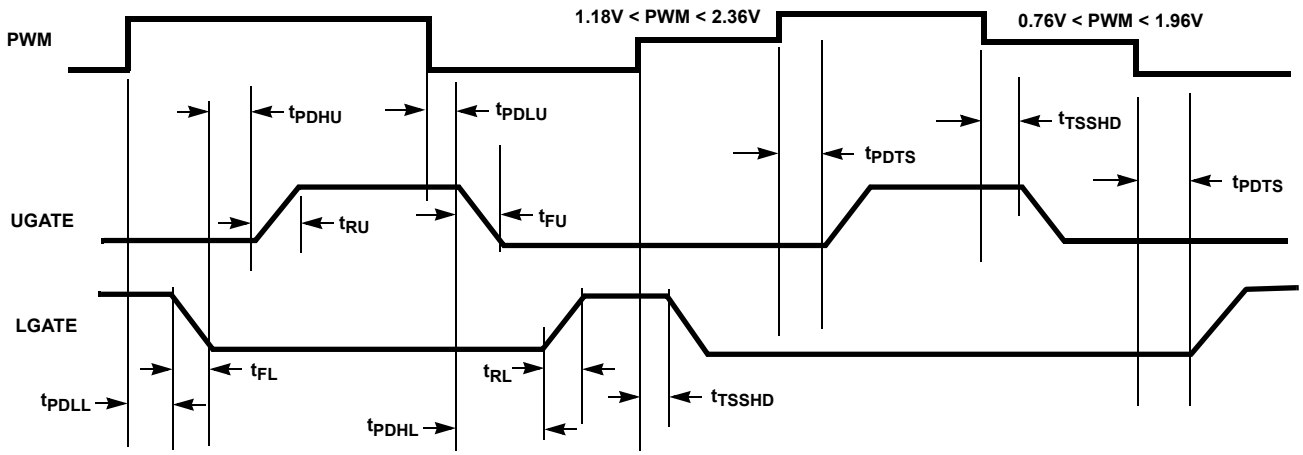



FIGURE 1. TIMING DIAGRAM

### Operation

Designed for versatility and speed, the ISL6594A and ISL6594B MOSFET drivers control both high-side and low-side N-Channel FETs of a half-bridge power train from one externally provided PWM signal.

Prior to VCC exceeding its POR level, the Pre-POR overvoltage protection function is activated during initial start-up; the upper gate (UGATE) is held low and the lower gate (LGATE), controlled by the Pre-POR overvoltage protection circuits, is connected to the PHASE. Once the VCC voltage surpasses the VCC Rising Threshold (See “Electrical Specifications” on page 4), the PWM signal takes control of gate transitions. A rising edge on PWM initiates the turn-off of the lower MOSFET (see “Timing Diagram” on page 6). After a short propagation delay [$t_{PDLL}$], the lower gate begins to fall. Typical fall times [$t_{FL}$] are provided in “Electrical Specifications” on page 4. Adaptive shoot-through circuitry monitors the LGATE voltage and determines the upper gate delay time [$t_{PDHU}$]. This prevents both the lower and upper MOSFETs from conducting simultaneously. Once this delay period is complete, the upper gate drive begins to rise [$t_{RU}$] and the upper MOSFET turns on.

A falling transition on PWM results in the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [$t_{PDLU}$] is encountered before the upper gate begins to fall [$t_{FU}$]. Again, the adaptive shoot-through circuitry determines the lower gate delay time, $t_{PDHL}$. The PHASE voltage and the UGATE voltage are monitored, and the lower gate is allowed to rise after PHASE drops below a level or the voltage of UGATE to PHASE reaches a level depending upon the current direction (See next section for details). The lower gate then rises [$t_{RL}$], turning on the lower MOSFET.

### Adaptive Zero Shoot-Through Deadtime Control

These drivers incorporate an adaptive deadtime control technique to minimize deadtime, resulting in high efficiency from the reduced freewheeling time of the lower MOSFETs’ body-diode conduction, and to prevent the upper and lower MOSFETs from conducting simultaneously. This is accomplished by ensuring either rising gate turns on its MOSFET with minimum and sufficient delay after the other has turned off.

During turn-off of the lower MOSFET, the LGATE voltage is monitored until it drops below 1.75V, at which time the UGATE is released to rise after 20ns of propagation delay. Once the PHASE is high, the adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn on.

### Three-State PWM Input

A unique feature of these drivers and other Intersil drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set hold off time, the driver outputs are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the “Electrical Specifications” on page 4 determine when the lower and upper gates are enabled.

This feature helps prevent a negative transient on the output voltage when the output is shut down, eliminating the Schottky diode that is used in some systems for protecting the load from reversed output voltage events.

In addition, more than 400mV hysteresis also incorporates into the three-state shutdown window to eliminate PWM input oscillations due to the capacitive load seen by the PWM input through the body diode of the controller's PWM output when the power-up and/or power-down sequence of bias supplies of the driver and PWM controller are required.

### *Power-On Reset (POR) Function*

During initial start-up, the VCC voltage rise is monitored. Once the rising VCC voltage exceeds 9.8V (typically), operation of the driver is enabled and the PWM input signal takes control of the gate drives. If VCC drops below the falling threshold of 7.6V (typically), operation of the driver is disabled.

### *Pre-POR Overvoltage Protection*

For the ISL6594A, prior to VCC exceeding its POR level, the upper gate is held low. For the ISL6594B, the upper gate driver is powered from PVCC and will be held low when a voltage of 2.75V or higher is present on PVCC as VCC surpasses its POR threshold. For both devices, the lower gate is controlled by the overvoltage protection circuits during initial start-up. The PHASE is connected to the gate of the low side MOSFET (LGATE), which provides some protection to the microprocessor if the upper MOSFET(s) is shorted during initial start-up. For complete protection, the low side MOSFET should have a gate threshold well below the maximum voltage rating of the load/microprocessor.

When VCC drops below its POR level, both gates pull low and the Pre-POR overvoltage protection circuits are not activated until VCC resets.

### *Internal Bootstrap Device*

Both drivers feature an internal bootstrap Schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the trailing-edge of the PHASE node. This reduces voltage stress on the boot to phase pins.

The bootstrap capacitor must have a maximum voltage rating above UVCC + 5V and its capacitance value can be chosen from Equation 1:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}} \qquad \text{(EQ. 1)}$$

$$Q_{GATE} = \frac{Q_{G1} \bullet UVCC}{V_{GS1}} \bullet N_{Q1}$$

where $Q_{G1}$ is the amount of gate charge per upper MOSFET at $V_{GS1}$ gate-source voltage and $N_{Q1}$ is the number of control MOSFETs. The $\Delta V_{BOOT\_CAP}$ term is defined as the allowable droop in the rail of the upper gate drive.

As an example, suppose two IRLR7821 FETs are chosen as the upper MOSFETs. The gate charge, $Q_G$, from the data sheet is 10nC at 4.5V ($V_{GS}$) gate-source voltage. Then the $Q_{GATE}$ is calculated to be 53nC for UVCC (i.e. PVCC in ISL6594B, VCC in ISL6594A) = 12V. We will assume a 200mV droop in drive voltage over the PWM cycle. We find that a bootstrap capacitance of at least 0.267µF is required.

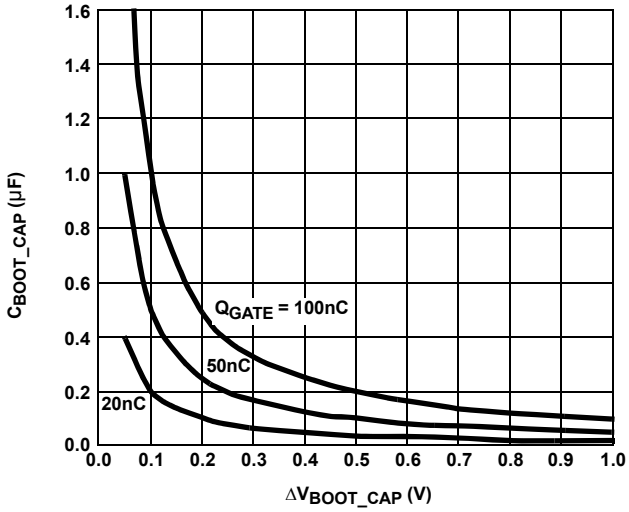



**FIGURE 2. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE**

### *Gate Drive Voltage Versatility*

The ISL6594A and ISL6594B provide the user flexibility in choosing the gate drive voltage for efficiency optimization. The ISL6594A upper gate drive is fixed to VCC [+12V], but the lower drive rail can range from 12V down to 5V depending on what voltage is applied to PVCC. The ISL6594B ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC sets both gate drive rail voltages simultaneously.

### *Power Dissipation*

Package power dissipation is mainly a function of the switching frequency ($f_{SW}$), the output drive impedance, the external gate resistance, and the selected MOSFET's internal gate resistance and total gate charge. Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. The maximum allowable IC power dissipation for the SO8 package is approximately 800mW at room temperature, while the power dissipation capacity in the DFN package with an exposed heat escape pad is more than 1.5W. The DFN package is more suitable for high frequency applications. See "Layout Considerations" on page 8 for thermal transfer improvement suggestions. When designing the driver into an application, it is recommended that the following calculation is used to ensure safe operation at the

desired frequency for the selected MOSFETs. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated with Equations 2 and 3, respectively:

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \bullet VCC \quad \text{(EQ. 2)}$$

$$P_{Qg\_Q1} = \frac{Q_{G1} \bullet UVCC^2}{V_{GS1}} \bullet f_{SW} \bullet N_{Q1}$$

$$P_{Qg\_Q2} = \frac{Q_{G2} \bullet LVCC^2}{V_{GS2}} \bullet f_{SW} \bullet N_{Q2}$$

$$I_{DR} = \left( \frac{Q_{G1} \bullet UVCC \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet LVCC \bullet N_{Q2}}{V_{GS2}} \right) \bullet f_{SW} + I_Q \quad \text{(EQ. 3)}$$

where the gate charge ($Q_{G1}$ and $Q_{G2}$) is defined at a particular gate to source voltage ($V_{GS1}$and $V_{GS2}$) in the corresponding MOSFET datasheet; $I_Q$ is the driver's total quiescent current with no load at both drive outputs; $N_{Q1}$ and $N_{Q2}$ are number of upper and lower MOSFETs, respectively; UVCC and LVCC are the drive voltages for both upper and lower FETs, respectively. The $I_Q$*VCC product is the quiescent power of the driver without capacitive load and is typically 116mW at 300kHz.

The total gate drive power losses are dissipated among the resistive components along the transition path. The drive resistance dissipates a portion of the total gate drive power losses, the rest will be dissipated by the external gate resistors ($R_{G1}$ and $R_{G2}$) and the internal gate resistors ($R_{GI1}$ and $R_{GI2}$) of MOSFETs. Figures 3 and 4 show the typical upper and lower gate drives turn-on transition path. The power dissipation on the driver can be roughly estimated as shown in Equation 4:

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + I_Q \bullet VCC \quad \text{(EQ. 4)}$$

$$P_{DR\_UP} = \left( \frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}} \right) \bullet \frac{P_{Qg\_Q1}}{2}$$

$$P_{DR\_LOW} = \left( \frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}} \right) \bullet \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

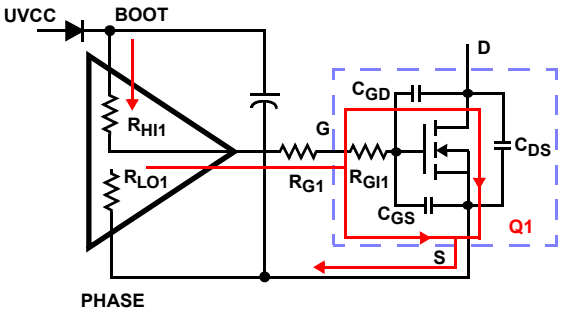



FIGURE 3. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

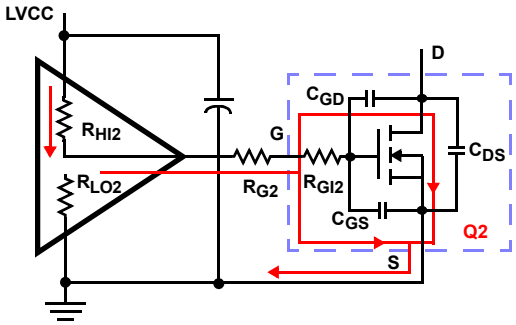



FIGURE 4. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

### *Layout Considerations*

For heat spreading, place copper underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried copper plane(s) with thermal vias. This combination of vias for vertical heat escape, extended copper plane, and buried planes for heat spreading allows the IC to achieve its full thermal potential.

Place each channel power component as close to each other as possible to reduce PCB copper losses and PCB parasitics: shortest distance between DRAINs of upper FETs and SOURCEs of lower FETs; shortest distance between DRAINs of lower FETs and the power ground. Thus, smaller amplitudes of positive and negative ringing are on the switching edges of the PHASE node. However, some space in between the power components is required for good airflow. The traces from the drivers to the FETs should be kept short and wide to reduce the inductance of the traces and to promote clean drive signals.

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| September 11, 2015 | FN9157.6 | Updated Ordering Information table on page 2.<br>Added Revision History and About Intersil sections.<br>Updated Package Outline Drawing L10.3x3 to the latest revision.<br>-Revision 3 to Revision 4 changes - Add Typical Recommended Land Pattern<br>-Revision 4 to Revision 5 changes - Converted to newer standard<br>-Revision 5 to Revision 6 changes - Changed Note 4 from "Dimension b applies..." to "Lead width applies...", Changed Note callout in Detail X from 4 to 5, Changed height in side view from 0.90 MAX to 1.00 MAX, Added Note 4 callout next to lead width in Bottom View, In Land Pattern, corrected lead shape for 4 corner pins to "L" shape (was rectangular and did not match bottom view)<br>-Revision 6 to Revision 7 changes - Removed package outline and included center to center distance between lands on recommended land pattern. Removed Note 4 "Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip." since it is not applicable to this package. Renumbered notes accordingly.<br>-Revision 7 to Revision 8 changes - Corrected L-shaped leads in Bottom view and land pattern so that they align with the rest of the leads (L shaped leads were shorter)<br>-Revision 8 to Revision 9 changes - Added missing dimension 0.415 in Typical Recommended land pattern.<br>-Revision 9 to Revision 10 changes - Shortened the e-pad rectangle on both the recommended land pattern and the package bottom view to line up with the centers of the corner pins.<br>-Revision 10 to Revision 11 changes - Tiebar Note 4 updated<br>From: Tiebar shown (if present) is a non-functional feature.<br>To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends). |

## About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

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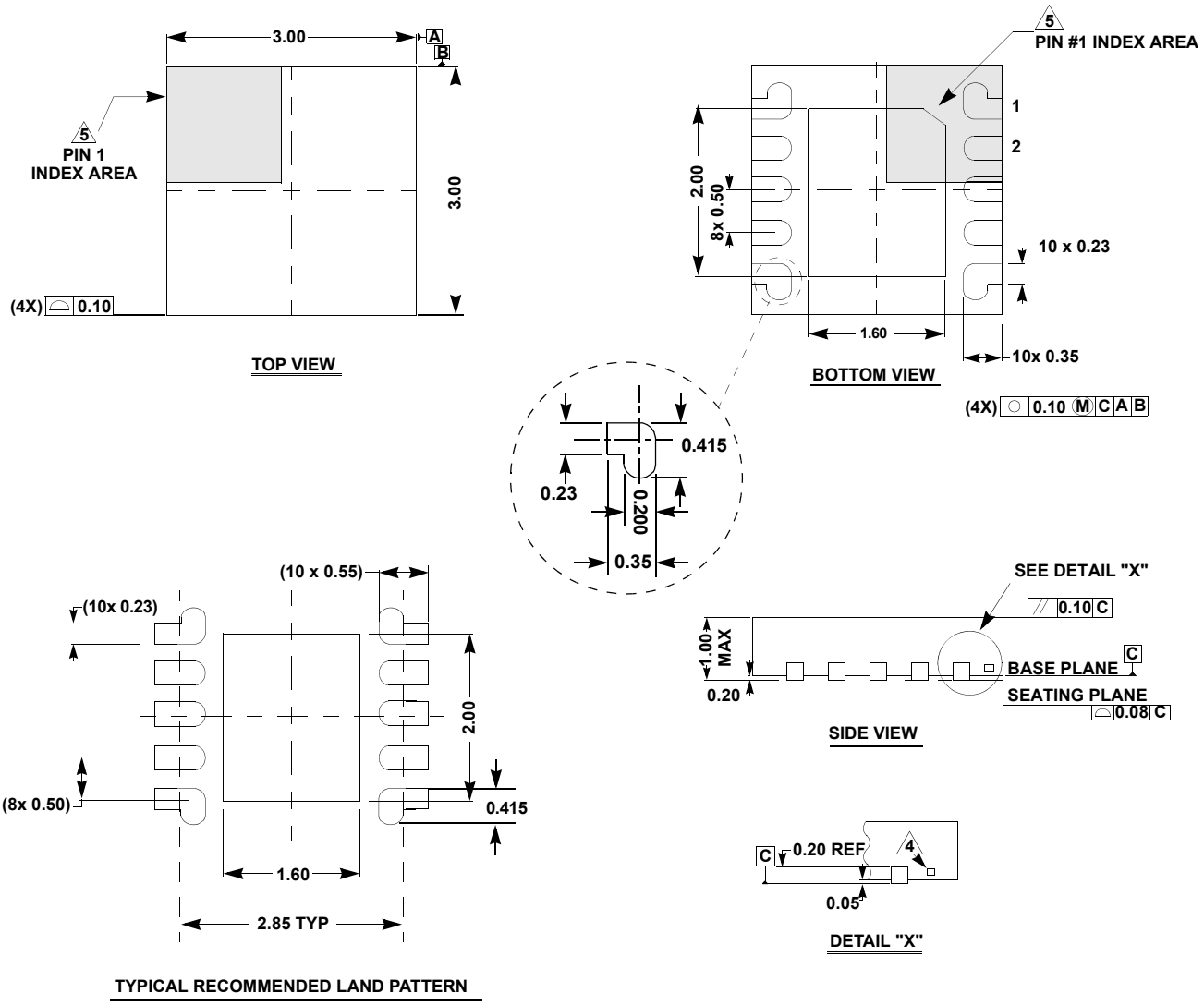
# Package Outline Drawing

## L10.3x3

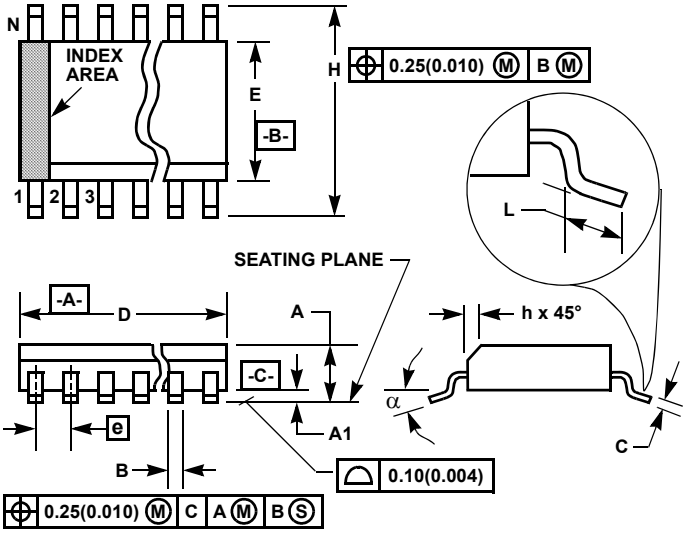
**10 LEAD DUAL FLAT PACKAGE (DFN)**
**Rev 11, 3/15**




**NOTES:**

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

## *Small Outline Plastic Packages (SOIC)*




NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

**M8.15 (JEDEC MS-012-AA ISSUE C)**
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

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