

# 74LVC244A; 74LVCH244A

Octal buffer/line driver; 3-state

Rev. 8 — 26 June 2013

Product data sheet

## 1. General description

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The 74LVC244A; 74LVCH244A is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs  $\overline{1OE}$  and  $\overline{2OE}$ . A HIGH on  $\overline{nOE}$  causes the outputs to assume a high-impedance OFF-state.

Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

Inputs can be driven from either 3.3 V or 5.0 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 V and 5 V environment.

The 74LVCH244A bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

## 2. Features and benefits

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- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when  $V_{CC} = 0$  V
- Bus hold on all data inputs (74LVCH244A only)
- Complies with JEDEC standard:
  - ◆ JESD8-7A (1.65 V to 1.95 V)
  - ◆ JESD8-5A (2.3 V to 2.7 V)
  - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115B exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC244AD 74LVCH244AD	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVC244ADB 74LVCH244ADB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVC244APW 74LVCH244APW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVC244ABQ 74LVCH244ABQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74LVC244ABX 74LVCH244ABX	-40 °C to +125 °C	DHXQFN20	plastic dual in-line compatible thermal enhanced extremely thin quad flat package; no leads; 20 terminals; body 4.5 × 2.5 × 0.5 mm	SOT1045-2

### 4. Functional diagram

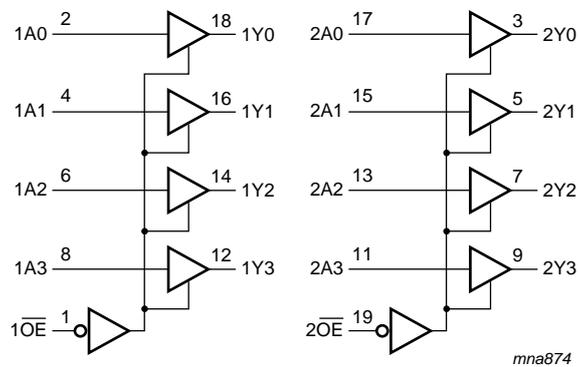


Fig 1. Logic symbol

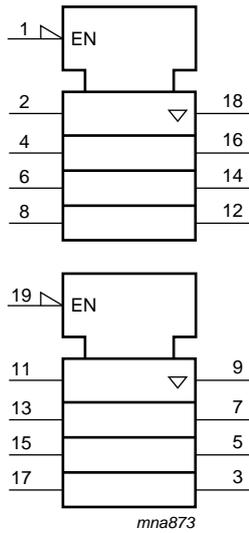


Fig 2. IEC logic diagram

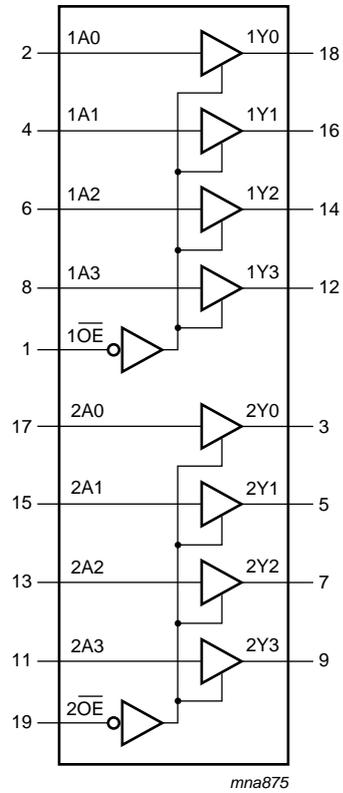
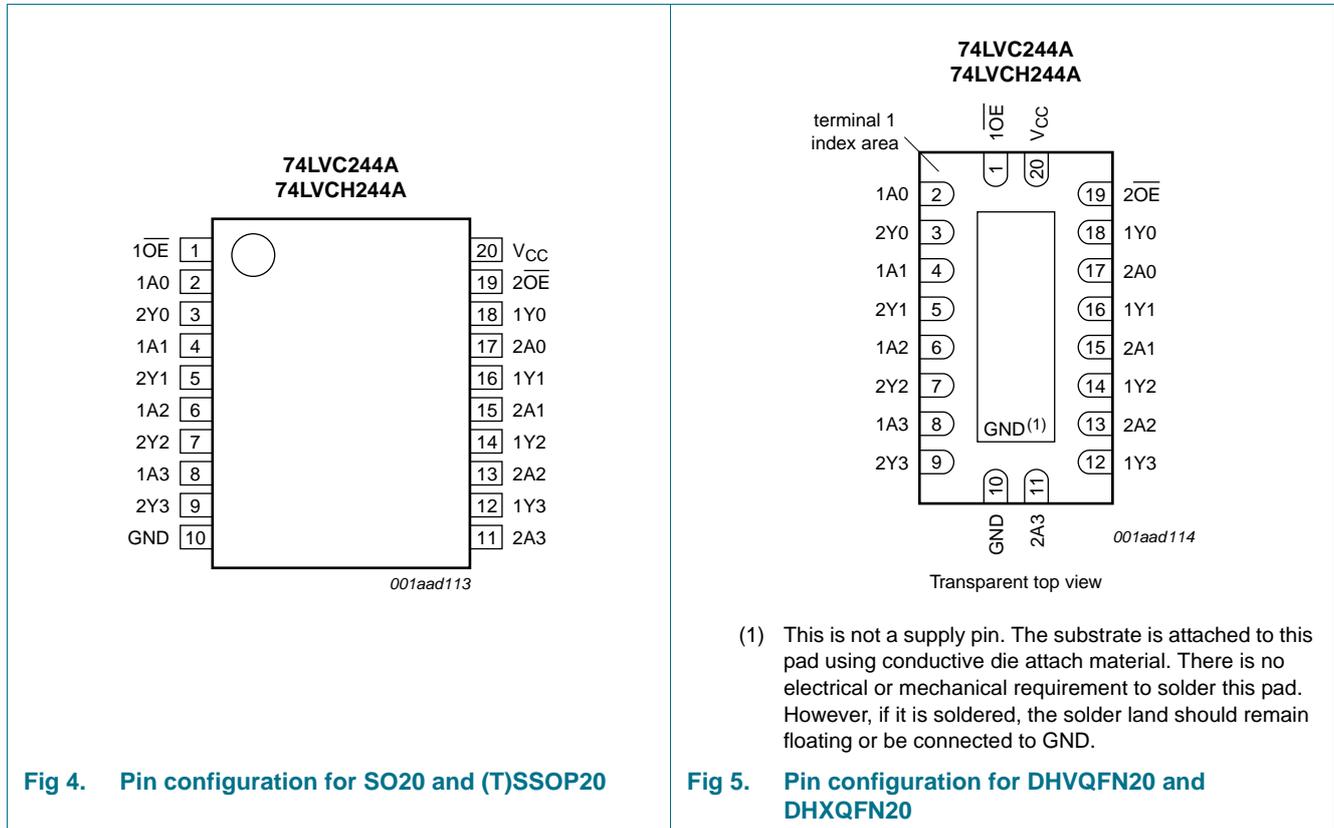


Fig 3. Functional diagram

## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
10 $\overline{OE}$ , 20 $\overline{OE}$	1, 19	output enable input (active low)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	data output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table [\[1\]](#)

Control	Input	Output
$\overline{\text{nOE}}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		<a href="#">[1]</a> -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$V_O$	output voltage	output HIGH or LOW	<a href="#">[2]</a> -0.5	$V_{CC} + 0.5$	V
		output 3-state	<a href="#">[2]</a> -0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	<a href="#">[3]</a> -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.

For (T)SSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN20 and DHXQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	3.6	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.2 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	0.65 × V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V		
I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V		

**Table 6. Static characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ <sup>[1]</sup>	Max	Min	Max		
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 3.6 \text{ V}$	[2]	-	$\pm 0.1$	$\pm 5$	-	$\pm 20$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = 5.5 \text{ V}$ or GND; $V_{CC} = 3.6 \text{ V}$	[2]	-	$\pm 0.1$	$\pm 5$	-	$\pm 20$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 5.5 \text{ V}$ ; $V_{CC} = 0.0 \text{ V}$		-	$\pm 0.1$	$\pm 10$	-	$\pm 20$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 3.6 \text{ V}$		-	0.1	10	-	40	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 0.6 \text{ V}$ ; $I_O = 0 \text{ A}$ ; $V_{CC} = 2.7 \text{ V}$ to $3.6 \text{ V}$		-	5	500	-	5000	$\mu\text{A}$
$C_I$	input capacitance			-	4.0	-	-	-	pF
$I_{BHL}$	bus hold LOW current	$V_{CC} = 1.65 \text{ V}$ ; $V_I = 0.58 \text{ V}$	[3][4]	10	-	-	10	-	$\mu\text{A}$
		$V_{CC} = 2.3 \text{ V}$ ; $V_I = 0.7 \text{ V}$		30	-	-	25	-	$\mu\text{A}$
		$V_{CC} = 3.0 \text{ V}$ ; $V_I = 0.8 \text{ V}$		75	-	-	60	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	$V_{CC} = 1.65 \text{ V}$ ; $V_I = 1.07 \text{ V}$	[3][4]	-10	-	-	-10	-	$\mu\text{A}$
		$V_{CC} = 2.3 \text{ V}$ ; $V_I = 1.7 \text{ V}$		-30	-	-	-25	-	$\mu\text{A}$
		$V_{CC} = 3.0 \text{ V}$ ; $V_I = 2.0 \text{ V}$		-75	-	-	-60	-	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	$V_{CC} = 1.95 \text{ V}$	[3][5]	200	-	-	200	-	$\mu\text{A}$
		$V_{CC} = 2.7 \text{ V}$		300	-	-	300	-	$\mu\text{A}$
		$V_{CC} = 3.6 \text{ V}$		500	-	-	500	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	$V_{CC} = 1.95 \text{ V}$	[3][5]	-200	-	-	-200	-	$\mu\text{A}$
		$V_{CC} = 2.7 \text{ V}$		-300	-	-	-300	-	$\mu\text{A}$
		$V_{CC} = 3.6 \text{ V}$		-500	-	-	-500	-	$\mu\text{A}$

[1] All typical values are measured at  $V_{CC} = 3.3 \text{ V}$  (unless stated otherwise) and  $T_{amb} = 25 \text{ }^\circ\text{C}$ .[2] The bus hold circuit is switched off when  $V_I > V_{CC}$  allowing 5.5 V on the input terminal.

[3] Valid for data inputs of bus hold parts only (74LVCH244A). Note that control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data input holds the input below the specified  $V_I$  level.

[5] The specified overdrive current at the data input forces the data input to the opposite input state.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nAn to nYn; see <a href="#">Figure 6</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	17.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	6.4	13.7	1.5	15.8	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	3.4	7.1	1.0	8.2	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.4	6.9	1.5	9.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.5	2.9	5.9	1.5	7.5	ns
t <sub>en</sub>	enable time	nOE to nYn; see <a href="#">Figure 7</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	24.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	7.0	17.3	1.5	20.0	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	3.9	9.5	1.5	11.0	ns
		V <sub>CC</sub> = 2.7 V	1.5	4.1	8.6	1.5	11.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.2	7.6	1.0	9.5	ns
t <sub>dis</sub>	disable time	nOE to nYn; see <a href="#">Figure 7</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	9.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.2	4.5	9.8	2.2	11.3	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	3.6	5.5	0.5	6.4	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.3	6.8	1.5	8.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.5	3.1	5.8	1.5	7.5	ns
t <sub>sk(o)</sub>	output skew time	<sup>[3]</sup>	-	-	1.0	-	1.5	ns
C <sub>PD</sub>	power dissipation capacitance	per input; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[4]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	6.4	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	9.6	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	12.5	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

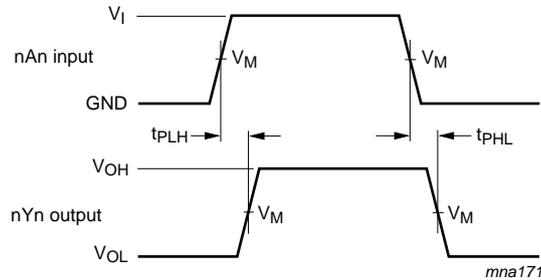
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

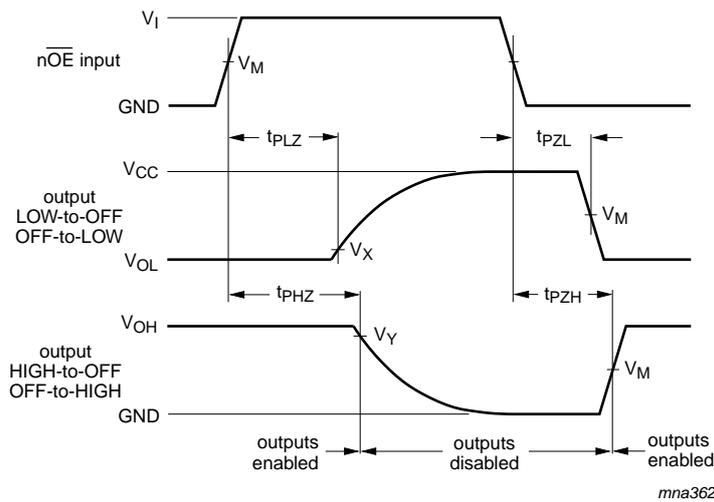
## 11. AC waveforms



Measurement points are given in [Table 8](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 6. The input (nAn) to output (nYn) propagation delays**



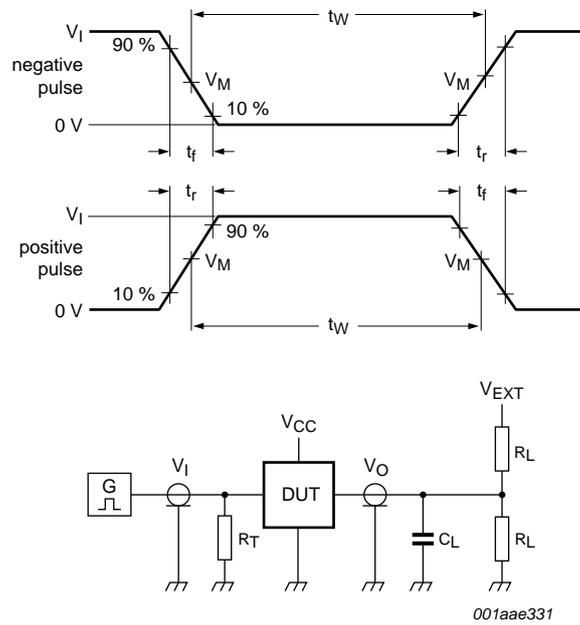
Measurement points are given in [Table 8](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7. 3-state enable and disable times.**

**Table 8. Measurement points**

Supply voltage	Input		Output		
	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
1.2 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 8. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

## 12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

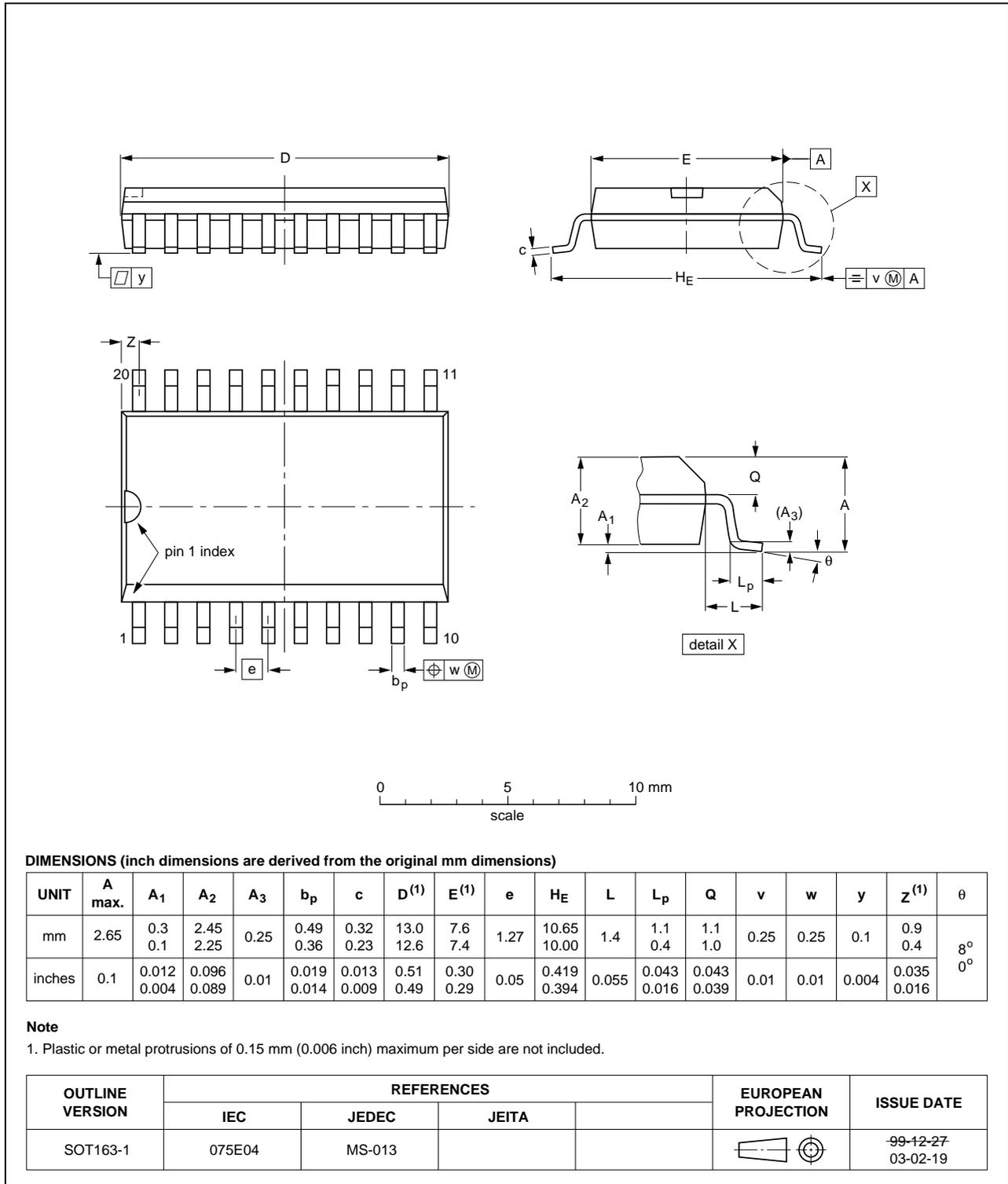


Fig 9. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

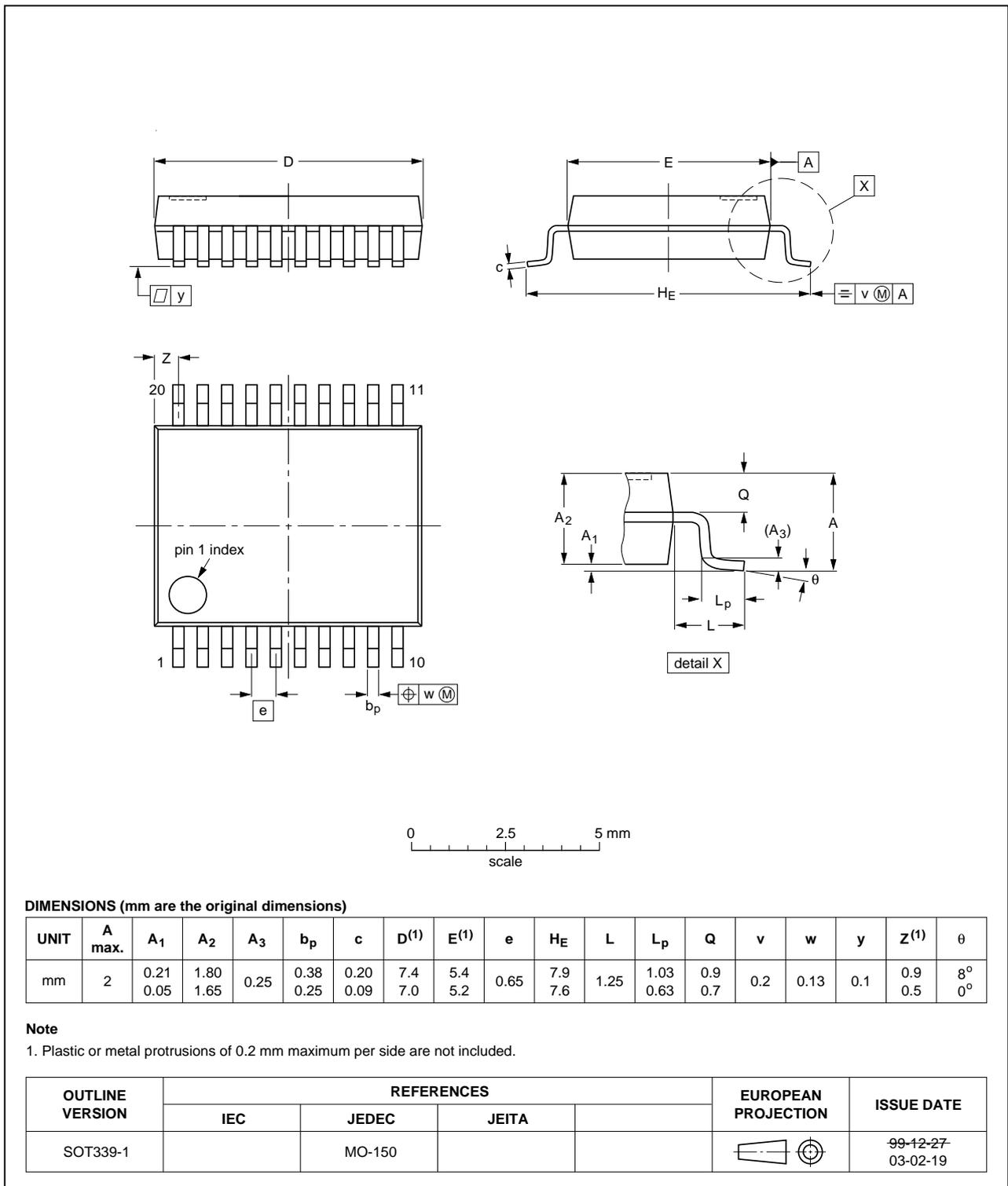


Fig 10. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

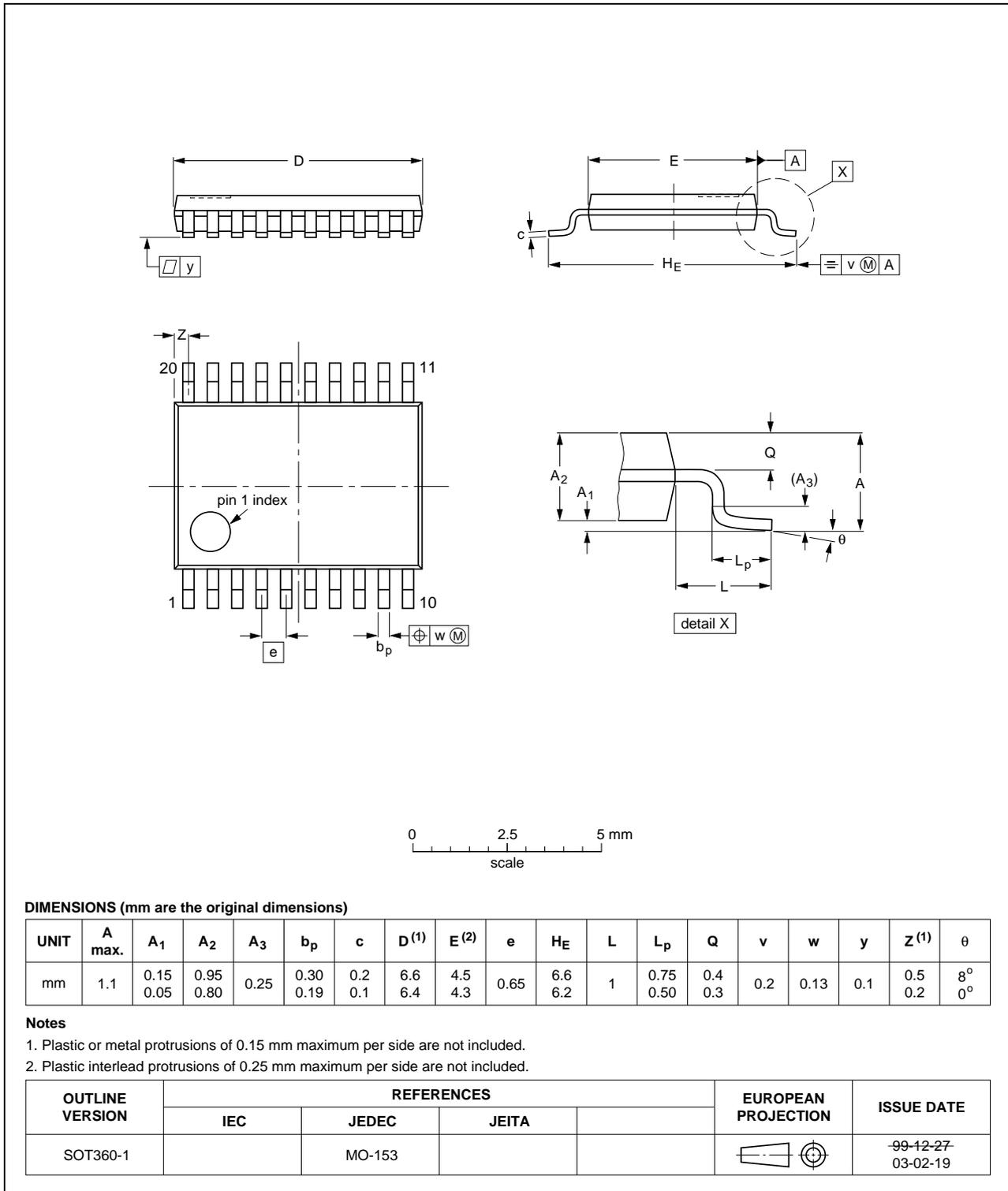


Fig 11. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

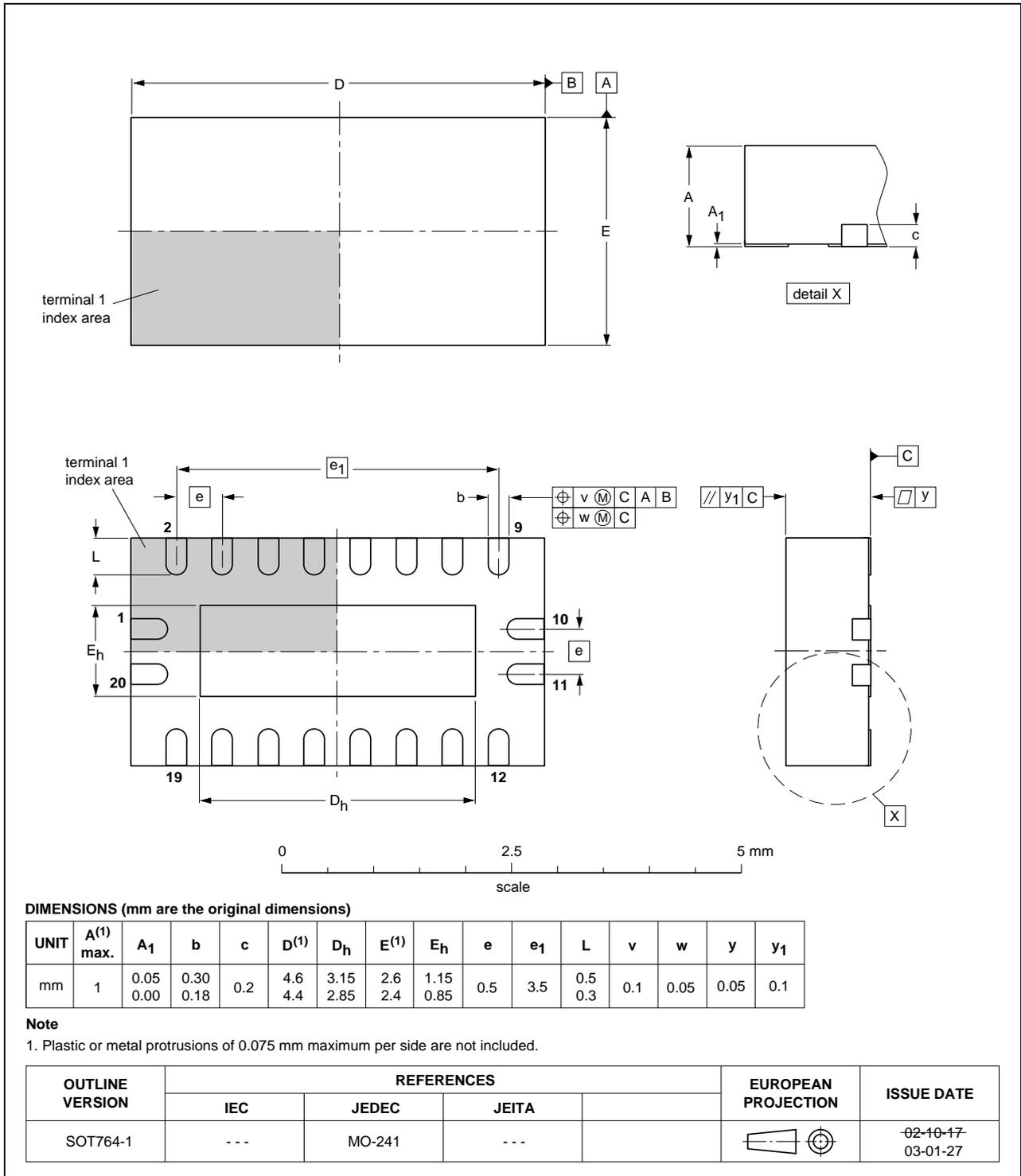


Fig 12. Package outline SOT764-1 (DHVQFN20)

DHXQFN20: plastic dual in-line compatible thermal enhanced extremely thin quad flat package; no leads; 20 terminals; body 4.5 x 2.5 x 0.5 mm

SOT1045-2

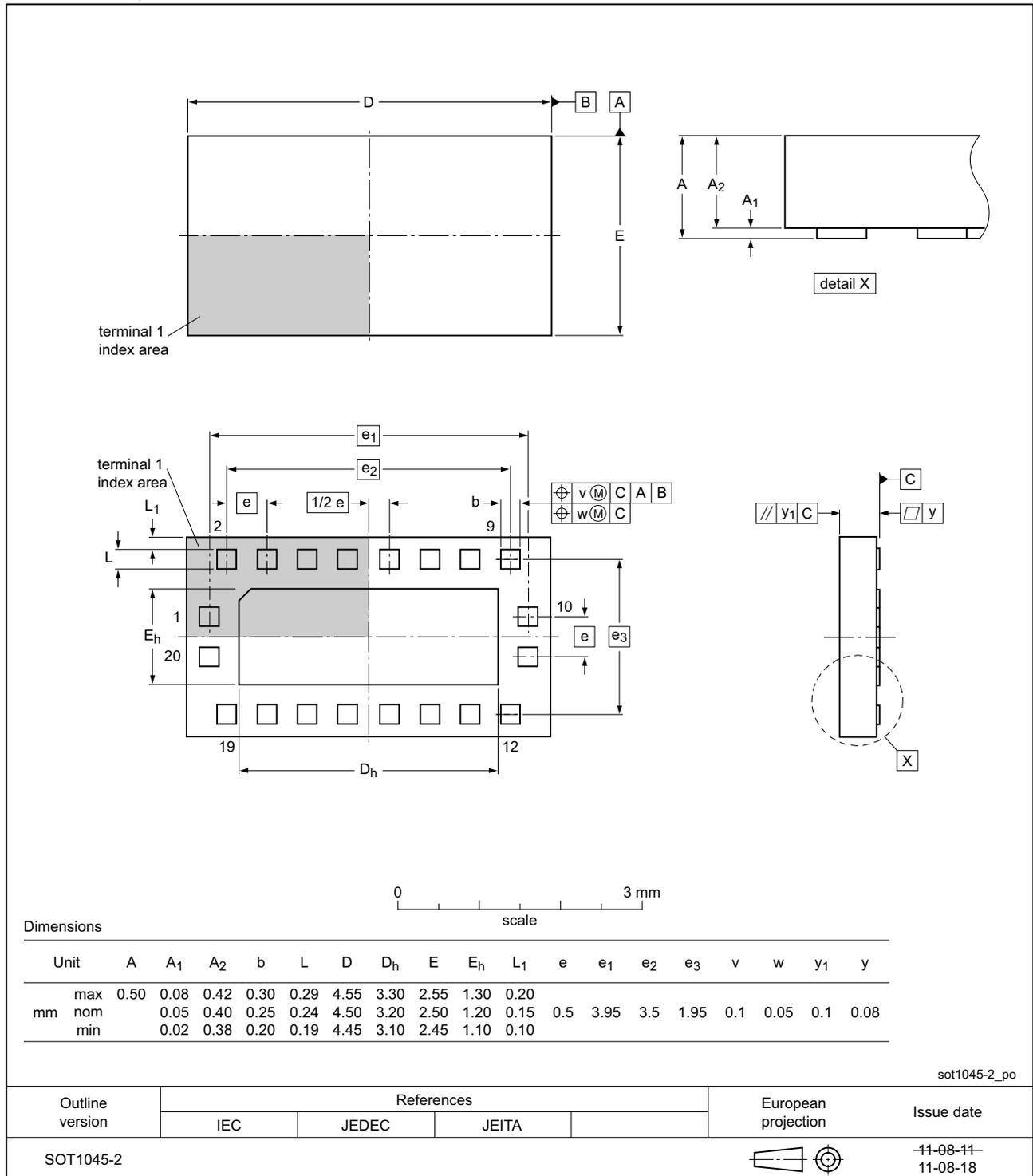


Fig 13. Package outline SOT1045-2 (DHXQFN20)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH244A v.8	20130626	Product data sheet	-	74LVC_LVCH244A v.7
Modifications:	<ul style="list-style-type: none"> <li>For type numbers 74LVC244ABX and 74LVCH244ABX DHXQFN20U (SOT1045-1) has changed to DHXQFN20 (SOT1045-2).</li> </ul>			
74LVC_LVCH244A v.7	20111122	Product data sheet	-	74LVC_LVCH244A v.6
Modifications:	<ul style="list-style-type: none"> <li>The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>, <a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a>, <a href="#">Table 8</a> and <a href="#">Table 9</a>: values added for lower voltage ranges.</li> </ul>			
74LVC_LVCH244A v.6	20090813	Product data sheet	-	74LVC_LVCH244A v.5
74LVC_LVCH244A v.5	20090709	Product data sheet	-	74LVC_LVCH244A v.4
74LVC_LVCH244A v.4	20031030	Product specification	-	74LVC_LVCH244A v.3
74LVC_LVCH244A v.3	20030520	Product specification	-	74LVC_H244A v.2
74LVC_H244A v.2	19980520	Product specification	-	74LVC244A_74LVCH244A v.1
74LVC244A_74LVCH244A v.1	19960906	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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