LM5085/-Q1 75-V Constant On-Time PFET Buck Switching Controller

1 Features

- LM5085-Q1 is an Automotive Grade Product that is AEC-Q100 Grade 1 Qualified (–40°C to 125°C Operating Junction Temperature)
- Wide 4.5-V to 75-V Input Voltage Range
- Adjustable Current Limit Using $R_{DS(ON)}$ or a Current Sense Resistor
- Programmable Switching Frequency to 1MHz
- No Loop Compensation Required
- Ultra-Fast Transient Response
- Nearly Constant Operating Frequency with Line and Load Variations
- Adjustable Output Voltage from 1.25 V
- Precision ±2% Feedback Reference
- Capable of 100% Duty Cycle Operation
- Internal Soft-start Timer
- Integrated High Voltage Bias Regulator
- Thermal Shutdown
- Package:
  - HVSSOP-8
  - VSSOP-8
  - WSON-8

2 Applications

- Automotive Infotainment
- Battery/Super Capacitor Chargers
- LED Drivers

3 Description

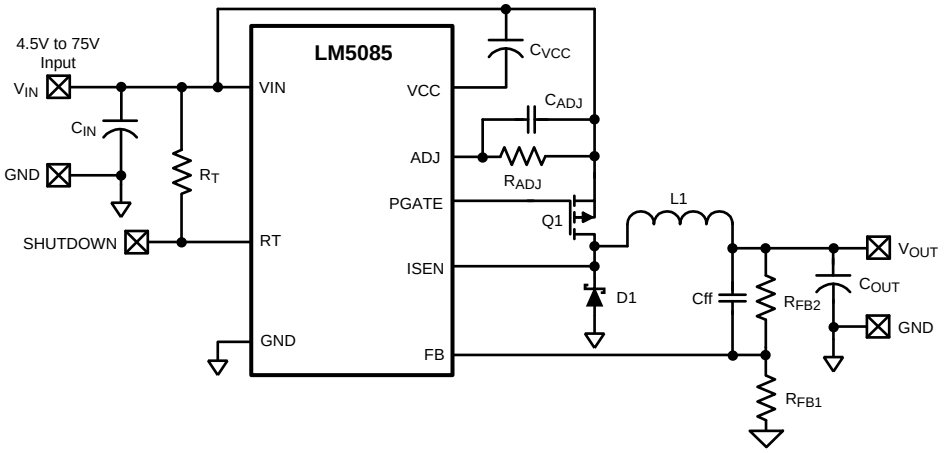
The LM5085 is a high efficiency PFET switching regulator controller that can be used to quickly and easily develop a small, efficient buck regulator for a wide range of applications. This high voltage controller contains a PFET gate driver and a high voltage bias regulator which operates over a wide 4.5-V to 75-V input range. The constant on-time regulation principle requires no loop compensation, simplifies circuit implementation, and results in ultrafast load transient response. The operating frequency remains nearly constant with line and load variations due to the inverse relationship between the input voltage and the on-time. The PFET architecture allows 100% duty cycle operation for a low dropout voltage. Either the $R_{DS(ON)}$ of the PFET or an external sense resistor can be used to sense current for over-current detection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5085	VSSOP (8)	3.00 mm x 3.00 mm
	HVSSOP (8)	
	WSON (8)	
LM5085-Q1	HVSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application, Basic Step Down Controller



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (October 2014) to Revision I — **Page**

- Moved the Storage temperature, T_{stg} to the *Absolute Maximum Ratings* ... 3
- Changed "*Handling Ratings*" to *ESD Ratings: LM5085* and *ESD Ratings: LM5085-Q1* ... 4
- Added text "*Figure 24 shows the required placement of this Schottky diode...*" and Figure 24 to section *VCC Regulator*. 14

Changes from Revision G (March 2013) to Revision H — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision F (March 2013) to Revision G — **Page**

- Changed layout of National Data Sheet to TI format ... 23

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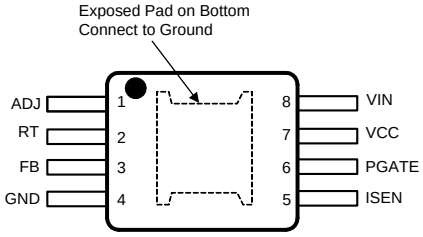
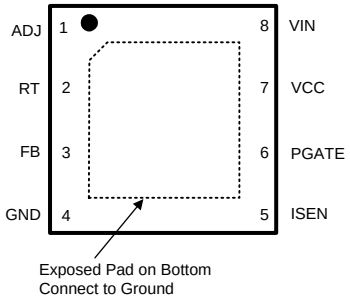
5 Pin Configuration and Functions

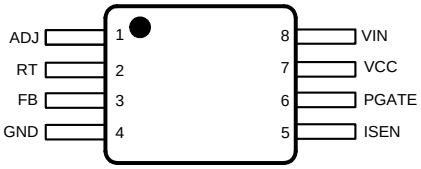
8-Pins HVSSOP Package Top View



8-Pins WSON Package Top View



8-Pins VSSOP Package Top View



Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NAME	NO.			
ADJ	1	I	Current Limit Adjust	The current limit threshold is set by an external resistor from VIN to ADJ in conjunction with the external sense resistor or the PFET's $R_{DS(ON)}$.
RT	2	I	On-Time Control and Shutdown	An external resistor from VIN to RT sets the buck switch on-time and switching frequency. Grounding this pin shuts down the controller.
FB	3	I	Voltage Feedback From the Regulated Output	Input to the regulation and over-voltage comparators. The regulation level is 1.25V.
GND	4	-	Circuit Ground	Ground reference for all internal circuitry
ISEN	5	I	Current Sense Input for Current limit Detection.	Connect to the PFET drain when using $R_{DS(ON)}$ current sense. Connect to the PFET source and the sense resistor when using a current sense resistor.
PGATE	6	O	Gate Driver Output	Connect to the gate of the external PFET.
VCC	7	O	Output of the gate driver bias regulator	Output of the negative voltage regulator (relative to VIN) that biases the PFET gate driver. A low ESR capacitor is required from VIN to VCC, located as close as possible to the pins.
VIN	8	I	Input Supply Voltage	The operating input range is from 4.5V to 75V. A low ESR bypass capacitor must be located as close as possible to the VIN and GND pins.
EP		-	Exposed Pad	Exposed pad on the underside of the package (HVSSOP and WSON only). This pad is to be soldered to the PC board ground plane to aid in heat dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

	MIN	MAX	UNIT
VIN to GND	–0.3	76	V
ISEN to GND	–3	V_{IN} + 0.3	V
ADJ to GND	–0.3	V_{IN} + 0.3	V
RT, FB to GND	–0.3	7	V
VIN to VCC, VIN to PGATE	–0.3	10	V
Storage temperature, T_{stg}	–65	150	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the *Electrical Characteristics* .

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

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6.2 ESD Ratings: LM5085

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LM5085-Q1

				MIN	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)			±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, and 8)		±750	
			Other pins		±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

	MIN	MAX	UNIT
VIN Voltage	4.5	75	V
Junction Temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		LM5085		LM5085, LM5085-Q1	UNIT
		DGK	NGQ	DGN	
		8 PINS	8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	153	44.8	54.1	°C/W
θ_{JC}(top)	Junction-to-case (top) thermal resistance	52.5	39.4	49.1	
θ_{JB}	Junction-to-board thermal resistance	71.9	11.6	26.7	
ψ_{JT}	Junction-to-top characterization parameter	4.6	0.3	1.3	
ψ_{JB}	Junction-to-board characterization parameter	70.8	11.6	26.5	
θ_{JC}(bot)	Junction-to-case (bottom) thermal resistance	29	5.0	3.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. Unless otherwise stated the following conditions apply: V_{IN} = 48 V, R_T = 100kΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN PIN						
I_{IN}	Operating Current	Non-Switching, FB = 1.4 V (1)		1.3	1.8	mA
I_Q	Shutdown Current	RT = 0 V (1)		200	345	µA
VCC REGULATOR(2)						
$V_{CC(reg)}$	VIN - VCC	Vin = 9 V, FB = 1.4 V, ICC = 0 mA	6.9	7.7	8.5	V
		Vin = 9 V, FB = 1.4 V, ICC = 20 mA		7.7		V
		Vin = 75 V, FB = 1.4 V, ICC = 0 mA		7.7		V
$UVLO_{Vcc}$	VCC Under-Voltage Lock-out Threshold	V_{CC} Increasing		3.8		V
	$UVLO_{Vcc}$ Hysteresis	V_{CC} Decreasing		260		mV
$V_{CC(CL)}$	VCC Current Limit	FB = 1.4 V	20	40		mA

(1) Operating current and shutdown current do not include the current in the R_T resistor.
(2) V_{CC} provides self bias for the internal gate drive.

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Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. Unless otherwise stated the following conditions apply: V_{IN} = 48 V, R_T = 100kΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGATE PIN						
$V_{PGATE(HI)}$	PGATE High Voltage	PGATE Pin = Open	V_{IN} -0.1	V_{IN}		V
$V_{PGATE(LO)}$	PGATE Low Voltage	PGATE Pin = Open		V_{CC}	V_{CC}+0.1	V
$V_{PGATE(HI)4.5}$	PGATE High Voltage at Vin = 4.5V	PGATE Pin = Open	V_{IN} -0.1	V_{IN}		V
$V_{PGATE(LO)4.5}$	PGATE Low Voltage at Vin = 4.5V	PGATE Pin = Open		V_{CC}	V_{CC}+0.1	V
I_{PGATE}	Driver Output Source Current	VIN = 12 V, PGATE = VIN - 3.5 V		1.75		A
	Driver Output Sink Current	VIN = 12 V, PGATE = VIN - 3.5 V		1.5		A
R_{PGATE}	Driver Output Resistance	Source Current = 500 mA		2.3		Ω
		Sink Current = 500 mA		2.3		Ω
CURRENT LIMIT DETECTION						
I_{ADJ}	ADJUST Pin Current Source	V_{ADJ} = 46.5 V	32	40	48	µA
$V_{CL\ OFFSET}$	Current Limit Comparator Offset	V_{ADJ} = 46.5 V, V_{ADJ} - V_{ISEN}	-9	0	9	mV
RT PIN						
RT_{SD}	Shutdown Threshold	RT Pin Voltage Rising		0.73		V
RT_{HYS}	Shutdown Threshold Hysteresis			50		mV
ON-TIME						
t_{ON-1}	On-Time	VIN = 4.5 V, R_T = 100kΩ	3.5	5	7.15	µs
t_{ON-2}		VIN = 48 V, R_T = 100kΩ	276	360	435	ns
t_{ON-3}		VIN = 75 V, R_T = 100kΩ	177	235	285	ns
t_{ON-4}	Minimum On-Time in Current Limit (3)	VIN = 48 V, 25 mV Overdrive at ISEN	55	140	235	ns
OFF-TIME						
$t_{OFF(CL1)}$	Off-Time (Current Limit) (3)	VIN = 12 V, V_{FB} = 0 V	5.35	7.9	10.84	µs
$t_{OFF(CL2)}$		VIN = 12 V, V_{FB} = 1 V	1.42	1.9	3.03	µs
$t_{OFF(CL3)}$		VIN = 48 V, V_{FB} = 0 V	16	24	32.4	µs
$t_{OFF(CL4)}$		VIN = 48 V, V_{FB} = 1 V	3.89	5.7	8.67	µs
REGULATION AND OVERVOLTAGE COMPARATORS (FB PIN)						
V_{REF}	FB Regulation Threshold		1.225	1.25	1.275	V
V_{OV}	FB Over-Voltage Threshold	Measured with Respect to V_{REF}		350		mV
I_{FB}	FB Bias Current			10		nA
SOFT-START FUNCTION						
t_{SS}	Soft-Start Time		1.4	2.5	4.3	ms
THERMAL SHUTDOWN						
T_{SD}	Junction Shutdown Temperature	Junction Temperature Rising		170		°C
T_{HYS}	Junction Shutdown Hysteresis			20		°C

(3) The tolerance of the minimum on-time (t_{ON}-4) and the current limit off-times ($t_{OFF(CL1)}$ through ($t_{OFF(CL4)}$) track each other over process and temperature variations. A device which has an on-time at the high end of the range will have an off-time that is at the high end of its range.

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6.7 Typical Characteristics

Unless otherwise specified the following conditions apply: T_J = 25°C, V_{IN} = 48V.

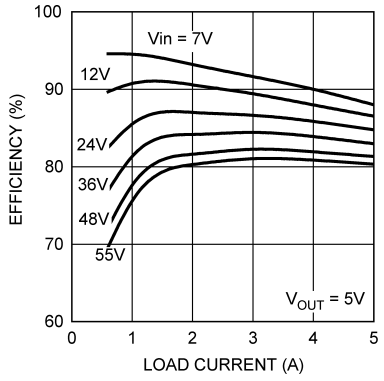

Figure 1. Efficiency (Circuit of Figure 25)

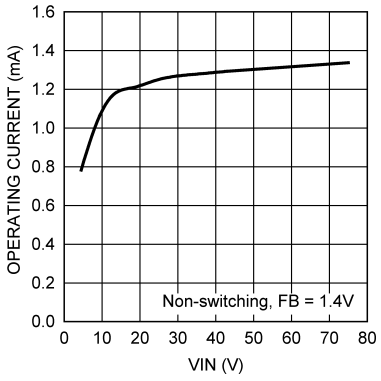

Figure 2. Input Operating Current vs. V_{IN}

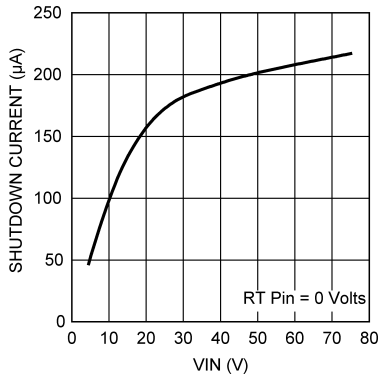

Figure 3. Shutdown Current vs. V_{IN}

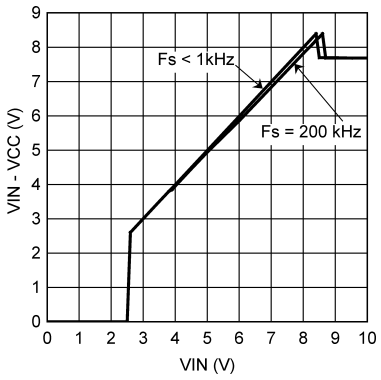

Figure 4. V_{CC} vs. V_{IN}

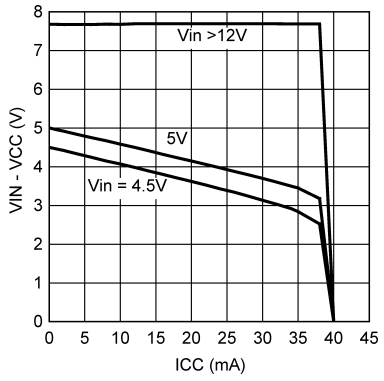

Figure 5. V_{CC} vs. I_{CC}

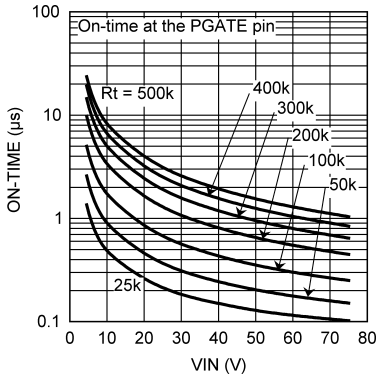

Figure 6. On-Time vs. R_T and V_{IN}

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Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: T_J = 25°C, V_{IN} = 48V.

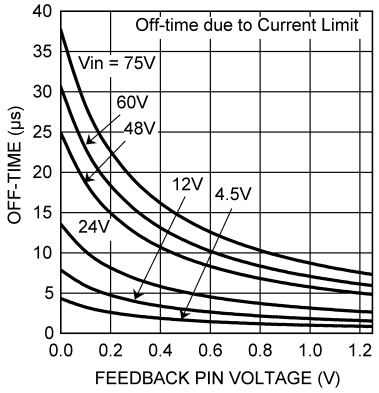

Figure 7. Off-Time vs. V_{IN} and V_{FB}

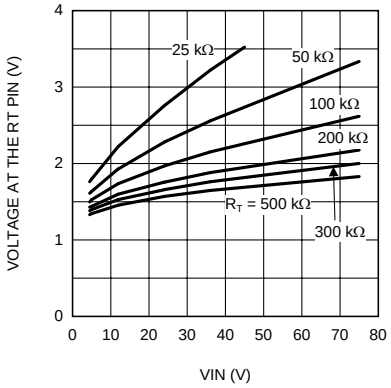

Figure 8. Voltage at the RT Pin

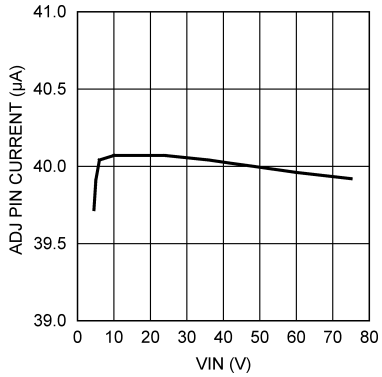

Figure 9. ADJ Pin Current vs. V_{IN}

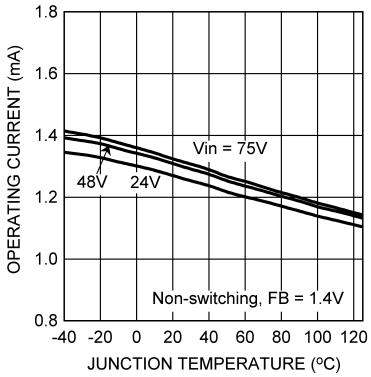

Figure 10. Input Operating Current vs. Temperature

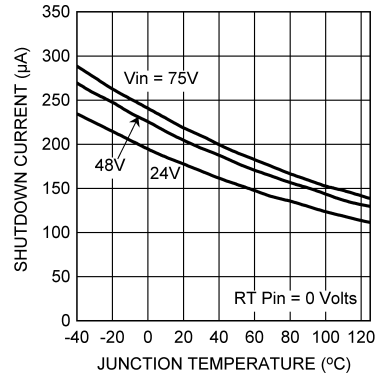

Figure 11. Shutdown Current vs. Temperature

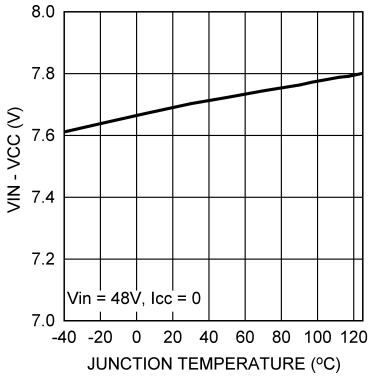

Figure 12. VCC vs. Temperature

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Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: T_J = 25°C, V_{IN} = 48V.

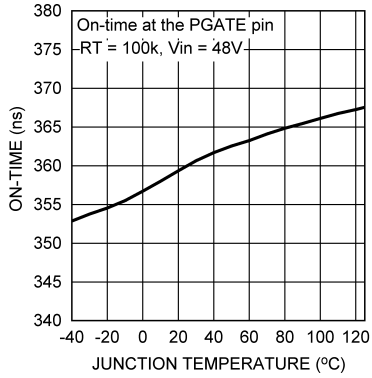

Figure 13. On-Time vs. Temperature

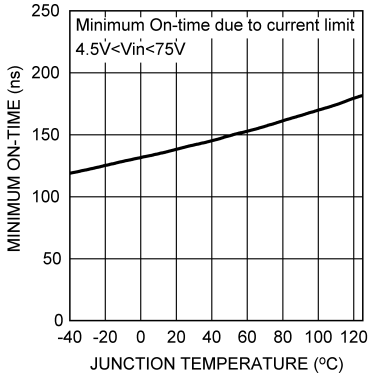

Figure 14. Minimum On-Time vs. Temperature

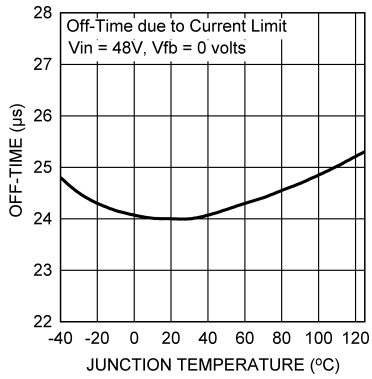

Figure 15. Off-Time vs. Temperature

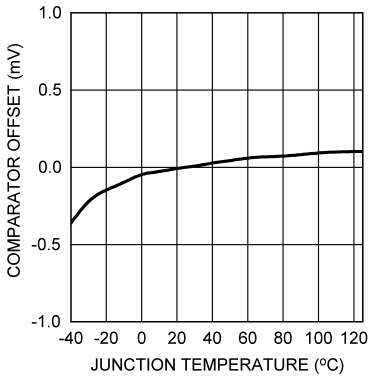

Figure 16. Current Limit Comparator Offset vs. Temperature

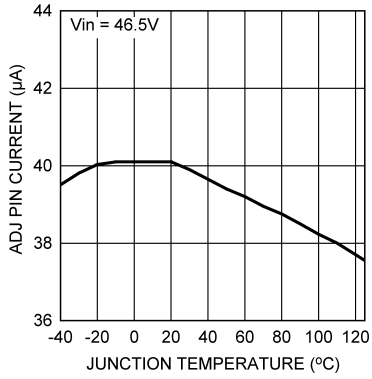

Figure 17. ADJ Pin Current vs. Temperature

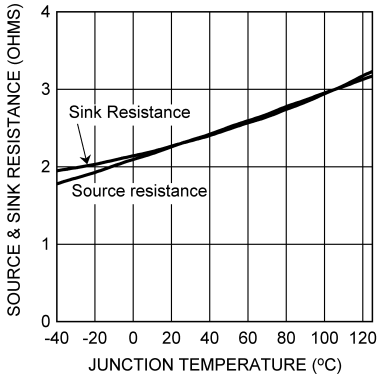

Figure 18. PGATE Driver Output Resistance vs. Temperature

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Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: T_J = 25°C, V_{IN} = 48V.

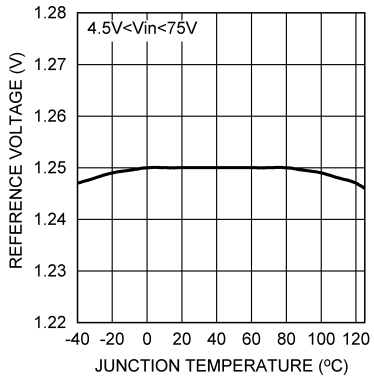


Figure 19. Feedback Reference Voltage vs. Temperature

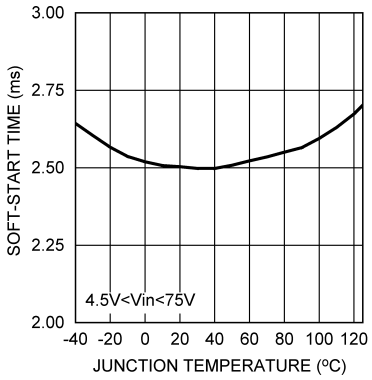


Figure 20. Soft-Start Time vs. Temperature

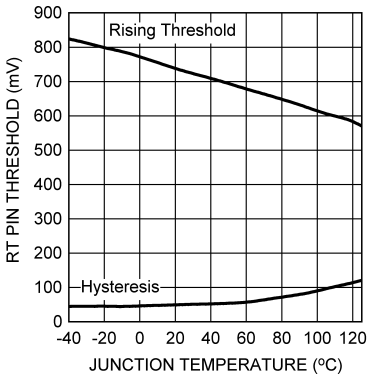


Figure 21. RT Pin Shutdown Threshold vs. Temperature

7 Detailed Description

7.1 Overview

The LM5085 is a PFET buck (step-down) DC-DC controller using the constant on-time (COT) control principle. The input operating voltage range of the LM5085 is 4.5V to 75V. The use of a PFET in a buck regulator greatly simplifies the gate drive requirements and allows for 100% duty cycle operation to extend the regulation range when operating at low input voltage. However, PFET transistors typically have higher on-resistance and gate charge when compared to similarly rated NFET transistors. Consideration of available PFETs, input voltage range, gate drive capability of the LM5085, and thermal resistances indicate an upper limit of 10A for the load current for LM5085 applications. Constant on-time control is implemented using an on-time one-shot that is triggered by the feedback signal. During the off-time, when the PFET (Q1) is off, the load current is supplied by the inductor and the output capacitor. As the output voltage falls, the voltage at the feedback comparator input (FB) falls below the regulation threshold. When this occurs Q1 is turned on for the one-shot period which is determined by the input voltage (V_{IN}) and the R_T resistor. During the on-time the increasing inductor current increases the voltage at FB above the feedback comparator threshold. For a buck regulator the basic relationship between the on-time, off-time, input voltage and output voltage is:

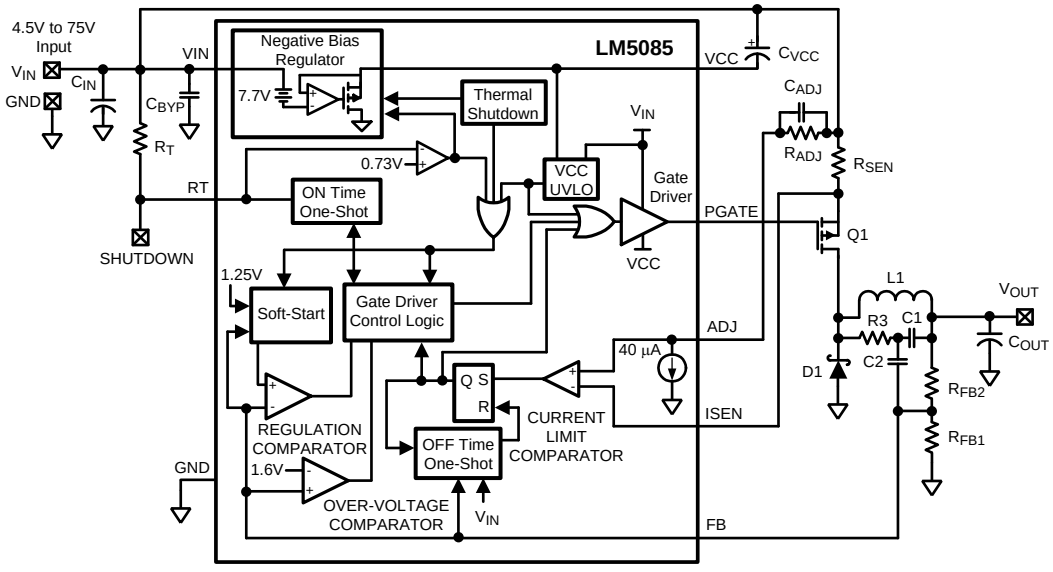
$$\text{Duty Cycle} = \frac{V_{OUT}}{V_{IN}} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times F_S \tag{1}$$

where Fs is the switching frequency. Equation 1 is valid only in continuous conduction mode (inductor current does not reach zero). Since the LM5085 controls the on-time inversely proportional to V_{IN}, the switching frequency remains relatively constant as V_{IN} is varied. If the input voltage falls to a level that is equal to or less than the regulated output voltage Q1 is held on continuously (100% duty cycle) and V_{OUT} is approximately equal to V_{IN}.

The COT control scheme, with the feedback signal applied to a comparator rather than an error amplifier, requires no loop compensation, resulting in very fast load transient response.

The LM5085 is available in both an 8-pin HVSSOP package and an 8-pin WSON package with an exposed pad to aid in heat dissipation. An 8-pin VSSOP package without an exposed pad is also available.

7.2 Functional Block Diagram



Sense resistor method shown for current limit detection.
Minimum output ripple configuration shown.

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7.3 Feature Description

7.3.1 Regulation Control Circuit

The LM5085 buck DC-DC controller employs a control scheme based on a comparator and a one-shot on-timer, with the output voltage feedback compared to an internal reference voltage (1.25V). When the FB pin voltage falls below the feedback reference, Q1 is switched on for a time period determined by the input voltage and a programming resistor (R_T). Following the on-time Q1 remains off until the FB voltage falls below the reference. Q1 is then switched on for another on-time period. The output voltage is set by the feedback resistors (R_{FB1}, R_{FB2} in the Block Diagram). The regulated output voltage is calculated as follows:

$$V_{OUT} = 1.25V \times (R_{FB2} + R_{FB1}) / R_{FB1} \quad (2)$$

The feedback voltage supplied to the FB pin is applied to a comparator rather than a linear amplifier. For proper operation sufficient ripple amplitude is necessary at the FB pin to switch the comparator at regular intervals with minimum delay and noise susceptibility. This ripple is normally obtained from the output voltage ripple attenuated through the feedback resistors. The output voltage ripple is a result of the inductor's ripple current passing through the output capacitor's ESR, or through a resistor in series with the output capacitor. Multiple methods are available to ensure sufficient ripple is supplied to the FB pin, and three different configurations are discussed in the *Typical Application* section.

When in regulation, the LM5085 operates in continuous conduction mode at medium to heavy load currents and discontinuous conduction mode at light load currents. In continuous conduction mode the inductor's current is always greater than zero, and the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. In discontinuous conduction mode, where the inductor's current reaches zero during the off-time, the operating frequency is lower than in continuous conduction mode and varies with load current. Conversion efficiency is maintained at light loads since the switching losses are reduced with the reduction in load and frequency.

If the voltage at the FB pin exceeds 1.6V due to a transient overshoot or excessive ripple at V_{OUT} the internal over-voltage comparator immediately switches off Q1. The next on-time period starts when the voltage at FB falls below the feedback reference voltage.

7.3.2 On-Time Timer

The on-time of the PFET gate drive output (PGATE pin) is determined by the resistor (R_T) and the input voltage (V_{IN}), and is calculated from:

$$t_{ON} = \frac{1.45 \times 10^{-7} \times (R_T + 1.4)}{(V_{IN} - 1.56V + R_T/3167)} + 50\ ns \quad (3)$$

where R_T is in kΩ.

The minimum on-time, which occurs at maximum V_{IN}, should not be set less than 150ns (see *Current Limiting* section). The buck regulator effective on-time, measured at the SW node (junction of Q1, L1, and D1) is typically longer than that calculated in Equation 3 due to the asymmetric delay of the PFET. The on-time difference caused by the PFET switching delay can be estimated as the difference of the turn-off and turn-on delays listed in the PFET data sheet. Measuring the difference between the on-time at the PGATE pin versus the SW node in the actual application circuit is also recommended.

In continuous conduction mode, the inverse relationship of t_{ON} with V_{IN} results in a nearly constant switching frequency as V_{IN} is varied. The operating frequency can be calculated from:

$$F_S = \frac{V_{OUT} \times (V_{IN} - 1.56V + R_T/3167)}{V_{IN} \times [(1.45 \times 10^{-7} \times (R_T + 1.4)) + (t_D \times (V_{IN} - 1.56V + R_T/3167))]} \quad (4)$$

where R_T is in kΩ, and t_D is equal to 50ns plus the PFET's delay difference. To set a specific continuous conduction mode switching frequency (F_S), the R_T resistor is determined from the following:

$$R_T = \frac{V_{OUT} \times (V_{IN} - 1.56V)}{1.45 \times 10^{-7} \times V_{IN} \times F_S} - \frac{t_D \times (V_{IN} - 1.56V)}{1.45 \times 10^{-7}} - 1.4 \quad (5)$$

where R_T is in kΩ. A simplified version of Equation 5 at V_{IN} = 12V, and t_D = 100ns, is:

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Feature Description (continued)

$$R_T = \frac{V_{OUT} \times 6 \times 10^6}{F_S} - 8.6 \quad (6)$$

For V_{IN} = 48V and t_D = 100ns, the simplified equation is:

$$R_T = \frac{V_{OUT} \times 6.67 \times 10^6}{F_S} - 33.4 \quad (7)$$

7.3.3 Shutdown

The LM5085 can be shutdown by grounding the RT pin (see Figure 22). In this mode the PFET is held off, and the VCC regulator is disabled. The internal operating current is reduced to the value shown in the graph "Shutdown current vs. VIN". The shutdown threshold at the RT pin is ≅0.73V, with ≅50mV of hysteresis. Releasing the pin enables normal operation. The RT pin must not be forced high during normal operation.

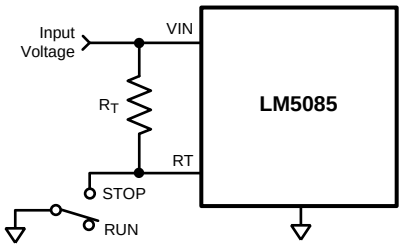

Figure 22. Shutdown Implementation

7.3.4 Current Limiting

The LM5085 current limiting operates by sensing the voltage across either the $R_{DS(ON)}$ of Q1, or a sense resistor, during the on-time and comparing it to the voltage across the resistor R_{ADJ} (see Figure 23). The current limit function is much more accurate and stable over temperature when a sense resistor is used. The $R_{DS(ON)}$ of a MOSFET has a wide process variation and a large temperature coefficient.

If the voltage across $R_{DS(ON)}$ of Q1, or the sense resistor, is greater than the voltage across R_{ADJ}, the current limit comparator switches to turn off Q1. Current sensing is disabled for a blanking time of ≅100ns at the beginning of the on-time to prevent false triggering of the current limit comparator due to leading edge current spikes. Because of the blanking time and the turn-on and turn-off delays created by the PFET, the on-time at the PGATE pin should not be set less than 150ns. An on-time shorter than that may prevent the current limit detection circuit from properly detecting an over-current condition. The duration of the subsequent forced off-time is a function of the input voltage and the voltage at the FB pin, as shown in the graph "Off-time vs. V_{IN} and V_{FB}". The longer-than-normal forced off-time allows the inductor current to decrease to a low level before the next on-time. This cycle-by-cycle monitoring, followed by a forced off-time, provides effective protection from output load faults over a wide range of operating conditions.

The voltage across the R_{ADJ} resistor is set by an internal 40µA current sink at the ADJ pin. When using Q1's $R_{DS(ON)}$ for sensing, the current at which the current limit comparator switches is calculated from:

$$I_{CL} = 40\mu A \times R_{ADJ}/R_{DS(ON)} \quad (8)$$

When using a sense resistor (R_{SEN}) the threshold of the current limit comparator is calculated from:

$$I_{CL} = 40\mu A \times R_{ADJ}/R_{SEN} \quad (9)$$

When using Equation 8 or Equation 9, the tolerances for the ADJ pin current sink and the offset of the current limit comparator should be included to ensure the resulting minimum current limit is not less than the required maximum switch current. Simultaneously increasing the values of R_{ADJ} and R_{SEN} decreases the effects of the current limit comparator offset, but at the expense of higher power dissipation. When using a sense resistor, the R_{SEN} resistor value should be chosen within the practical limitations of power dissipation and physical size. For example, for a 10A current limit, setting R_{SEN} = 0.005Ω results in a power dissipation as high as 0.5W. Current sense connections to the R_{SEN} resistor, or to Q1, must be Kelvin connections to ensure accuracy.

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Feature Description (continued)

The C_{ADJ} capacitor filters noise from the ADJ pin, and helps prevent unintended switching of the current limit comparator due to input voltage transients. The recommended value for C_{ADJ} is 1000pF.

7.3.5 Current Limit Off-Time

When the current through Q1 exceeds the current limit threshold, the LM5085 forces an off-time longer than the normal off-time defined by Equation 1. See the graph "Off-Time vs. V_{IN} and V_{FB}", or calculate the current limit off-time from the following equation:

$$t_{OFF(CL)} = \frac{4.1 \times 10^{-6} \times ((V_{IN}/31) + 0.15)}{(V_{FB} \times 0.93) + 0.28V} \quad (10)$$

where V_{IN} is the input voltage, and V_{FB} is the voltage at the FB pin at the time current limit was detected. This feature is necessary to allow the inductor current to decrease sufficiently to offset the current increase which occurred during the on-time. During the on-time, the inductor current increases an amount equal to:

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L} \quad (11)$$

During the off-time the inductor current decreases due to the reverse voltage applied across the inductor by the output voltage, the freewheeling diode's forward voltage (V_{FD}), and the voltage drop due to the inductor's series resistance (V_{ESR}). The current decrease is equal to:

$$\Delta I = \frac{(V_{OUT} + V_{FD} + V_{ESR}) \times t_{OFF}}{L} \quad (12)$$

The on-time in Equation 11 is shorter than the normal on-time since the PFET is shut off when the current limit threshold is crossed. If the off-time is not long enough, such that the current decrease (Equation 12) is less than the current increase (Equation 11), the current levels are higher at the start of the next on-time. This results in a further decrease in on-time, since the current limit threshold is crossed sooner. A balance is reached when the current changes in Equation 11 and Equation 12 are equal. The worst case situation is that of a direct short circuit at the output terminals, where V_{OUT} = 0V, as that results in the largest current increase during the on-time, and the smallest decrease during the off-time. The sum of the diode's forward voltage and the inductor's ESR voltage must be sufficient to ensure current runaway does not occur. Using Equation 11 and Equation 12, this requirement can be stated as:

$$V_{FD} + V_{ESR} \geq \frac{V_{IN} \times t_{ON}}{t_{OFF}} \quad (13)$$

For t_{ON} in Equation 13, use the minimum on-time at the SW node. To determine this time period add the "Minimum On-Time in Current Limit" specified in the Electrical Characteristics (t_{ON}-4) to the difference of the turn-off and turn-on delays of the PFET. For t_{OFF} use the value in the graph "Off-Time vs. V_{IN} and V_{FB}", or use Equation 10, where V_{FB} is equal to zero volts. When using the minimum or maximum limits of those specifications to determine worst case situations, the tolerance of the minimum on-time (t_{ON}-4) and the current limit off-times ($t_{OFF(CL1)}$ through $t_{OFF(CL4)}$) track each other over the process and temperature variations. A device which has an on-time at the high end of the range will have an off-time that is at the high end of its range.

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Feature Description (continued)

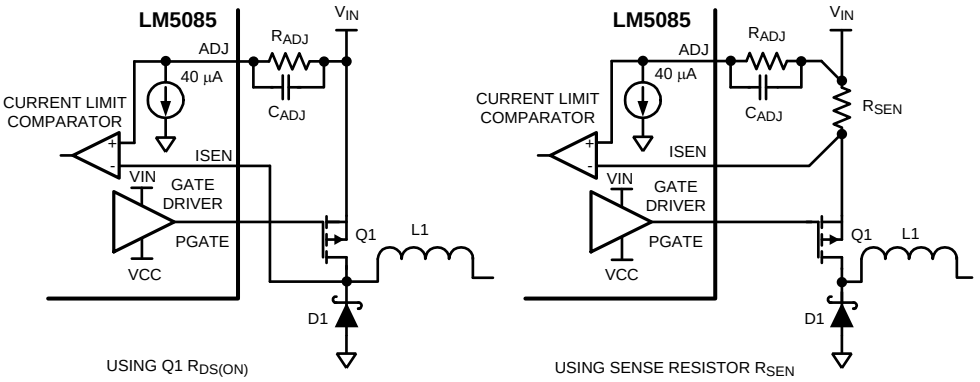

Figure 23. Current Limit Sensing

7.3.6 VCC Regulator

The VCC regulator provides a regulated voltage between the VIN and the VCC pins to provide the bias and gate current for the PFET gate driver. The 0.47µF capacitor at the VCC pin must be a low ESR capacitor, preferably ceramic as it provides the high surge current for the PFET's gate at each turn-on. The capacitor must be located as close as possible to the VIN and VCC pins to minimize inductance in the PC board traces.

Referring to Figure 4 "VCC vs. VIN", the voltage across the VCC regulator (VIN – VCC) is equal to VIN until VIN reaches approximately 8.5V. At higher values of VIN, the voltage at the VCC pin is regulated at approximately 7.7V below VIN. If VIN drops below about 8V due to voltage transients, the VCC pin can be pulled down below GND. To prevent the negative VCC voltage from disturbing the internal circuit and causing abnormal operation, Figure 24 shows the required placement of this Schottky diode between the VCC pin and GND pin. The Schottky diode should be placed as close as possible to the VCC pin. The VCC regulator has a maximum current capability of at least 20mA. The regulator is disabled when the LM5085 is shutdown using the RT pin, or when the thermal shutdown is activated.

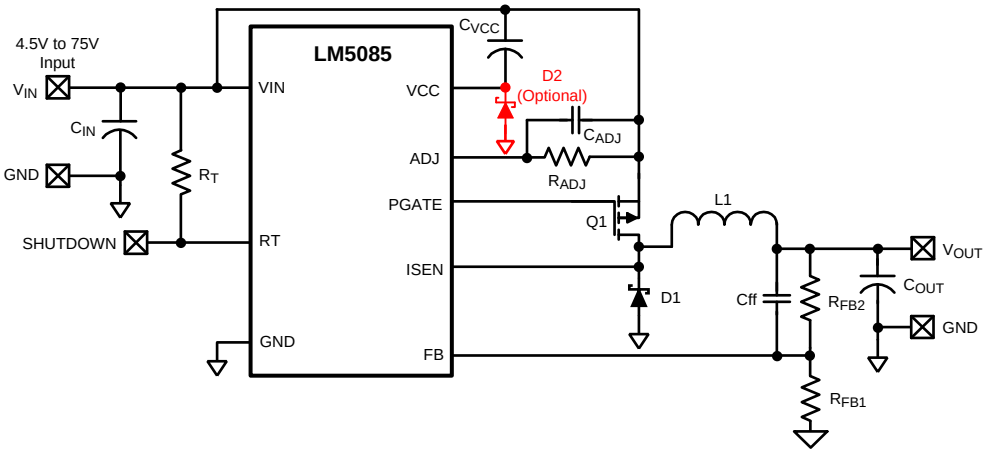

Figure 24. Schottky Diode at VCC Pin During VIN Negative Transients (VIN < 8 V)

7.3.7 PGATE Driver Output

The PGATE pin output swings between V_{IN} (Q1 off) and the VCC pin voltage (Q1 on). The rise and fall times depend on the PFET gate capacitance and the source and sink currents provided by the internal gate driver. See the *Electrical Characteristics* for the current capability of the driver.

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Feature Description (continued)

7.3.8 P-Channel MOSFET Selection

The PFET must be rated for the maximum input voltage, with some margin above that to allow for transients and ringing which can occur on the supply line and the switching node. The gate-to-source voltage (V_{GS}) normally provided to the PFET is 7.7V for VIN greater than 8.5V. However, if the circuit is to be operated at lower values of VIN, the selected PFET must be able to fully turn-on with a V_{GS} voltage equal to VIN. The minimum input operating voltage for the LM5085 is 4.5V.

Similar to NFETs, the case or exposed thermal pad for a PFET is electrically connected to the drain terminal. When designing a PFET buck regulator the drain terminal is connected to the switching node. This situation requires a trade-off between thermal and EMI performance since increasing the PC board area of the switching node to aid the PFET power dissipation also increases radiated noise, possibly disrupting the circuit operation. Typically the switching node area is kept to a reasonable minimum and the PFET peak current is derated to stay within the recommended temperature rating of the PFET. The $R_{DS(ON)}$ of the PFET determines a portion of the power dissipation in the PFET. However, PFETs with very low $R_{DS(ON)}$ usually have large values of gate charge. A PFET with a higher gate charge has a corresponding slower switching speed, leading to higher switching losses and affecting the PFET power dissipation.

If the PFET $R_{DS(ON)}$ is used for current limit detection, note that it typically has a positive temperature coefficient. At 100°C the $R_{DS(ON)}$ may be as much as 50% higher than the value at 25°C which could result in incorrect current limiting if not accounted for when determining the value of the R_{ADJ} resistor. The PFET Total Gate Charge determines most of the power dissipation in the LM5085 due to the repetitive charge and discharge of the PFET's gate capacitance by the gate driver (powered from the VCC regulator). The LM5085's internal power dissipation can be calculated from the following:

$$P_{DISS} = V_{IN} \times ((Q_G \times F_S) + I_{IN}) \quad (14)$$

where Q_G is the PFET's Total Gate Charge obtained from its datasheet, F_S is the switching frequency, and I_{IN} is the LM5085's operating current obtained from the graph "Input Operating Current vs. V_{IN}". Using the Thermal Resistance specifications in the *Electrical Characteristics* table, the approximate junction temperature can be determined. If the calculated junction temperature is near the maximum operating temperature of 125°C, either the switching frequency must be reduced, or a PFET with a smaller Total Gate Charge must be used.

7.3.9 Soft-Start

The internal soft-start feature of the LM5085 allows the regulator to gradually reach a steady state operating point at power up, thereby reducing startup stresses and current surges. Upon turn-on, when Vcc reaches its under-voltage lockout threshold, the internal soft-start circuit ramps the feedback reference voltage from 0V to 1.25V, causing V_{OUT} to ramp up in a proportional manner. The soft-start ramp time is typically 2.5ms.

In addition to controlling the initial power up cycle, the soft-start circuit also activates when the LM5085 is enabled by releasing the RT pin, and when the circuit is shutdown and restarted by the internal Thermal Shutdown circuit.

If the voltage at FB is below the regulation threshold value due to an over-current condition or a short circuit at V_{OUT}, the internal reference voltage provided by the soft-start circuit to the regulation comparator is reduced along with FB. When the over-current or short circuit condition is removed, V_{OUT} returns to the regulated value at a rate determined by the soft-start ramp. This feature helps prevent the output voltage from overshooting following an overload event.

7.3.10 Thermal Shutdown

The LM5085 should be operated such that the junction temperature does not exceed 125°C. If the junction temperature increases above that, an internal Thermal Shutdown circuit activates at 170°C (typical) to disable the VCC regulator and the gate driver, and discharge the soft-start capacitor. This feature helps prevent catastrophic failures from accidental device overheating. When the junction temperature falls below 150°C (typical hysteresis = 20°C), the gate driver is enabled, the soft-start circuit is released, and normal operation resumes.

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7.4 Device Functional Modes

7.4.1 Standby Mode with VIN <4.5 V

The LM5085 is intended to operate with input voltages above 4.5 V. The minimum operating input voltage is determined by the VCC undervoltage lockout threshold of 3.8 V (typ). If V_{IN} is too low to support a VCC voltage greater than the VCC UVLO threshold, the controller switches to the standby mode with the PFET buck switch in the off state.

7.4.2 RT Shutdown Mode

The LM5085 is in shutdown mode when the RT pin is pulled below 0.73 V (typ). In this mode, the PFET gate driver is held off and the VCC regulator is disabled.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5085/LM5085-Q1 devices are step-down DC-DC converters. The devices are typically used to convert a higher DC voltage to a lower DC voltage. Use the following design procedure to select component values. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The final circuit is shown in Figure 25, and its performance is presented in Figure 29 through Figure 32.

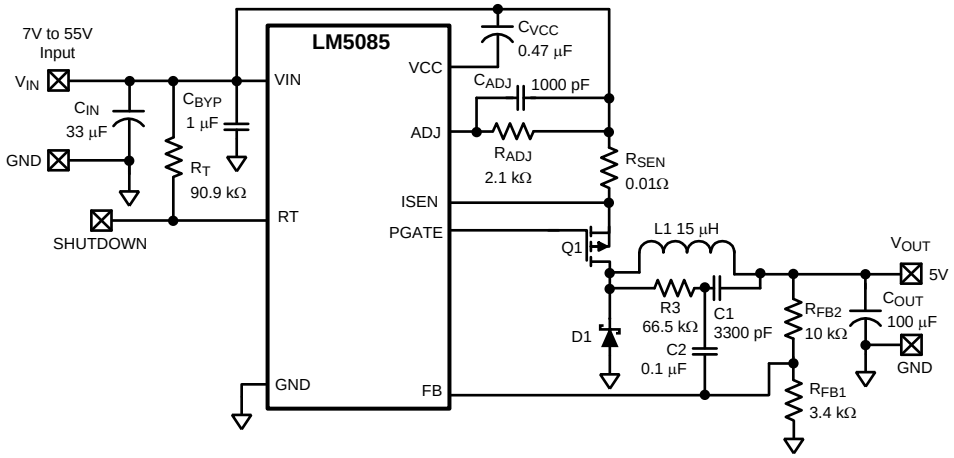

Figure 25. Example Circuit

8.2.1 Design Requirements

Referring to *Functional Block Diagram* , the circuit is to be configured for the following specifications:

- V_{OUT} = 5V
- V_{IN} = 7V to 55V, 12V Nominal
- Maximum load current ($I_{OUT(max)}$) = 5A
- Minimum load current ($I_{OUT(min)}$) = 600mA (for continuous conduction mode)
- Switching Frequency (F_{SW}) = 300kHz
- Maximum allowable output ripple (V_{OS}) = 5mVp-p
- Selected PFET: Vishay Si7465

8.2.2 Detailed Design Procedure

8.2.2.1 External Components

The procedure for calculating the external components is illustrated with the following design example.

Selected PFET: Vishay Si7465

R_{FB1} and R_{FB2}: These resistors set the output voltage. The ratio of these resistors is calculated from:

$$R_{FB2}/R_{FB1} = (V_{OUT}/1.25V) - 1 \quad (15)$$

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Typical Application (continued)

For this example, R_{FB2}/R_{FB1} = 3. Typically, R_{FB1} and R_{FB2} should be chosen from standard value resistors in the range of 1kΩ to 20kΩ which satisfy the above ratio. For this example, R_{FB2} = 10kΩ, and R_{FB1} = 3.4kΩ.

R_T, PFET: Before selecting the R_T resistor, the PFET must be selected as its turn-on and turn-off delays affect the calculated value of R_T. For the Vishay Si7465 PFET, the difference of its typical turn-off and turn-on delays is 57ns. Using Equation 5 at nominal input voltage, R_T calculates to be:

$$R_T = \frac{5 \times (12 - 1.56V)}{1.45 \times 10^{-7} \times 12 \times 300\ kHz} - \frac{(50\ ns + 57\ ns) \times (12 - 1.56V)}{1.45 \times 10^{-7}} - 1.4 = 90.9 \tag{16}$$

A standard value 90.9kΩ resistor is selected. Using Equation 3, the minimum on-time at the PGATE pin, which occurs at maximum input voltage (55V), is calculated to be 300ns. This minimum one-shot period is sufficiently longer than the minimum recommended value of 150ns. The minimum on-time at the SW node (junction of Q1, D1, L1) is longer due to the delay added by the PFET (57ns). Therefore the minimum SW node on-time is 357ns at 55V. The maximum on-time at the SW node is calculated to be 2.55µs at 7V.

L1: The main parameter controlled by the inductor value is the current ripple amplitude (I_{OR}). See Figure 26. The minimum load current for continuous conduction mode is used to determine the maximum allowable ripple such that the inductor current valley does not fall to zero. Continuous conduction mode operation at minimum load current is not a requirement of the LM5085, but serves as a guideline for selecting L1. For this example, the maximum ripple current is:

$$I_{OR(max)} = 2 \times I_{OUT(min)} = 1.2\ Amp \tag{17}$$

If the minimum load current of the application is zero, a good initial estimate for the maximum ripple current ($I_{OR(max)}$) is 20% of the maximum load current. The ripple calculated in Equation 17 is then used in the following equation to calculate L1:

$$L1 = \frac{t_{ON(min)} \times (V_{IN(max)} - V_{OUT})}{I_{OR(max)}} = 14.9\ \mu H \tag{18}$$

A standard value 15µH inductor is selected. Using this inductance value, the maximum ripple current amplitude, which occurs at maximum input voltage, is calculated to be 1.19 Ap-p. The peak current (I_{PK}) at maximum load current is 5.6A. However, the current rating of the selected inductor must be based on the maximum current limit value calculated below.

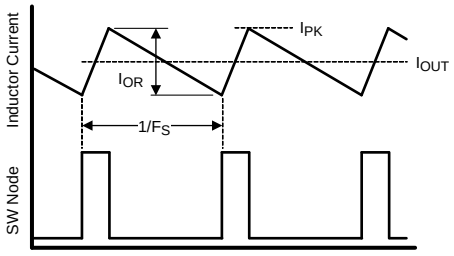

Figure 26. Inductor Current Waveform

R_{SEN}, R_{ADJ}: To achieve good current limit accuracy and avoid over designing the power stage components, the sense resistor method is used for current limiting in this example. A standard value 10mΩ resistor is selected for R_{SEN}, resulting in a 50mV drop at maximum load current, and a maximum 0.25W power dissipation in the resistor. Since the LM5085 uses peak current detection, the minimum value for the current limit threshold must be equal to the maximum load current (5A) plus half the maximum ripple amplitude calculated above:

$$I_{CL(min)} = 5A + 1.19A/2 = 5.6A \tag{19}$$

At this current level the voltage across R_{SEN} is 56mV. Adding the current limit comparator offset of 9mV (max) increases the required current limit threshold to 6.5A. Using Equation 9 with the minimum value for the ADJ pin current (32µA), the required R_{ADJ} resistor is calculated to be:

$$R_{ADJ} = \frac{6.5A \times 0.01\Omega}{32\ \mu A} = 2.03\ k\Omega \tag{20}$$

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Typical Application (continued)

A standard value 2.1kΩ resistor is selected. The nominal current limit threshold is:

$$I_{CL(nom)} = \frac{(2.1\ k\Omega \times 40\ \mu A)}{0.01\Omega} = 8.4A \quad (21)$$

Using the tolerances for the ADJ pin current and the current limit comparator offset, the maximum current limit threshold is calculated to be:

$$I_{CL(max)} = \frac{(2.1\ k\Omega \times 48\ \mu A) + 9\ mV}{0.01\Omega} = 11A \quad (22)$$

The minimum current limit threshold is:

$$I_{CL(min)} = \frac{(2.1\ k\Omega \times 32\ \mu A) - 9\ mV}{0.01\Omega} = 5.82A \quad (23)$$

The load current in each case is equal to the current limit threshold minus half the current ripple amplitude. The recommended value of 1000pF for C_{ADJ} is used in this example.

C_{OUT}: Since the maximum allowed output ripple voltage is very low in this example (5 mVp-p), the minimum ripple configuration (R3, C1, and C2 in the Block Diagram) must be used. The resulting ripple at V_{OUT} is then due to the inductor's ripple current passing through C_{OUT}. This capacitor's value can be selected based on the maximum allowable ripple voltage at V_{OUT}, or based on transient response requirements. The following calculation, based on ripple voltage, provides a first order result for the value of C_{OUT}:

$$C_{OUT} = \frac{I_{OR(max)}}{8 \times F_S \times V_{RIPPLE}} \quad (24)$$

where $I_{OR(max)}$ is the maximum ripple current calculated above, and V_{RIPPLE} is the allowable ripple at V_{OUT}.

$$C_{OUT} = \frac{1.19A}{8 \times 300\ kHz \times 0.005V} = 99.2\ \mu F \quad (25)$$

A 100µF capacitor is selected. Typically the ripple amplitude will be higher than the calculations indicate due to the capacitor's ESR.

R3, C1, C2: The minimum ripple configuration uses these three components to generate the ripple voltage required at the FB pin since there is insufficient ripple at V_{OUT}. A minimum of 25 mVp-p must be applied to the FB pin to obtain stable constant frequency operation. R3 and C1 are selected to generate a sawtooth waveform at their junction, and that waveform is AC coupled to the FB pin via C2. The values of the three components are determined using the following procedure:

Calculate $V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN(min)})))$ (26)

where V_{SW} is the absolute value of the voltage at the SW node during the off-time, typically 0.5V to 1V depending on the diode D1. Using a typical value of 0.65V, V_A calculates to 4.81V. V_A is the nominal DC voltage at the R3/C1 junction, and is used in the next equation to calculate the R3-C3 product:

$$R3 \times C1 = \frac{(V_{IN(min)} - V_A) \times t_{ON}}{\Delta V} \quad (27)$$

where t_{ON} is the maximum on-time (at minimum input voltage), and ΔV is the desired ripple amplitude at the R3-C1 junction. For ripple voltage of 25 mVp-p:

$$R3 \times C1 = \frac{(7V - 4.81V) \times 2.55\ \mu s}{0.025V} = 2.23 \times 10^{-4} \quad (28)$$

R3 and C1 are then selected from standard value components to produce the product calculated above. Typical values for C1 are 3000pF to 10,000pF, and R3 is typically from 10kΩ to 300kΩ. C2 is then chosen large compared to C1, typically 0.1µF. For this example, 3300pF is chosen for C1, requiring R3 to be 67.7kΩ. A standard value 66.5kΩ resistor is selected.

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Typical Application (continued)

C_{IN}, C_{BYP}: These capacitors limit the voltage ripple at VIN by supplying most of the switch current during the on-time. At maximum load current, when Q1 is switched on, the current through Q1 suddenly increases to the lower peak of the inductor's ripple current, then ramps up to the upper peak, and then drops to zero at turn-off. The average current during the on-time is the load current. For a worst case calculation, these capacitors must supply this average load current during the maximum on-time, while limiting the voltage drop at VIN. For this example, 0.5V is selected as the maximum allowable droop at VIN. The minimum input capacitance is calculated from:

$$C_{IN} + C_{BYP} = \frac{I_{OUT(max)} \times t_{ON(max)}}{\Delta V} = \frac{5A \times 2.55\ \mu s}{0.5V} = 25.5\ \mu F \quad (29)$$

A 33µF electrolytic capacitor is selected for C_{IN}, and a 1µF ceramic capacitor is selected for C_{BYP}. Due to the ESR of C_{IN}, the ripple at VIN will likely be higher than the calculation indicates, and therefore it may be desirable to increase C_{IN} to 47µF or 68µF. C_{BYP} must be located as close as possible to the VIN and GND pins of the LM5085. The voltage rating for both capacitors must be at least 55V. The RMS ripple current rating for the input capacitors must also be considered. A good approximation for the required ripple current rating is $I_{RMS} > I_{OUT}/2$.

D1: A Schottky diode is recommended. Ultra-fast recovery diodes are not recommended as the high speed transitions at the SW node may affect the regulator's operation due to the diode's reverse recovery transients. The diode must be rated for the maximum input voltage, and the worst case current limit level. The average power dissipation in the diode is calculated from:

$$P_{D1} = V_F \times I_{OUT} \times (1\text{-}D) \quad (30)$$

where V_F is the diode's forward voltage drop, and D is the on-time duty cycle. Using Equation 1, the minimum duty cycle occurs at maximum input voltage, and is calculated to be ≅9.1% in this example. The diode power dissipation calculates to be:

$$P_{D1} = 0.65V \times 5A \times (1 - 0.091) = 2.95W \quad (31)$$

C_{VCC}: The capacitor at the VCC pin (from VIN to VCC) provides not only noise filtering and stability for the VCC regulator, but also provides the surge current for the PFET gate drive. The typical recommended value for C_{VCC} is 0.47µF. A good quality, low ESR, ceramic capacitor is recommended. C_{VCC} must be located as close as possible to the VIN and VCC pins. If the selected PFET has a Total Gate Charge specification of 100nC or larger, or if the circuit is required to operate at input voltages below 7V, a larger capacitor may be required. The maximum recommended value for C_{VCC} is 1µF.

IC Power Dissipation: The maximum power dissipated in the LM5085 package is calculated using Equation 14 at the maximum input voltage. The Total Gate Charge for the Si7465 PFET is specified to be 40nC (max) in its data sheet. Therefore the total power dissipation within the LM5085 is calculated to be:

$$P_{DISS} = 55V \times ((40nC \times 300kHz) + 1.4mA) = 737mW \quad (32)$$

Using an HVSSOP package with a θ_{JA} of 46°C/W produces a temperature rise of 34°C from junction to ambient.

8.2.2.2 Alternate Output Ripple Configurations

The minimum ripple configuration employing C1, C2, and R3 in Figure 25 results in a low ripple amplitude at V_{OUT} determined mainly by the characteristics of the output capacitor and the ripple current in L1. This configuration allows multiple ceramic capacitors to be used for V_{OUT} if the output voltage is provided to several places on the PC board. However, if a slightly higher level of ripple at V_{OUT} is acceptable in the application, and distributed capacitance is not used, the ripple required for the FB comparator pin can be generated with fewer external components using the circuits shown below.

a) Reduced ripple configuration: In Figure 27, R3, C1 and C2 are removed (compared to Figure 25). A low value resistor (R4) is added in series with C_{OUT}, and a capacitor (Cff) is added across R_{FB2}. Ripple is generated at V_{OUT} by the inductor ripple current flowing through R4, and that ripple voltage is passed to the FB pin via Cff. The ripple at V_{OUT} can be set as low as 25 mVp-p since it is not attenuated by R_{FB2} and R_{FB1}. The minimum value for R4 is calculated from:

$$R4 = \frac{25\ mV}{I_{OR(min)}} \quad (33)$$

where $I_{OR(min)}$ is the minimum ripple current, which occurs at minimum input voltage. The minimum value for Cff is determined from:

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Typical Application (continued)

$$Cff = \frac{3 \times t_{ON(max)}}{(R_{FB1} // R_{FB2})} \quad (34)$$

where $t_{ON(max)}$ is the maximum on-time, which occurs at minimum VIN. The next larger standard value capacitor should be used for Cff.

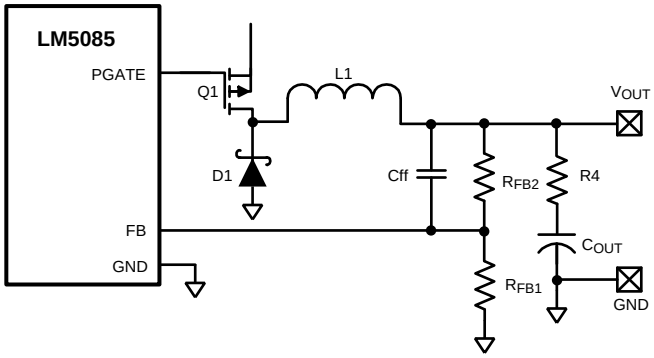

Figure 27. Reduced Ripple Configuration

b) Lowest cost configuration: This configuration, shown in Figure 28, is the same as Figure 27 except Cff is removed. Since the ripple voltage at V_{OUT} is attenuated by R_{FB2} and R_{FB1}, the minimum ripple required at V_{OUT} is equal to:

$$V_{RIP(min)} = 25mV \times (R_{FB2} + R_{FB1})/R_{FB1} \quad (35)$$

The minimum value for R4 is calculated from:

$$R4 = \frac{V_{RIP(min)}}{I_{OR(min)}} \quad (36)$$

where $I_{OR(min)}$ is the minimum ripple current, which occurs at minimum input voltage.

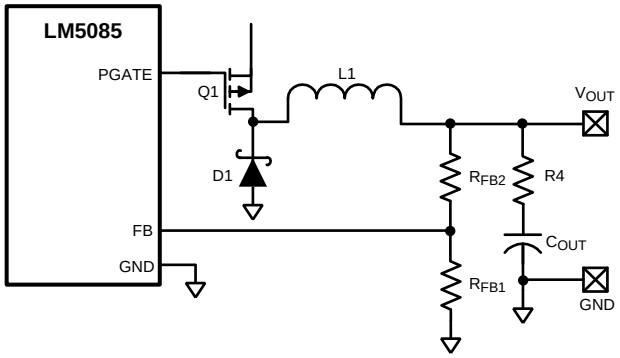

Figure 28. Lowest Cost Ripple Generating Configuration

Typical Application (continued)

8.2.3 Application Curves

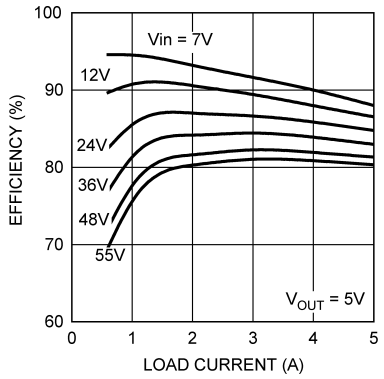

Figure 29. Efficiency vs. Load Current and V_{IN} (Circuit of Figure 25)

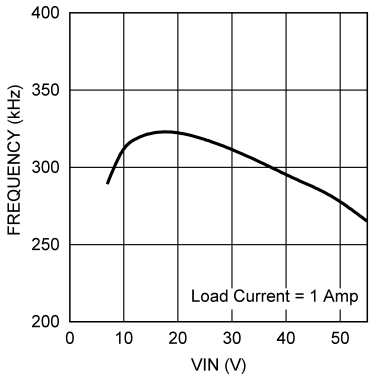

Figure 30. Frequency vs. V_{IN} (Circuit of Figure 25)

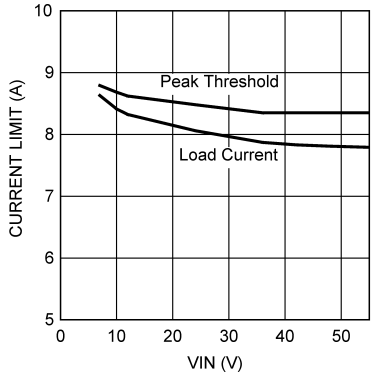

Figure 31. Current Limit vs. V_{IN} (Circuit of Figure 25)

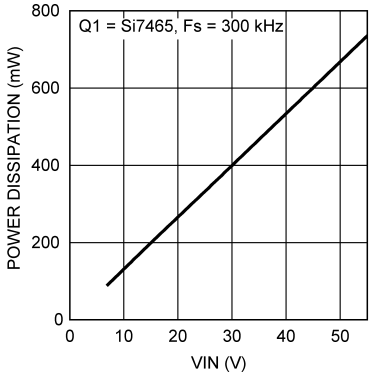

Figure 32. LM5085 Power Dissipation (Circuit of Figure 25)

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9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 75 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required at the input terminals of the converter in addition to the calculated values to limit the inductive spikes due to the input cables or wires.

10 Layout

10.1 Layout Guidelines

In most applications, the heat sink pad or tab of Q1 is connected to the switch node, i.e. the junction of Q1, L1 and D1. While it is common to extend the PC board pad from under these devices to aid in heat dissipation, the pad size should be limited to minimize EMI radiation from this switching node. If the PC board layout allows, a similarly sized copper pad can be placed on the underside of the PC board, and connected with as many vias as possible to aid in heat dissipation.

The voltage regulation, over-voltage, and current limit comparators are very fast and can respond to short duration noise pulses. Layout considerations are therefore critical for optimum performance. The layout must be as neat and compact as possible with all the components as close as possible to their associated pins. Two major current loops conduct currents which switch very fast, requiring the loops to be as small as possible to minimize conducted and radiated EMI. The first loop is that formed by C_{IN}, Q1, L1, C_{OUT}, and back to C_{IN}. The second loop is that formed by D1, L1, C_{OUT}, and back to D1. The connection from the anode of D1 to the ground end of C_{IN} must be short and direct. C_{IN} must be as close as possible to the VIN and GND pins, and C_{VCC} must be as close as possible to the VIN and VCC pins.

If the anticipated internal power dissipation of the LM5085 will produce excessive junction temperatures during normal operation, a package option with an exposed pad must be used (HVSSOP-8 or WSON-8). Effective use of the PC board ground plane can help dissipate heat. Additionally, the use of wide PC board traces, where possible, helps conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) also helps reduce the junction temperature.

10.2 Layout Example

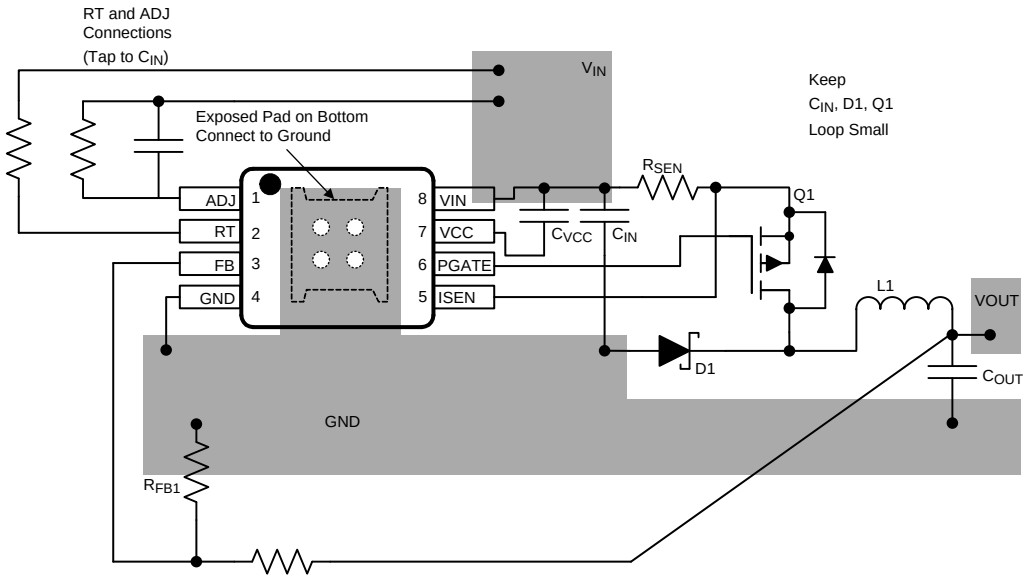

Figure 33. LM5085 Buck Converter Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM5085	Click here	Click here	Click here	Click here	Click here
LM5085-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5085MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SSTB	Samples
LM5085MME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SSTB	Samples
LM5085MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SSTB	Samples
LM5085MY/NOPB	ACTIVE	HVSSOP	DGN	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SSSB	Samples
LM5085MYE/NOPB	ACTIVE	HVSSOP	DGN	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SSSB	Samples
LM5085MYX/NOPB	ACTIVE	HVSSOP	DGN	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SSSB	Samples
LM5085QMY/NOPB	ACTIVE	HVSSOP	DGN	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SYCB	Samples
LM5085QMYE/NOPB	ACTIVE	HVSSOP	DGN	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SYCB	Samples
LM5085QMYX/NOPB	ACTIVE	HVSSOP	DGN	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SYCB	Samples
LM5085SD/NOPB	ACTIVE	WSON	NGQ	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L245B	Samples
LM5085SDE/NOPB	ACTIVE	WSON	NGQ	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L245B	Samples
LM5085SDX/NOPB	ACTIVE	WSON	NGQ	8	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L245B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM5085, LM5085-Q1 :

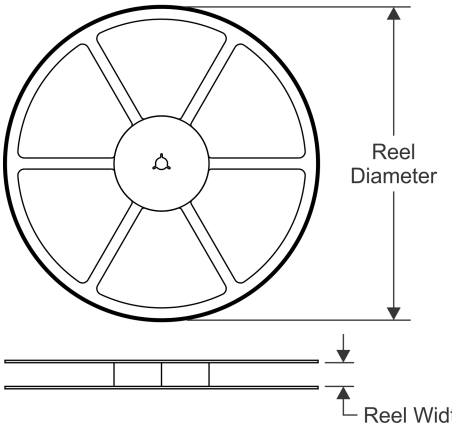
- Catalog: LM5085
- Automotive: LM5085-Q1

NOTE: Qualified Version Definitions:

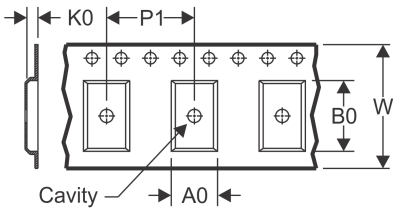
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

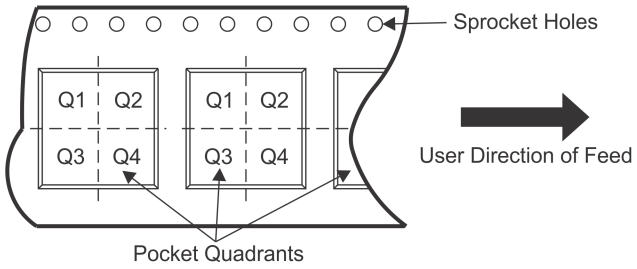


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

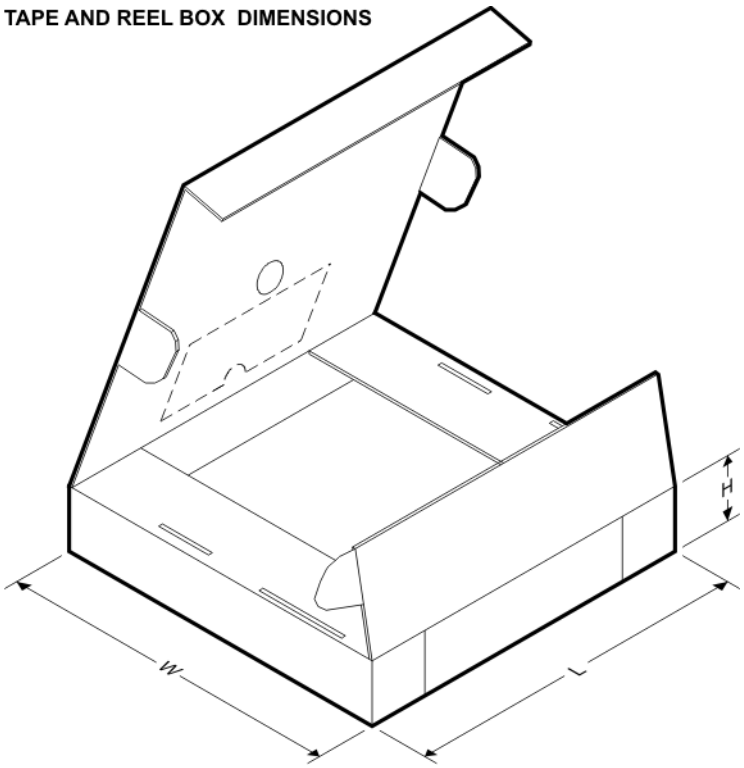
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5085MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5085MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5085MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5085MY/NOPB	HVSSOP	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5085MYE/NOPB	HVSSOP	DGN	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5085MYX/NOPB	HVSSOP	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5085QMY/NOPB	HVSSOP	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5085QMYE/NOPB	HVSSOP	DGN	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5085QMYX/NOPB	HVSSOP	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5085SD/NOPB	WSON	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5085SDE/NOPB	WSON	NGQ	8	250	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5085SDX/NOPB	WSON	NGQ	8	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

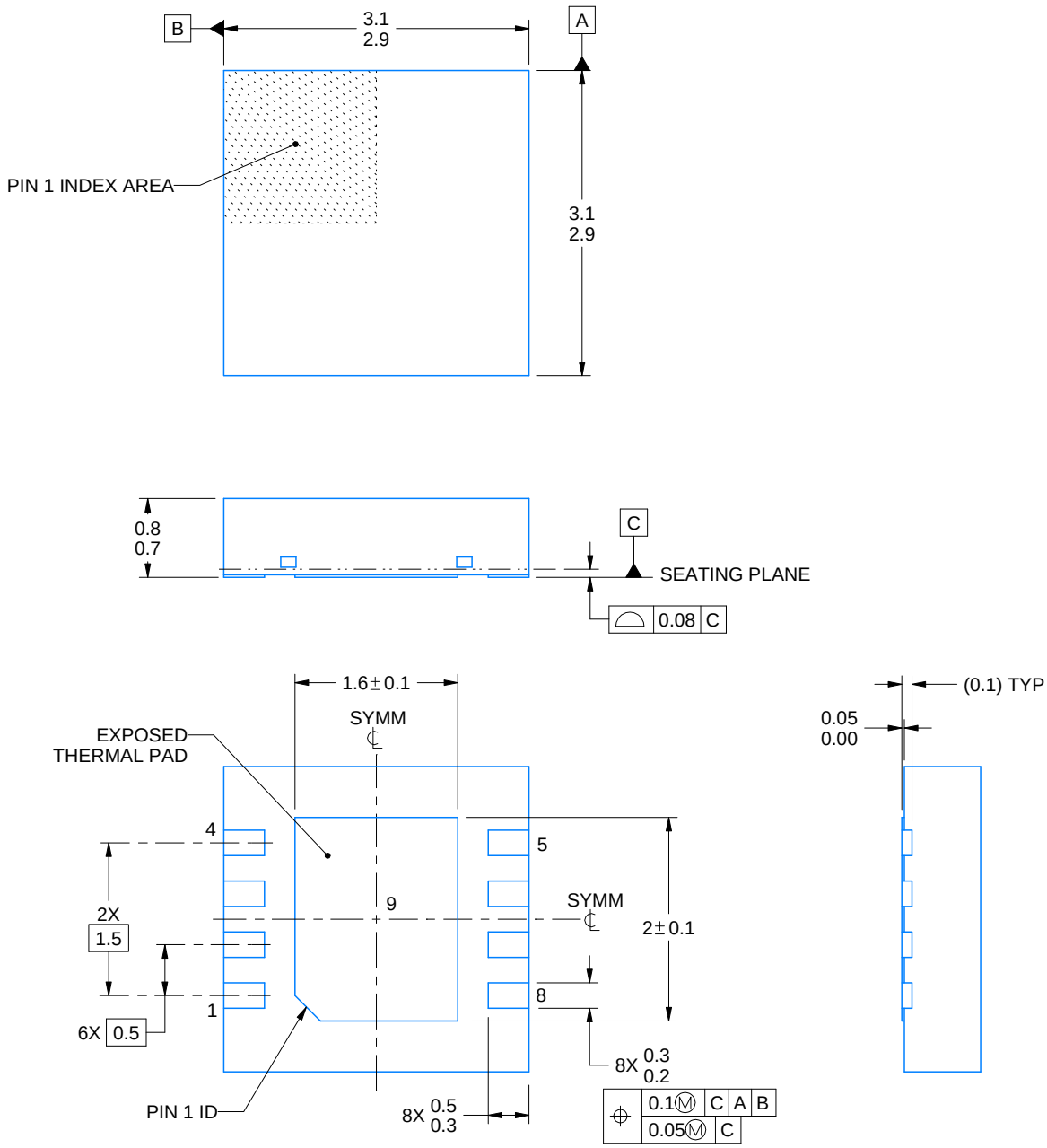
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5085MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM5085MME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LM5085MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM5085MY/NOPB	HVSSOP	DGN	8	1000	210.0	185.0	35.0
LM5085MYE/NOPB	HVSSOP	DGN	8	250	210.0	185.0	35.0
LM5085MYX/NOPB	HVSSOP	DGN	8	3500	367.0	367.0	35.0
LM5085QMY/NOPB	HVSSOP	DGN	8	1000	210.0	185.0	35.0
LM5085QMYE/NOPB	HVSSOP	DGN	8	250	210.0	185.0	35.0
LM5085QMYX/NOPB	HVSSOP	DGN	8	3500	367.0	367.0	35.0
LM5085SD/NOPB	WSON	NGQ	8	1000	210.0	185.0	35.0
LM5085SDE/NOPB	WSON	NGQ	8	250	210.0	185.0	35.0
LM5085SDX/NOPB	WSON	NGQ	8	4500	367.0	367.0	35.0

PACKAGE OUTLINE

NGQ0008A

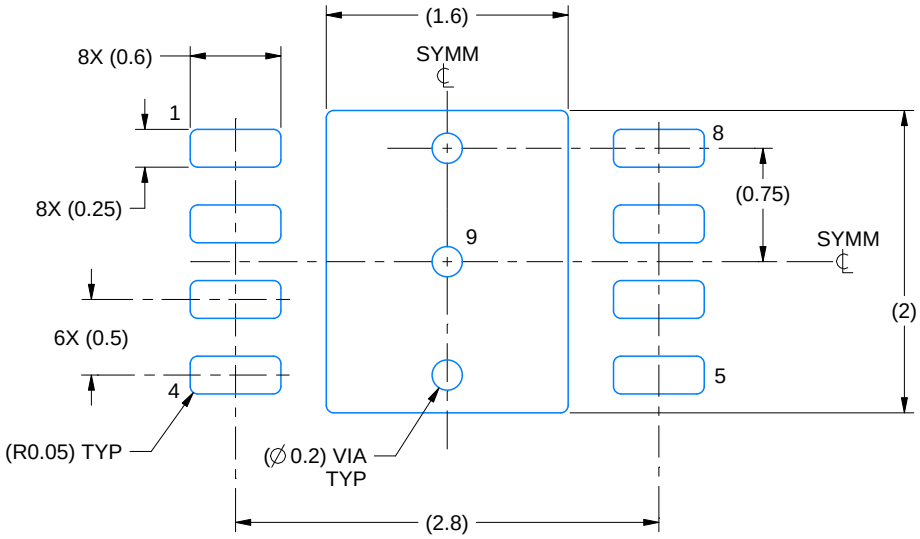
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

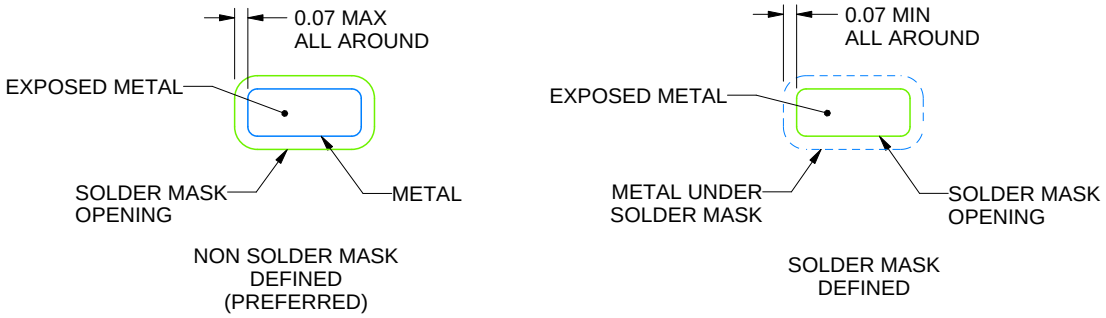


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

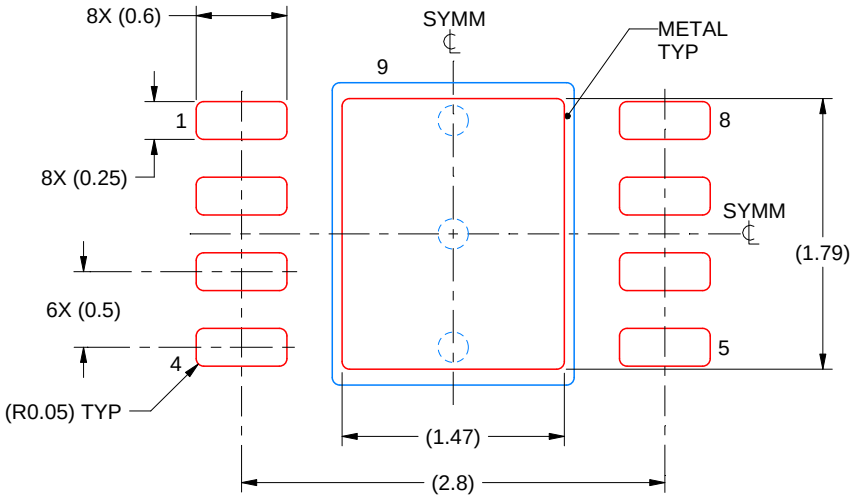


SOLDER MASK DETAILS

4214922/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

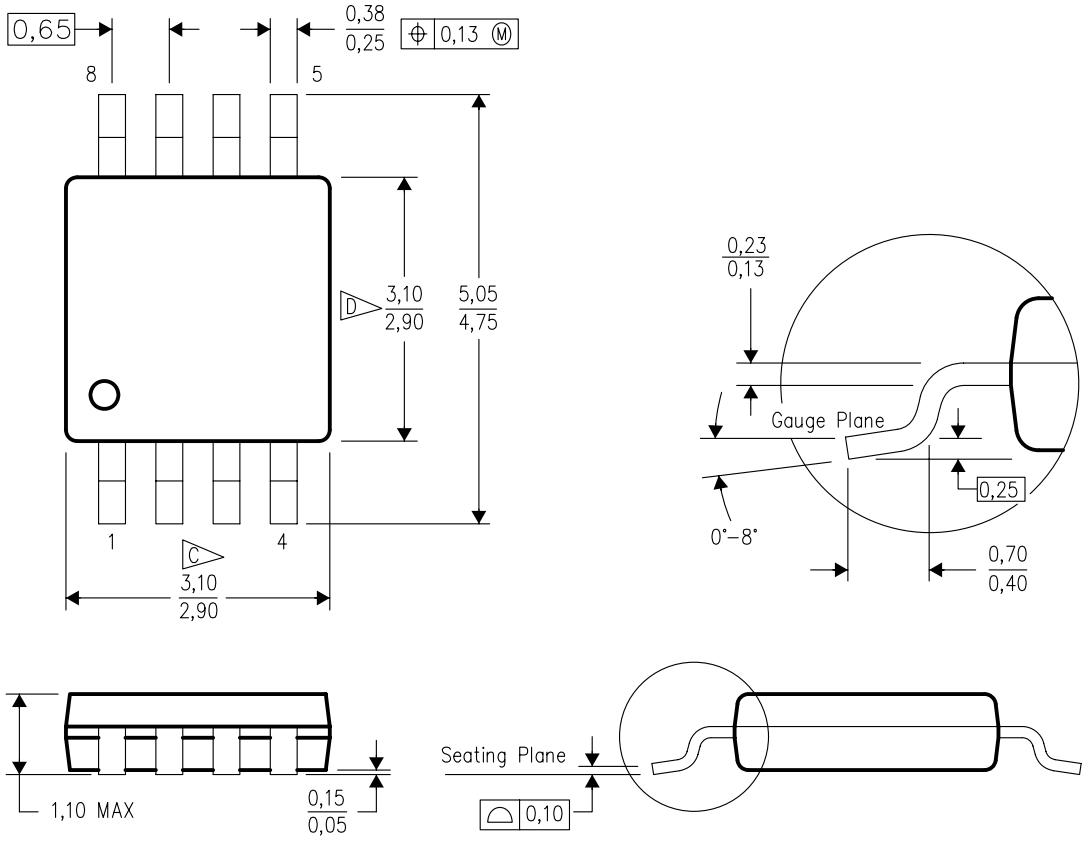
EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214922/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

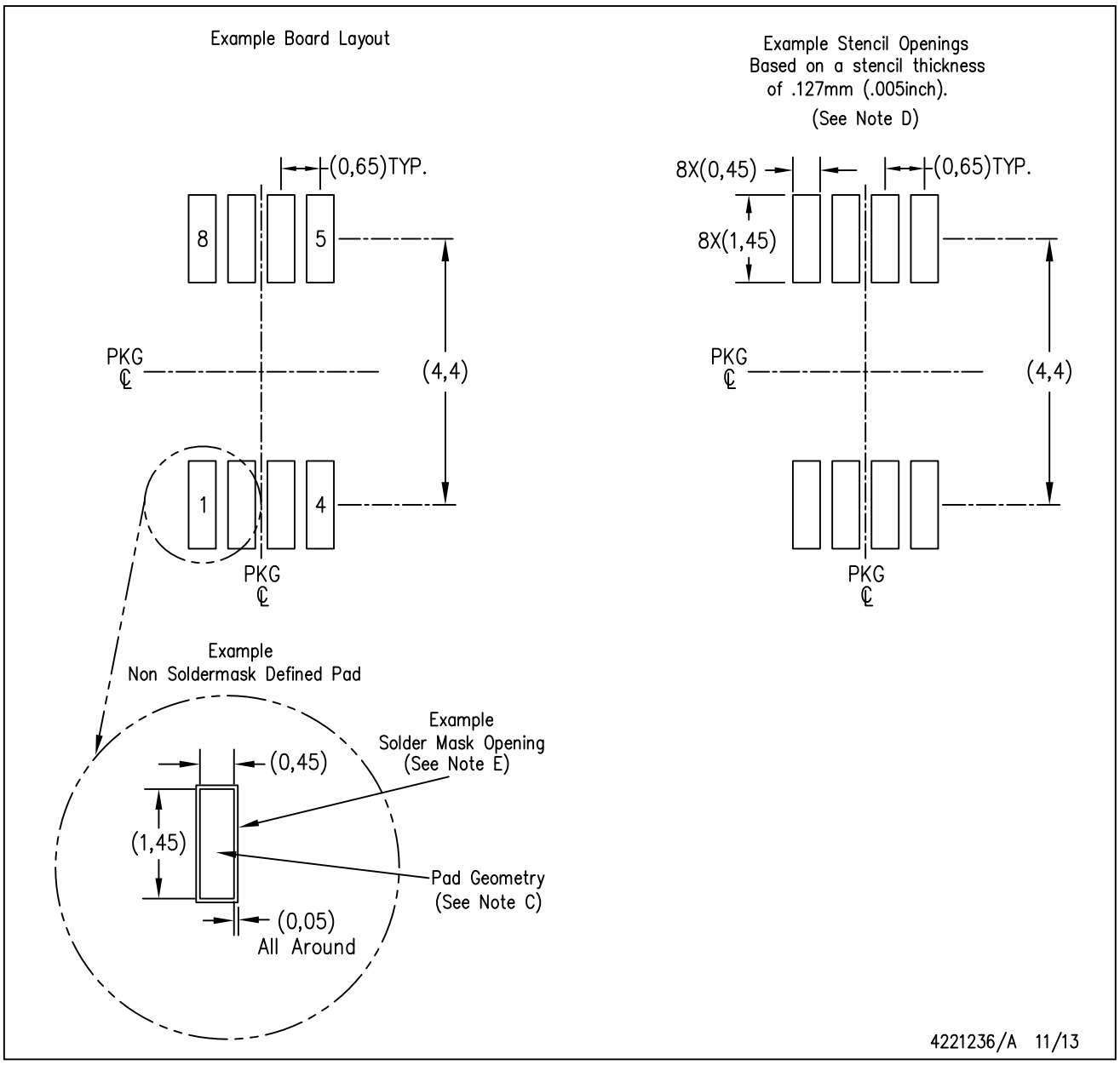
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

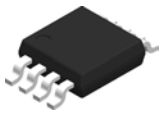
DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

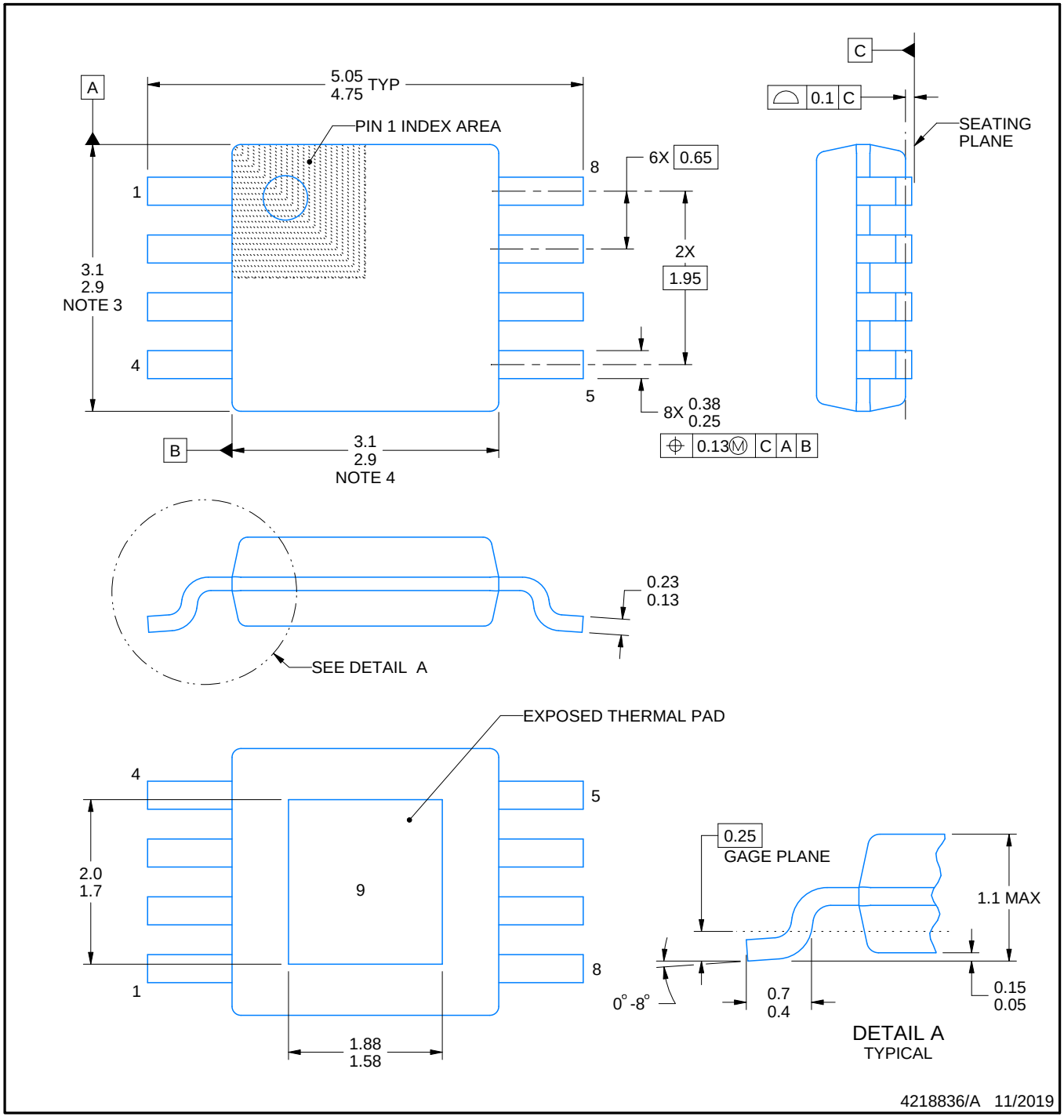
PACKAGE OUTLINE

DGN0008A



PowerPAD™ VSSOP - 1.1 mm max height

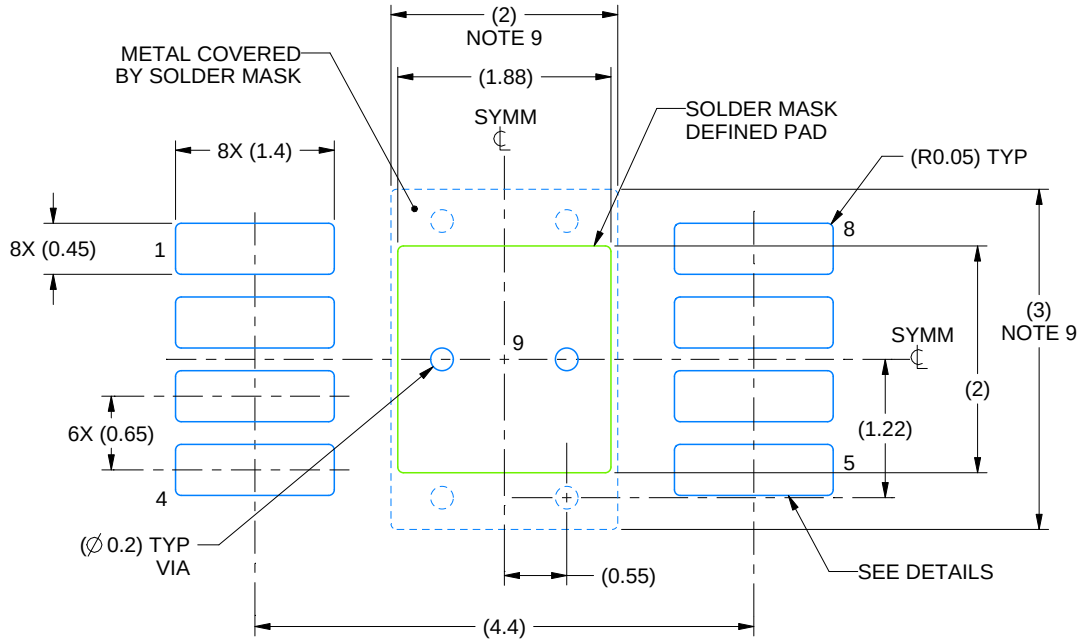
SMALL OUTLINE PACKAGE



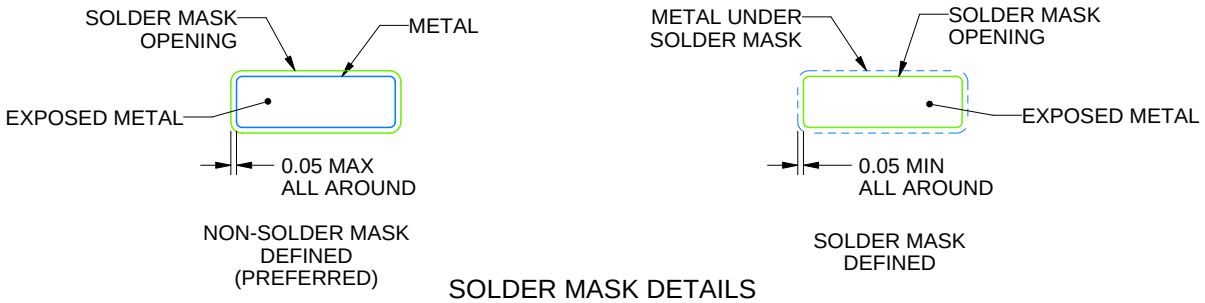
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

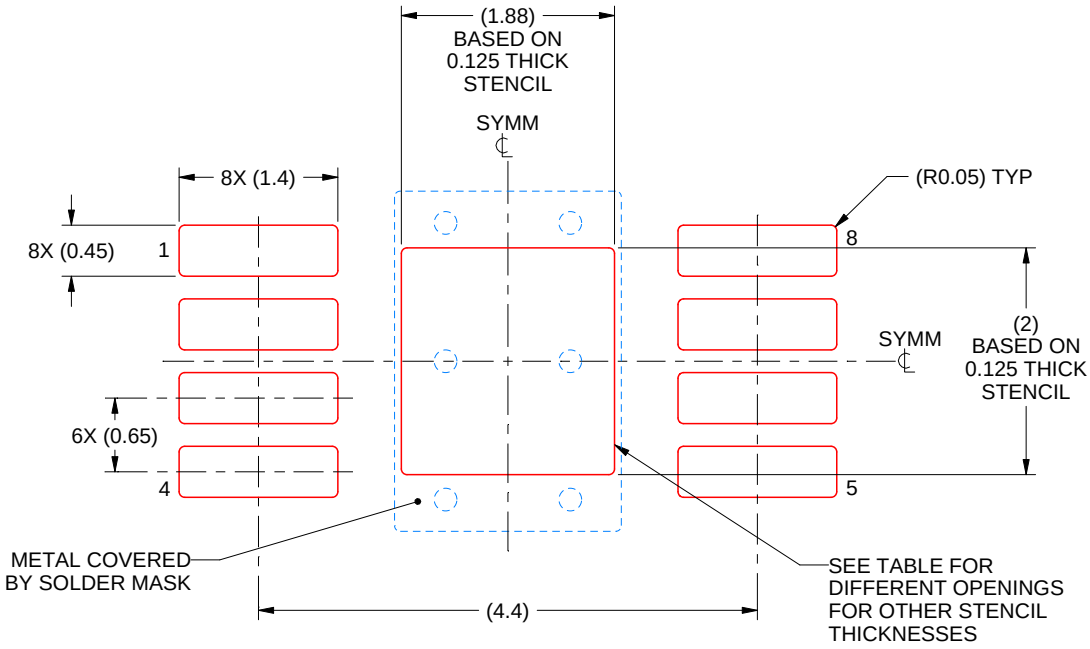
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.24
0.125	1.88 X 2.00 (SHOWN)
0.15	1.72 X 1.83
0.175	1.59 X 1.69

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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