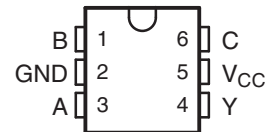
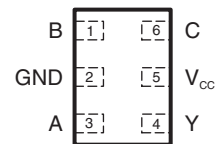


# SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

Check for Samples: [SN74AUP1T98](#)

## FEATURES

- Available in the Texas Instruments NanoStar™ Packages
- Single-Supply Voltage Translator
- 1.8 V to 3.3 V (at  $V_{CC} = 3.3$  V)
- 2.5 V to 3.3 V (at  $V_{CC} = 3.3$  V)
- 1.8 V to 2.5 V (at  $V_{CC} = 2.5$  V)
- 3.3 V to 2.5 V (at  $V_{CC} = 2.5$  V)
- Nine Configurable Gate Logic Functions
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity
- $I_{off}$  Supports Partial-Power-Down Mode With Low Leakage Current (0.5  $\mu$ A)
- Very Low Static and Dynamic Power Consumption
- Pb-Free Packages Available: SOT-23 (DBV), SC-70 (DCK), and WCSP (NanoStar)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Related Devices: SN74AUP1T97, SN74AUP1T57, and SN74AUP1T58

DBV OR DCK PACKAGE  
(TOP VIEW)

DRY OR DSF PACKAGE  
(TOP VIEW)

YFP OR YZP PACKAGE  
(TOP VIEW)


## DESCRIPTION

AUP technology is the industry's lowest-power logic technology designed for use in battery-operated or battery backed-up equipment. The SN74AUP1T98 is designed for logic-level translation applications with input switching levels that accept 1.8-V LVCMOS signals, while operating from either a single 3.3-V or 2.5-V  $V_{CC}$  supply.

The wide  $V_{CC}$  range of 2.3 V to 3.6 V allows the possibility of battery voltage drop during system operation and ensures normal operation between this range.

Schmitt-trigger inputs ( $\Delta V_T = 210$  mV between positive and negative input transitions) offer improved noise immunity during switching transitions, which is especially useful on analog mixed-mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and allow for slow input signal transition.

The SN74AUP1T98 can be easily configured to perform a required gate function by connecting A, B, and C inputs to  $V_{CC}$  or ground (see Function Selection table). Up to nine commonly used logic gate functions can be performed.

$I_{off}$  is a feature that allows for powered-down conditions ( $V_{CC} = 0$  V) and is important in portable and mobile applications. When  $V_{CC} = 0$  V, signals in the range from 0 V to 3.6 V can be applied to the inputs and outputs of the device. No damage occurs to the device under these conditions.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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The SN74AUP1T98 is designed with optimized current-drive capability of 4 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

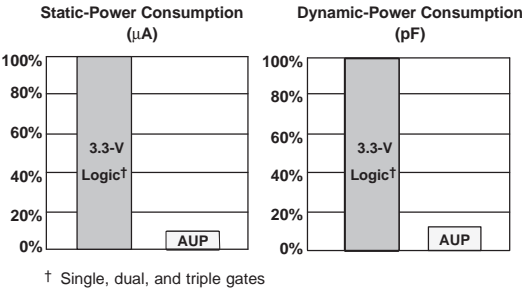
NanoStar package technology is a major breakthrough in IC packaging concepts, using the die as the package.

**ORDERING INFORMATION**

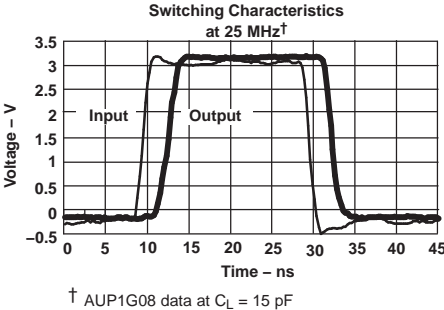
For package and ordering information, see the Package Option Addendum at the end of this document.

**FUNCTION SELECTION TABLE**

LOGIC FUNCTION	FIGURE NO.
2-to-1 data selector	5
2-input NAND gate	6
2-input NOR gate with one inverted input	7
2-input NAND gate with one inverted input	7
2-input NAND gate with one inverted input	8
2-input NOR gate with one inverted input	8
2-input NOR gate	9
Inverter	10
Noninverted buffer	11



**Figure 1. AUP – The Lowest-Power Family**



**Figure 2. Excellent Signal Integrity**

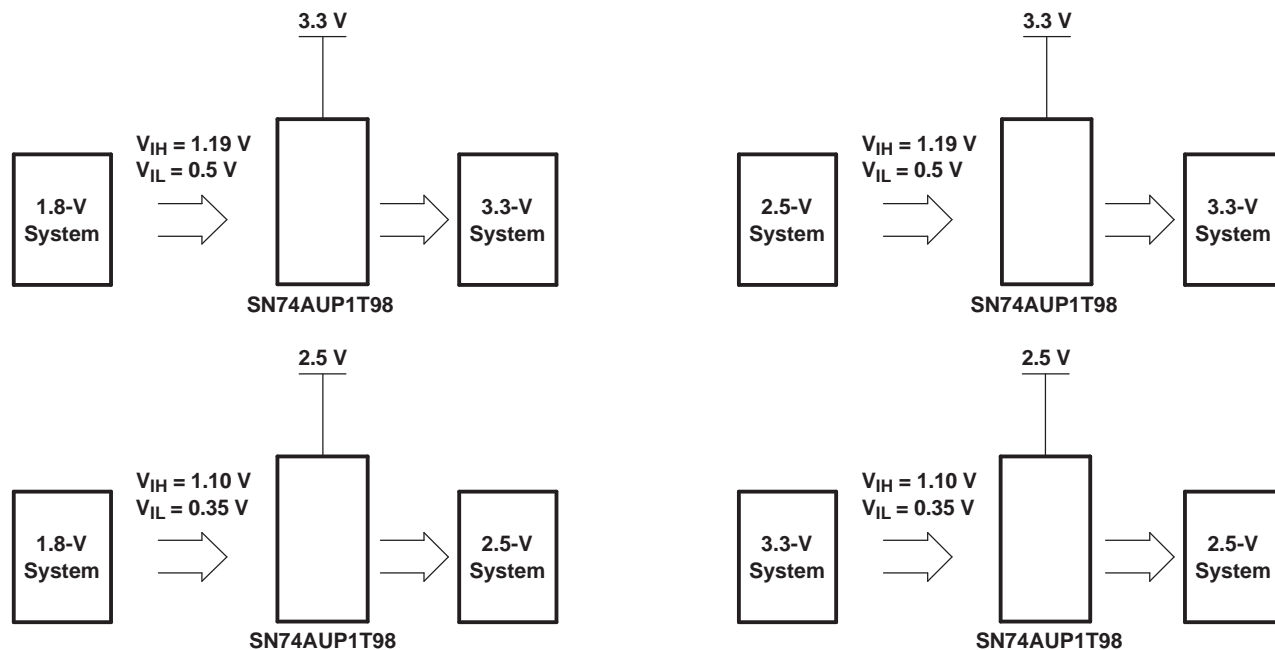


Figure 3. Possible Voltage-Translation Combinations

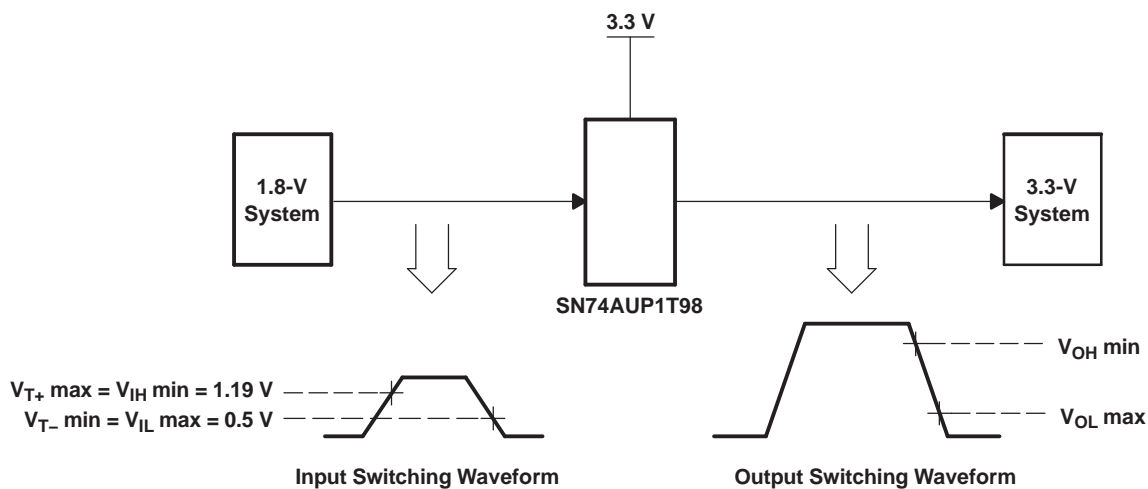
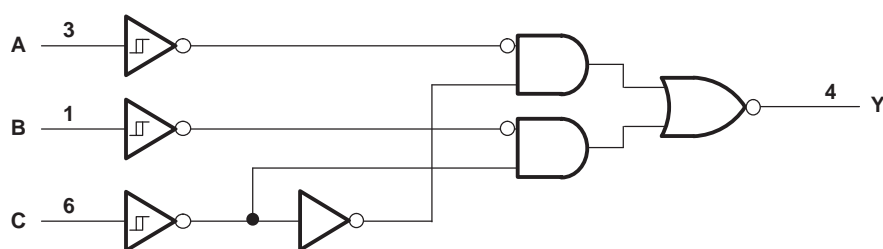
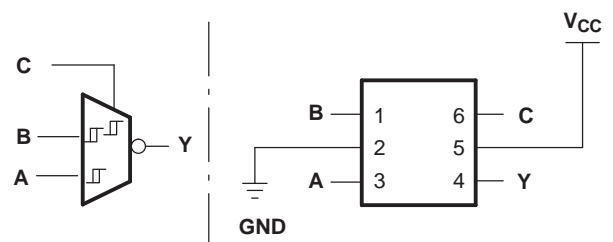


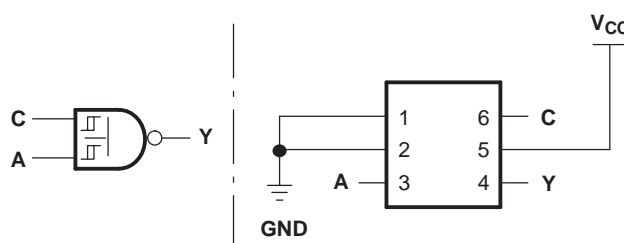
Figure 4. Switching Thresholds for 1.8-V to 3.3-V Translation

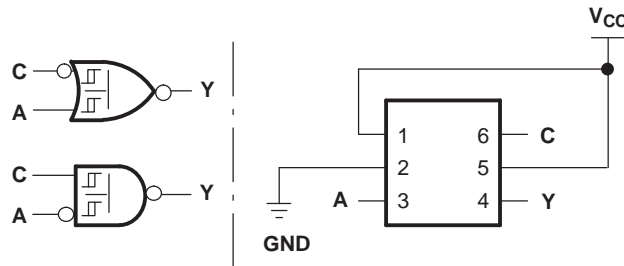
**FUNCTION TABLE**

INPUTS			OUTPUT Y
C	B	A	
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

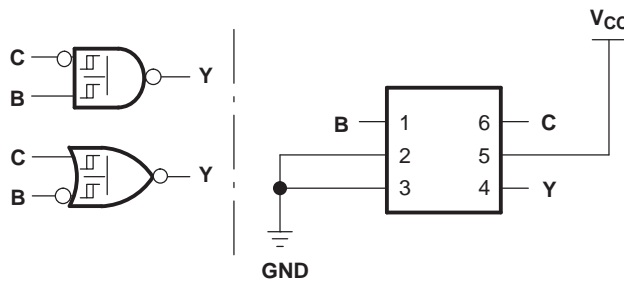
**LOGIC DIAGRAM (POSITIVE LOGIC)****LOGIC CONFIGURATIONS**

**Figure 5. 157+04: 2-to-1 Data Selector With Inverted Output**  
 When C is L, Y =  $\overline{B}$   
 When C is H, Y =  $\overline{A}$

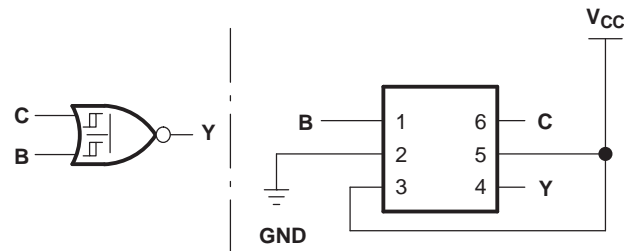
**Figure 6. 00: 2-Input NAND Gate**



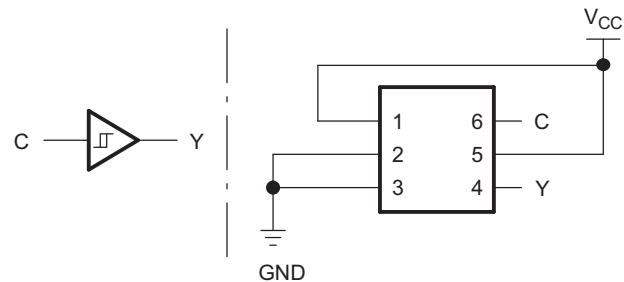
**Figure 7. 14+02/14+08: 2-Input NOR Gate With One Inverted Input  
2-Input NAND Gate With One Inverted Input**



**Figure 8. 14+00/14+32: 2-Input NAND Gate With One Inverted Input  
2-Input NOR Gate With One Inverted Input**



**Figure 9. 32: 2-Input NOR Gate**



**Figure 10. 17/34: Noninverted Buffer**

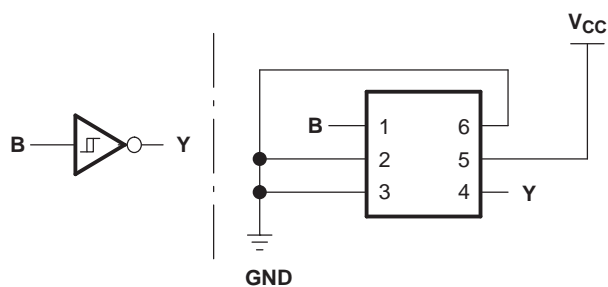


Figure 11. 04/14: Inverter

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		–0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>		–0.5	4.6	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>		–0.5	4.6	V
V <sub>O</sub>	Output voltage range in the high or low state <sup>(2)</sup>		–0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		–50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		–50	mA
I <sub>O</sub>	Continuous output current			±20	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>	DBV package		165	°C/W
		DCK package		259	
		DRY package		340	
		DSF package		300	
		YFP package		123	
		YZP package		123	
T <sub>stg</sub>	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.3	3.6	V
V <sub>I</sub>	Input voltage		0	3.6	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.3 V		–3.1	mA
		V <sub>CC</sub> = 3 V		–4	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.3 V		3.1	mA
		V <sub>CC</sub> = 3 V		4	
T <sub>A</sub>	Operating free-air temperature		–40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V <sub>T+</sub> Positive-going input threshold voltage			2.3 V to 2.7 V	0.6		1.1	0.6	1.1	V
			3 V to 3.6 V	0.75		1.16	0.75	1.19	
V <sub>T–</sub> Negative-going input threshold voltage			2.3 V to 2.7 V	0.35		0.6	0.35	0.6	V
			3 V to 3.6 V	0.5		0.85	0.5	0.85	
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> – V <sub>T–</sub> )			2.3 V to 2.7 V	0.23		0.6	0.1	0.6	V
			3 V to 3.6 V	0.25		0.56	0.15	0.56	
V <sub>OH</sub>		I <sub>OH</sub> = –20 μA	2.3 V to 3.6 V	V <sub>CC</sub> – 0.1			V <sub>CC</sub> – 0.1		V
		I <sub>OH</sub> = –2.3 mA	2.3 V	2.05			1.97		
		I <sub>OH</sub> = –3.1 mA		1.9			1.85		
		I <sub>OH</sub> = –2.7 mA	3 V	2.72			2.67		
		I <sub>OH</sub> = –4 mA		2.6			2.55		
V <sub>OL</sub>		I <sub>OL</sub> = 20 μA	2.3 V to 3.6 V	0.1			0.1		V
		I <sub>OL</sub> = 2.3 mA	2.3 V	0.31			0.33		
		I <sub>OL</sub> = 3.1 mA		0.44			0.45		
		I <sub>OL</sub> = 2.7 mA	3 V	0.31			0.33		
		I <sub>OL</sub> = 4 mA		0.44			0.45		
I <sub>I</sub>	All inputs	V <sub>I</sub> = 3.6 V or GND	0 V to 3.6 V	0.1			0.5	μA	
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V	0.1			0.5	μA	
ΔI <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 3.6 V	0 V to 0.2 V	0.2			0.5	μA	
I <sub>CC</sub>		V <sub>I</sub> = 3.6 V or GND, I <sub>O</sub> = 0	2.3 V to 3.6 V	0.5			0.9	μA	
ΔI <sub>CC</sub>		One input at 0.3 V or 1.1 V, Other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	2.3 V to 2.7 V				4	μA	
		One input at 0.45 V or 1.2 V, Other inputs at 0 or V <sub>CC</sub> , I <sub>O</sub> = 0	3 V to 3.6 V				12		
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	1.5				pF	
C <sub>o</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	3				pF	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V, V<sub>I</sub> = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>L</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A, B, or C	Y	5 pF	1.8	2.3	2.9	0.5	6.8	ns
			10 pF	2.3	2.8	3.4	1	7.9	
			15 pF	2.6	3.1	3.8	1	8.7	
			30 pF	3.8	4.4	5.1	1.5	10.8	



## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_I = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)  
(see [Figure 12](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	5 pF	1.8	2.3	3.1	0.5	6	ns
			10 pF	2.2	2.8	3.5	1	7.1	
			15 pF	2.6	3.2	5.2	1	7.9	
			30 pF	3.7	4.4	5.2	1.5	10	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_I = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)  
(see [Figure 12](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	5 pF	2	2.7	3.5	0.5	5.5	ns
			10 pF	2.4	3.1	3.9	1	6.5	
			15 pF	2.8	3.5	4.3	1	7.4	
			30 pF	4	4.7	5.5	1.5	9.5	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_I = 1.8\text{ V} \pm 0.15\text{ V}$  (unless otherwise noted)  
(see [Figure 12](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	5 pF	1.6	2	2.5	0.5	8	ns
			10 pF	2	2.4	2.9	1	8.5	
			15 pF	2.3	2.8	3.3	1	9.1	
			30 pF	3.4	3.9	4.4	1.5	9.8	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_I = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)  
(see [Figure 12](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	5 pF	1.6	1.9	2.4	0.5	5.3	ns
			10 pF	2	2.3	2.7	1	6.1	
			15 pF	2.3	2.7	3.1	1	6.8	
			30 pF	3.4	3.8	4.2	1.5	8.5	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_I = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)  
(see [Figure 12](#))

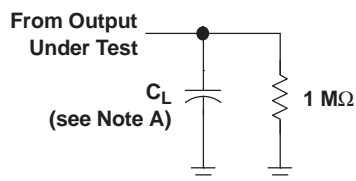
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	5 pF	1.6	2.1	2.7	0.5	4.7	ns
			10 pF	2	2.4	3	1	5.7	
			15 pF	2.3	2.7	3.3	1	6.2	
			30 pF	3.4	3.8	4.4	1.5	7.8	

## OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

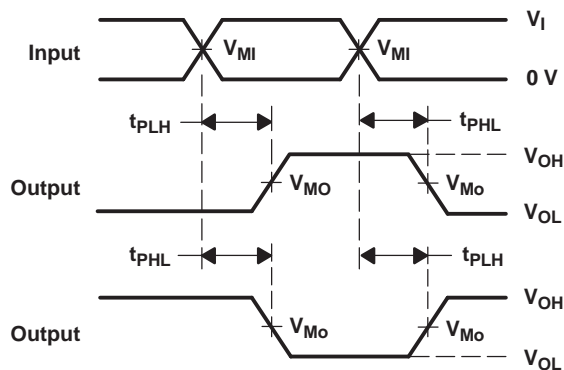
PARAMETER		TEST CONDITIONS	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	UNIT
			TYP	TYP	
$C_{pd}$	Power dissipation capacitance	$f = 10 \text{ MHz}$	4	5	pF

## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_{MI}$	$V_I/2$	$V_I/2$
$V_{MO}$	$V_{CC}/2$	$V_{CC}/2$



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ , slew rate  $\geq 1\text{ V/ns}$ .
  - C. The outputs are measured one at a time, with one transition per measurement.
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 12. Load Circuit and Voltage Waveforms**

REVISION HISTORY

Changes from Revision H (May 2010) to Revision I	Page
• Updated FUNCTION SELECTION Table. ....	<a href="#">2</a>
• Updated figure caption. ....	<a href="#">5</a>
• Updated figure caption. ....	<a href="#">5</a>

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1T98DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT6R	<a href="#">Samples</a>
SN74AUP1T98DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT6R	<a href="#">Samples</a>
SN74AUP1T98DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TKR	<a href="#">Samples</a>
SN74AUP1T98DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TKR	<a href="#">Samples</a>
SN74AUP1T98DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TK	<a href="#">Samples</a>
SN74AUP1T98DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TK	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T98DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T98DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T98DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1T98DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1T98DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP1T98DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T98DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUP1T98DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AUP1T98DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AUP1T98DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74AUP1T98DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP1T98DSFR	SON	DSF	6	5000	202.0	201.0	28.0



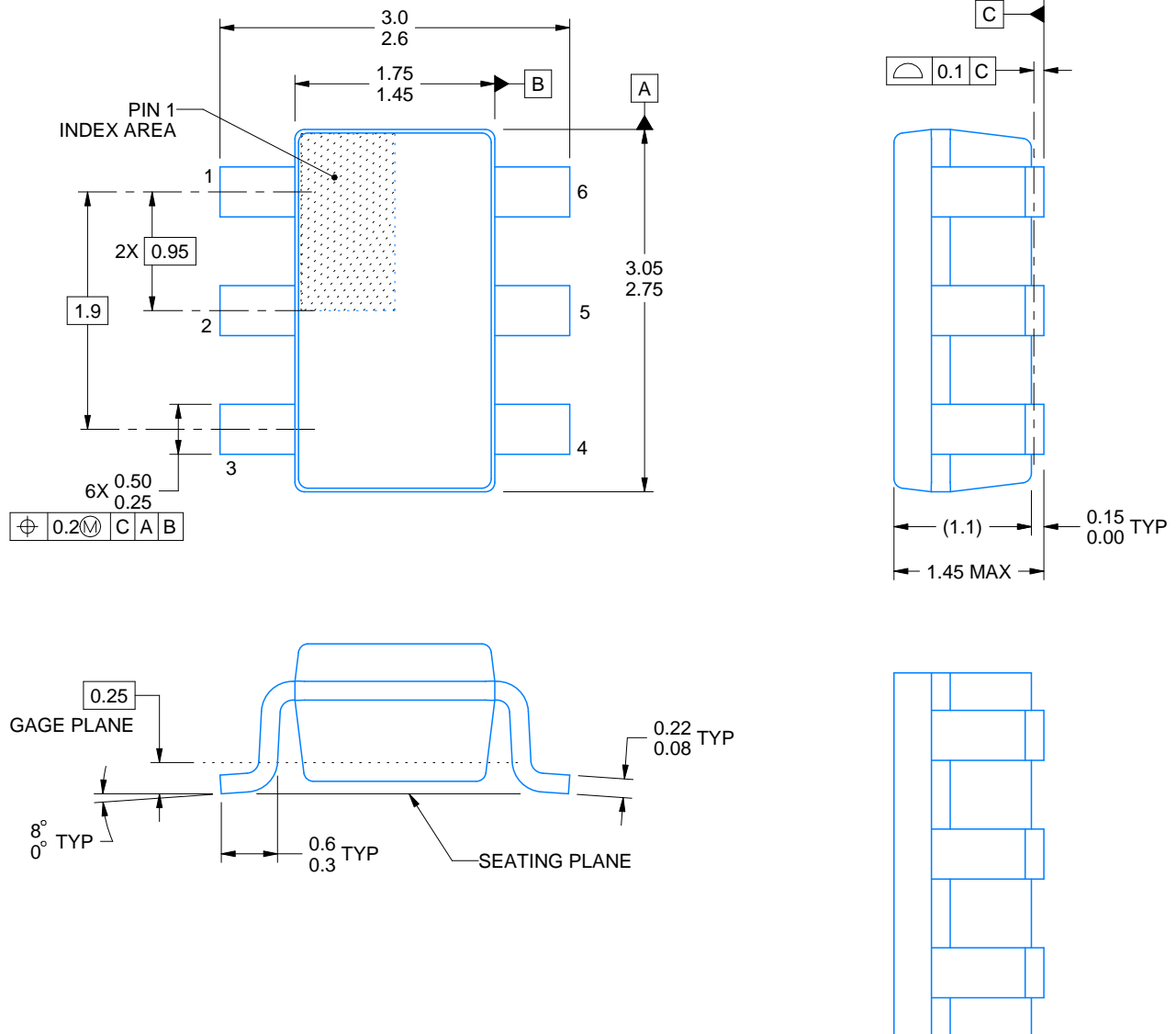
DBV0006A



## PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

4214840/E 02/2024

### NOTES:

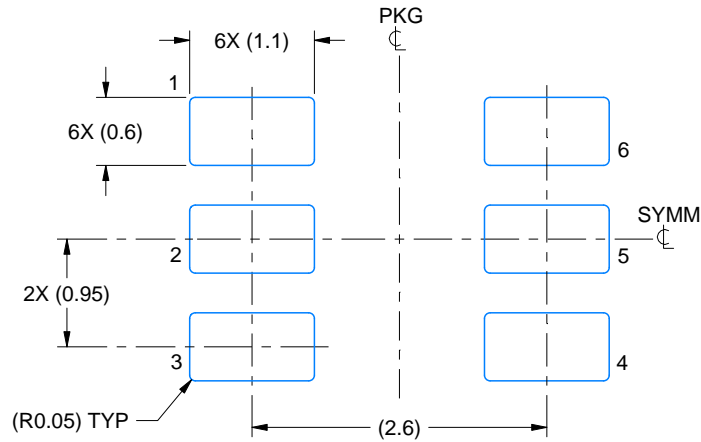
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

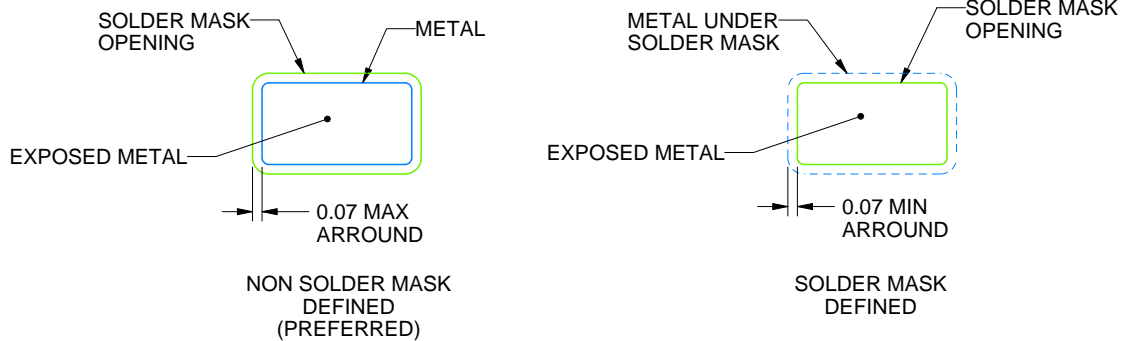
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

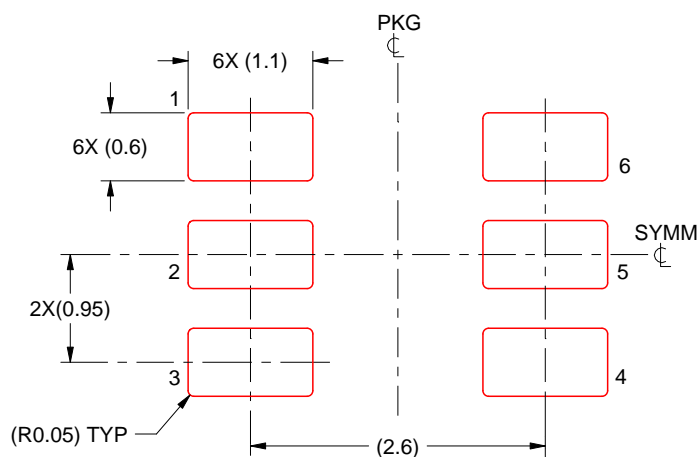
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

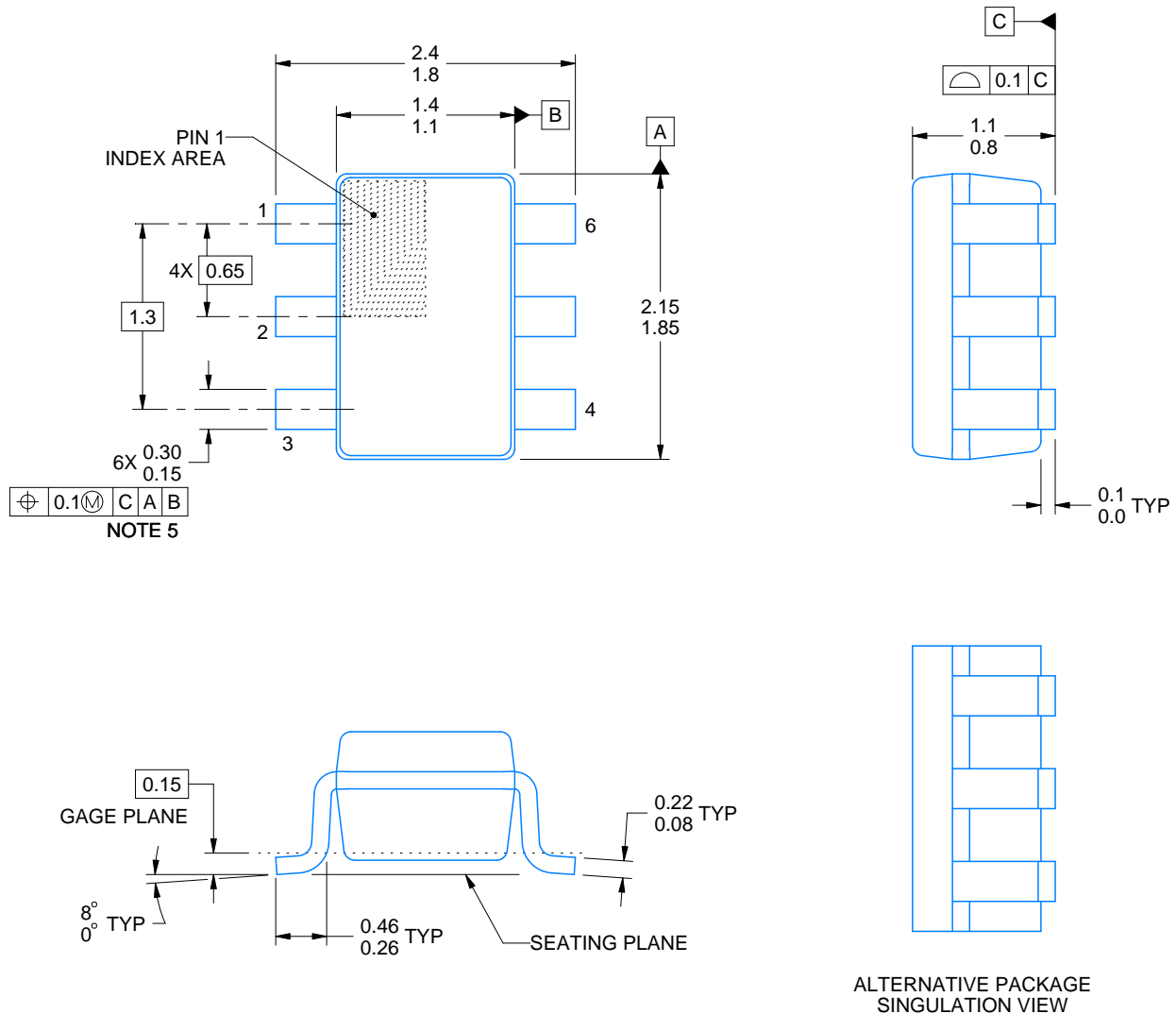


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

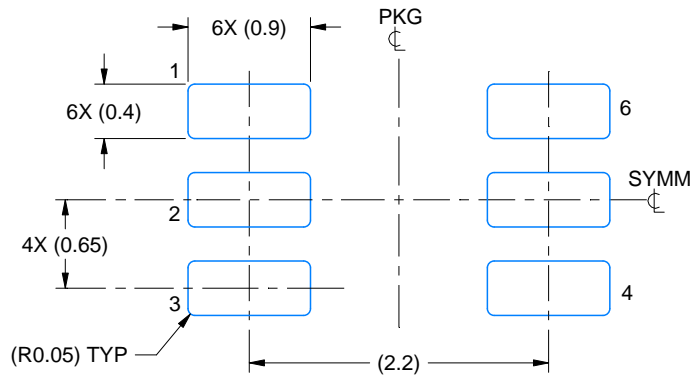
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



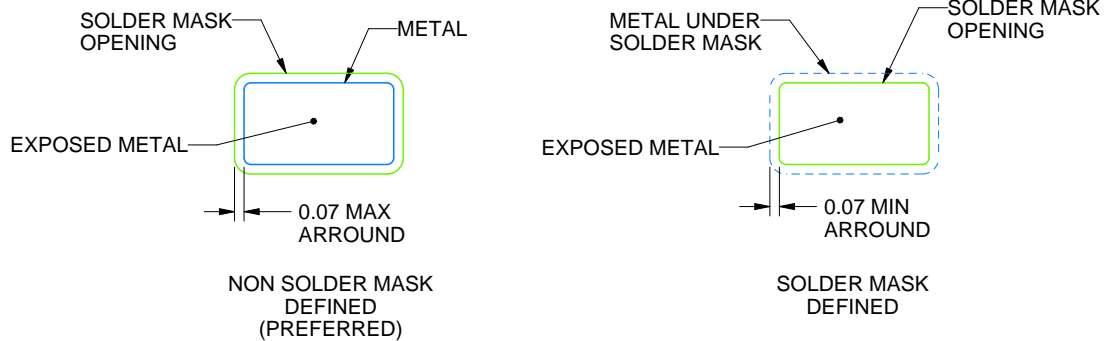
4214835/B 04/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

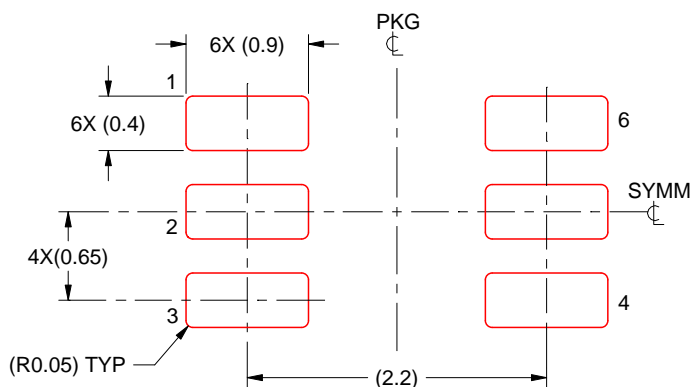


SOLDER MASK DETAILS

4214835/B 04/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 THICK STENCIL  
 SCALE:18X

4214835/B 04/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**DRY 6**

**USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G



### USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

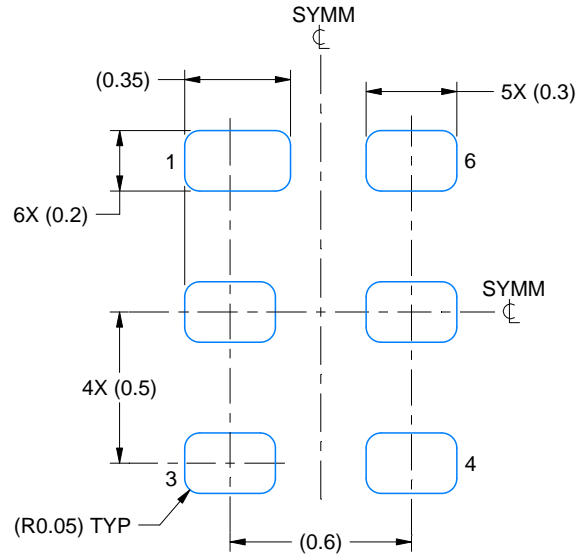


# EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**LAND PATTERN EXAMPLE**  
1:1 RATIO WITH PKG SOLDER PADS  
EXPOSED METAL SHOWN  
SCALE:40X



**SOLDER MASK DETAILS**

4222894/A 01/2018

NOTES: (continued)

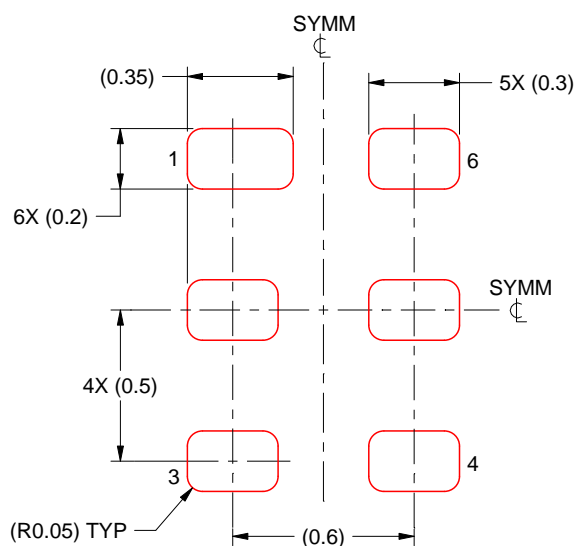
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).

## EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

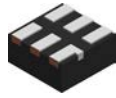


SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

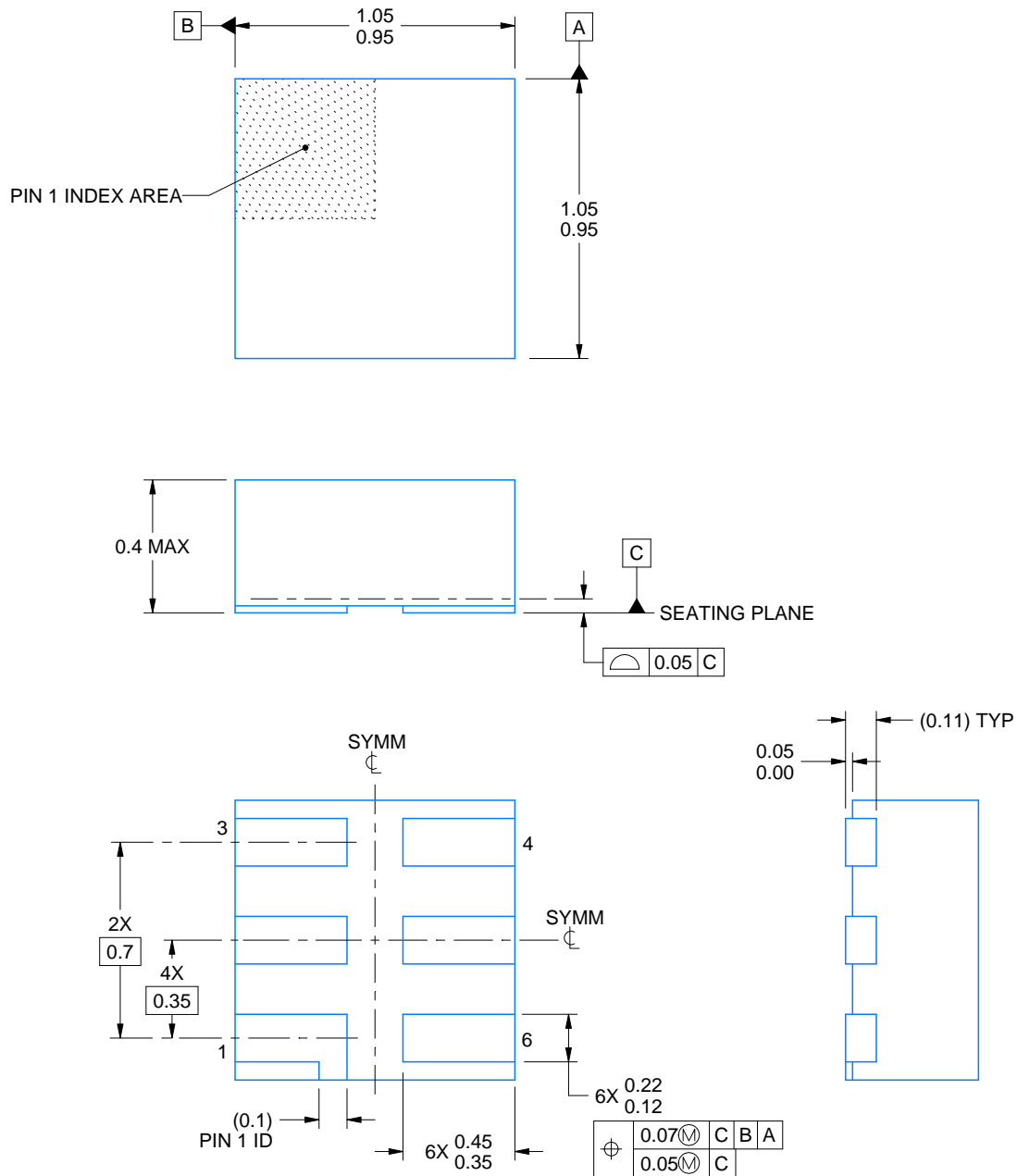


DSF0006A

## PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220597/B 06/2022

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

# EXAMPLE BOARD LAYOUT

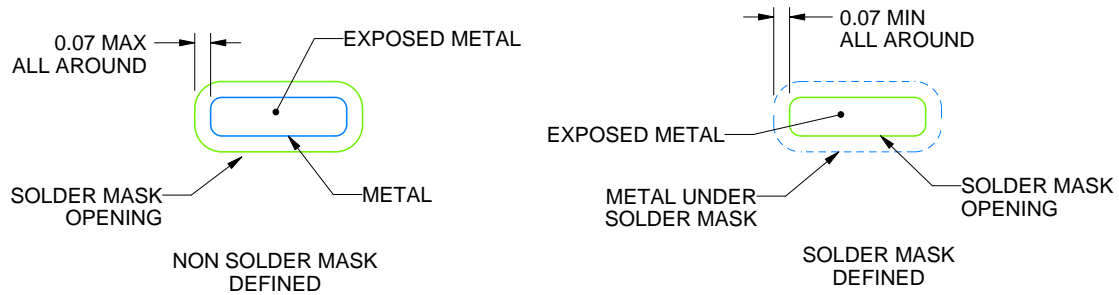
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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