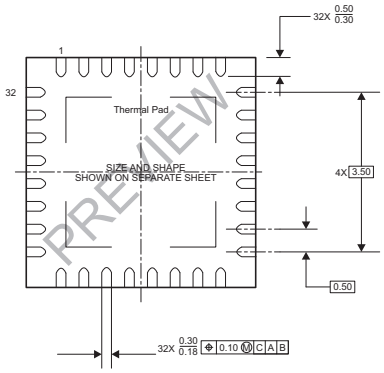
Low-Voltage 8x16 Keyboard Scanner with HID over I2C Compliant Interface

Check for Samples: TCA8424

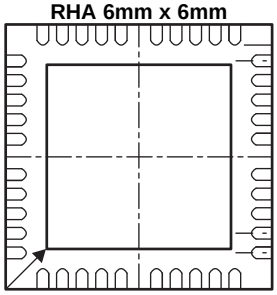
FEATURES

- **Operating Power-Supply Voltage Range of 1.65V to 3.6V**
- **Supports FM+ I2C Operation up to 1MHz**
- **Can Support up to 128 (8x16) Key Scan**
- **Internal Power-On-Reset**
- **Open Drain Open Drain Active Low INT Output**
- **Noise Filter on SCL/SDA and Inputs**
- **Open Drain Outputs Can Sink up to 12mA Current for LED**
- **Hardware Coded HID and REPORT Descriptors**
- **Available With Preprogrammed Keyboard Map**
- **Software Reset per HID Over I2C Standard**
- **Internal Pull-up Resistors Make Implementation Easy With no Need for External Components**
- **HID Over I2C Commands Supported**
  - **RESET**
  - **GET REPORT**
  - **SET REPORT**
  - **SET POWER**
- **Fixed Length 8-byte INPUT Report can Detect up to 6 Simultaneous Key Presses Excluding Modifiers (CTRL, ALT, SHIFT)**
- **INPUT Report Generated on Key Press and Release**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **1000-V Human-Body Model (A114-A)**

RHB 5mmx5mm
RSM 4mmx4mm
PREVIEW



RHA 6mm x 6mm



DESCRIPTION

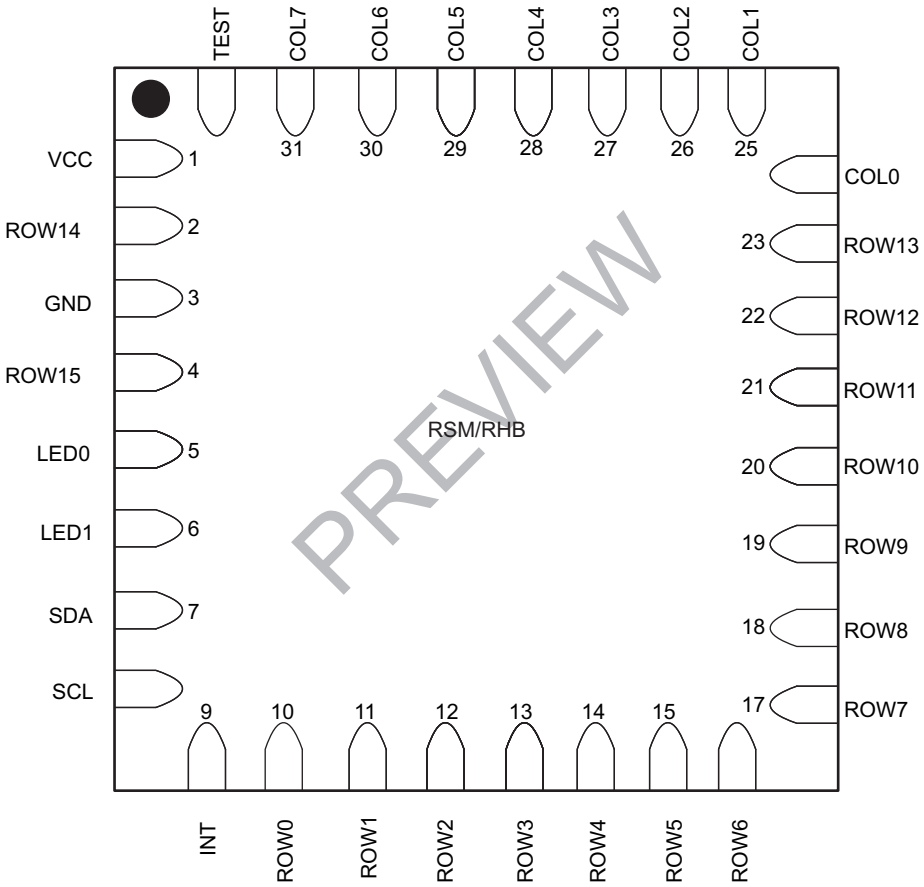
This 128 key scan device is specifically targeted towards end equipment that runs on Windows 8 operating system. The device is fully compliant with the HID over I2C specification defined (ver 1.0) defined by Microsoft. The HID and report descriptors are hard coded into the device so that they don't need to be programmed at production. The device also comes with a preprogrammed keyboard map that is compatible with most standard laptop/notebook keyboards. However, the device also available without a pre-programmed keyboard, so that any keyboard map may be written into it at production.

The device generates INPUT reports of standard 8-byte length with the 1st byte being the modifier byte. After the keyboard map is programmed into the device it automatically recognizes the row/column location of the modifier keys based on their usage code. It is capable of detecting and reporting up to six simultaneous key presses plus eight modifiers. It generates an input report on each key press and each key release.

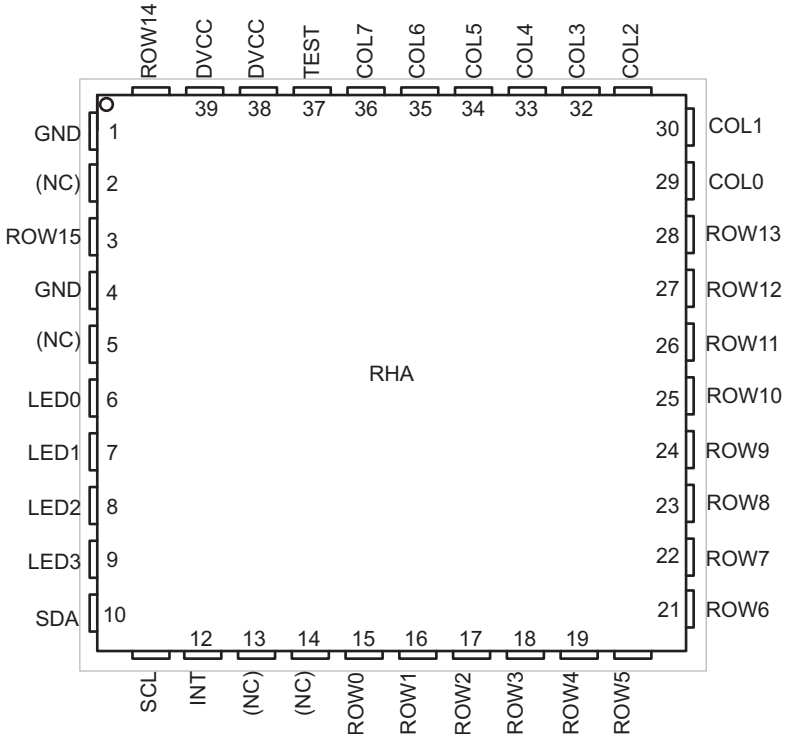
The device also supports LED indicators that are standard on a keyboard. Different variations support 2,4 or 8 LED outputs. Each output has open drain architecture and is capable of sinking up to 12mA of current. The LEDs are controlled by a standard OUTPUT report as described in the HID over I2C standard.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TOP THROUGH VIEW



TOP THROUGH VIEW

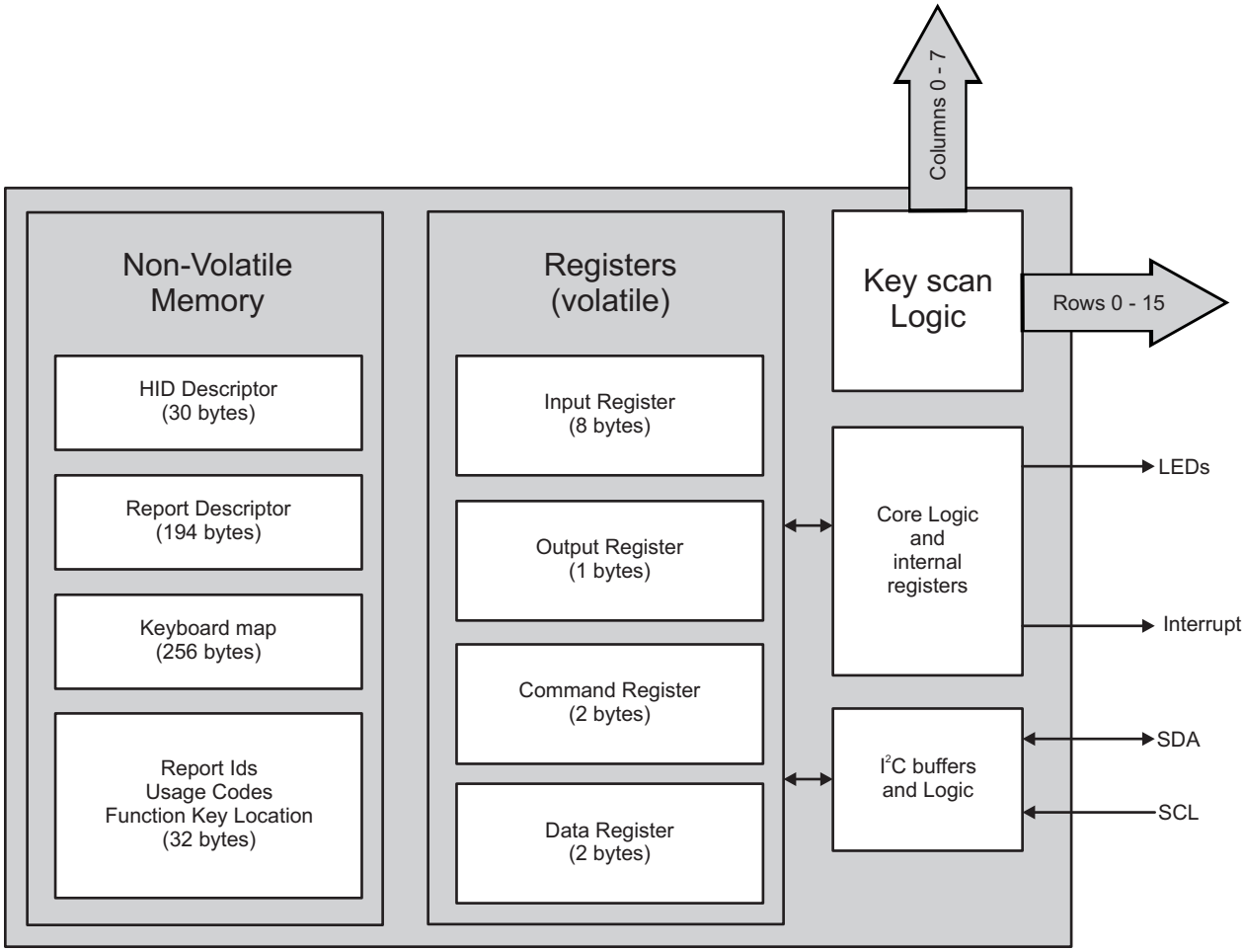


PIN FUNCTIONS

NAME	TYPE	FUNCTION
VCC	Power	Supply voltage for the device. The I2C bus should be pulled up to this rail. The key matrix IO voltages are also referenced to this supply voltage.
COL0–COL7	Input	COLs of the key matrix
ROW0–ROW15	Output	ROW of key matrix
LED0–LED7	Output	Open drain output for driving LEDs
TEST	Input	High voltage input used to program the internal memory. To be grounded in application.(1)
GND	Power	Ground
$\overline{INT}$	output	Active-low interrupt output. Connect to V_{CC} through a pull-up resistor.
SCL	Input	Serial clock bus. Connect to V_{CC} through a pull-up resistor.
SDA	I/O	Serial data bus. Connect to V_{CC} through a pull-up resistor.

(1) TEST pin must be grounded in application to ensure proper operation of device.

SIMPLIFIED BLOCK DIAGRAM



I²C INTERFACE

The bidirectional I2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to V_{CC} through a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop). A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

NOTE

Any communication to another device on the same I2C BUS must be terminated by a stop condition before communicating to the TCA8424. Any glitches below 0.7 × VCC on the SCL or SDA line should be less than 50 ns as per the I2C specification.

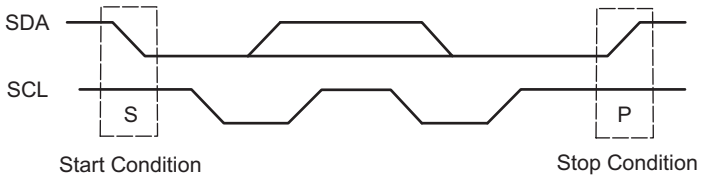


Figure 1. Definition of Start and Stop Conditions

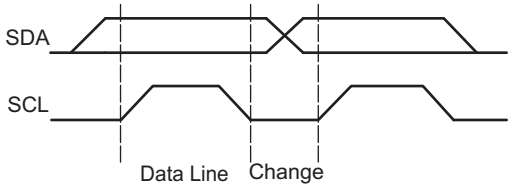


Figure 2. Bit Transfer

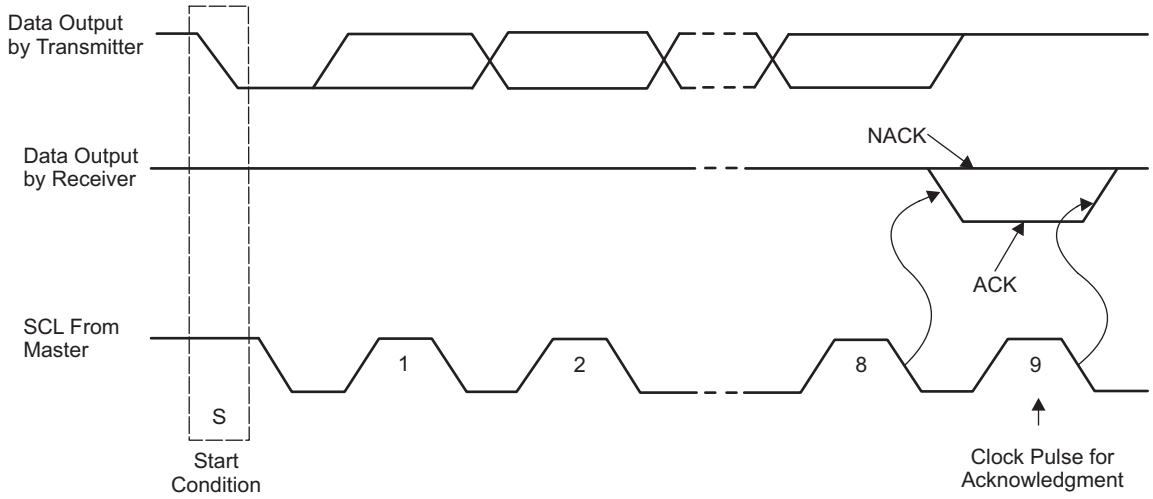


Figure 3. Acknowledgment on I²C Bus

DEVICE I²C ADDRESS

The address of the device is shown below:

Table 1. Address Reference

SLAVE ADDRESS								I2C BUS SLAVE ADDRESS
B7	B6	B5	B4	B3	B2	B1	B0	
0	1	1	1	0	1	1	0 (W)	134 (decimal), 76(h)
0	1	1	1	0	1	1	1 (R)	135 (decimal), 77(h)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation. While a low (0) selects a write operation.

Other I2C address options are available. Please contact your local TI sales person for devices with alternate I2C address.

REGISTER ADDRESS BYTE

Following the successful acknowledgment of the I2C address byte, the bus master sends two register address bytes indicating the address of the register on which the read or write operation needs to be performed. This register address is stored in an internal register and used by the device for subsequent read/write to the device. This is explained more in detail in subsequent sections of the DS.

Other I2C address options are available. Contact your local TI sales person for devices with alternate I2C address.

Table 2. Register Map

	REGISTER ADDRESS (Hex)	DESCRIPTION	POWER UP DEFAULT
HID descriptor	0000h-001Dh	HID descriptor	See section on HID descriptor
Report Descriptor	0030h-00F1h	Report descriptor	See section on Report descriptor
Keyboard Map	0100h-01FFh	keyboard Map	see section on Keyboard map
Function Key location (1)	0201h	Function Key location on Keyboard Map (2)	0
Default Report ID	0202h	Default Report ID	1
Report ID1	0203h	Report ID1	2
Report ID2	0204h	Report ID2	3
Report ID3	0205h	Report ID3	4
Report ID4	0206h	Report ID4	5
Report ID1 usage IDs	0207h-020Eh	Usage IDs associated with ReportID1	A7 – AE
Report ID2 usage IDs	020Fh-0216h	Usage IDs associated with ReportID2	AF – B6
Report ID3 usage IDs	0217h-021Eh	Usage IDs associated with ReportID3	B7 – BA
Report ID4 usage IDs	021Fh-0226h	Usage IDs associated with ReportID4	BB – BE
Input report	0400h	input report length (LSB)	00h
	0401h	input report length (MSB)	00h
	0402h	Report ID	A2
	0403h	modifier byte	00h
	0404h	reserved	reserved
	0405h	usage code 1	00h
	0406h	usage code 2	00h
	0407h	usage code 3	00h
	0408h	usage code 4	00h
	0409h	usage code 5	00h
	040Ah	usage code 6	00h
Output report	0500h	LED status	00h
Command register	0600h	HID over I2C Command low byte	00h
	0601h	HID over I2C Command high byte	00h
Data register	0700-070Ah	Data for HID over I2C command	00h

(1) Function Key Usage ID in keyboard map must be non-zero
(2) Column/Row intersection of function key. i.e. col3 row4 intersection would read 34h

Table 2. Register Map (continued)

	REGISTER ADDRESS (Hex)	DESCRIPTION	POWER UP DEFAULT
HID Descriptor[3] (0000h-001Dh)	0000h[3]	HID Descriptor length	40h
	0001h		41h
	0002h	BCD version	42h
	0003h		43h
	0004h	Report descriptor length	44h
	0005h		45h
	0006h	Report Descriptor Register address	46h
	0007h		47h
	0008h	Input register address	48h
	0009h		49h
	000Ah	max input report length (including 2 bytes length field)	4Ah
	000Bh		4Bh
	000Ch	Output register address	4Ch
	000Dh		4Dh
	000Eh	max output report length (including 2 bytes length field)	4Eh
	000Fh		4Fh
	0010h	Command register address	50h
	0011h		51h
	0012h	data register address	52h
	0013h		53h
	0014h	Vendor ID	54h
	0015h		55h
	0016h	Product ID	56h
	0017h		57h
	0018h	Version ID	58h
	0019h		59h
	001Ah	Reserved per HID over I2C spec v0.91	5Ah
	001Bh		5Bh
	001Ch		5Ch
	001Dh		5Dh
			5Eh

(3) **The Hid descriptor start address must be 0000h**

HID DESCRIPTOR RETRIEVAL

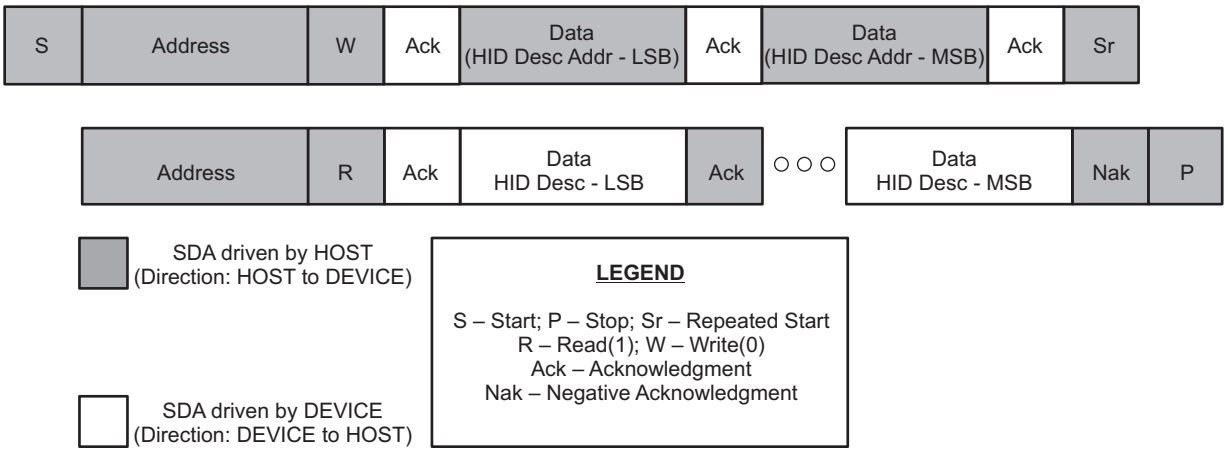


Figure 4. Typical Retrieval of the HID Descriptor

Figure 4 shows the typical retrieval of the HID descriptor. This is the most common way the HID descriptor is retrieved. However, the TCA8424 allows partial retrieval of the descriptor as described in the HID over I2C spec rev 1.0.

Table 3. Report Descriptor

	Register Address	Power up Default
Report(1) descriptor (0030h-00F1h)	30	5F
	31	60
	32	61
	33	62
	34	63
	35	64
	36	65
	37	66
	38	67
	39	68
	3A	69
	3B	6A
	3C	6B
	3D	6C
	3E	6D
	3F	6E
	40	6F
	41	70
	42	71
	43	72
	44	73
	45	74
	46	75
	47	76
	48	77

(1) Report descriptor contents may vary depending on version of device. Please contact TI for device for different Report Descriptor contents

Table 3. Report Descriptor (continued)

	Register Address	Power up Default
Report descriptor (0030h-00F1h)	49	78
	4A	79
	4B	7A
	4C	7B
	4D	7C
	4E	7D
	4F	7E
	50	7F
	51	80
	52	81
	53	82
	54	83
	55	84
	56	85
	57	86
	58	87
	59	88
	5A	89
	5B	8A
	5C	8B
	5D	8C
	5E	8D
	5F	8E
	60	8F
	61	90
	62	91
	63	92
	64	93
	65	94
	66	95
	67	96
	68	97
	69	98
	6A	99
	6B	9A
	6C	9B
	6D	9C
	6E	9D
	6F	9E
	70	9F
	71	A0
	72	A1
	73	A2
	74	A3
	75	A4
	76	A5

Table 3. Report Descriptor (continued)

	Register Address	Power up Default
Report descriptor (0030h-00F1h)	77	A6
	78	A7
	79	A8
	7A	A9
	7B	AA
	7C	AB
	7D	AC
	7E	AD
	7F	AE
	80	AF
	81	B0
	82	B1
	83	B2
	84	B3
	85	B4
	86	B5
	87	B6
	88	B7
	89	B8
	8A	B9
	8B	BA
	8C	BB
	8D	BC
	8E	BD
	8F	BE
	90	BF
	91	C0
	92	C1
	93	C2
	94	C3
	95	C4
	96	C5
	97	C6
	98	C7
	99	C8
	9A	C9
	9B	CA
	9C	CB
	9D	CC
	9E	CD
	9F	CE
	A0	CF
	A1	D0
	A2	D1
	A3	D2
	A4	D3
	A5	D4

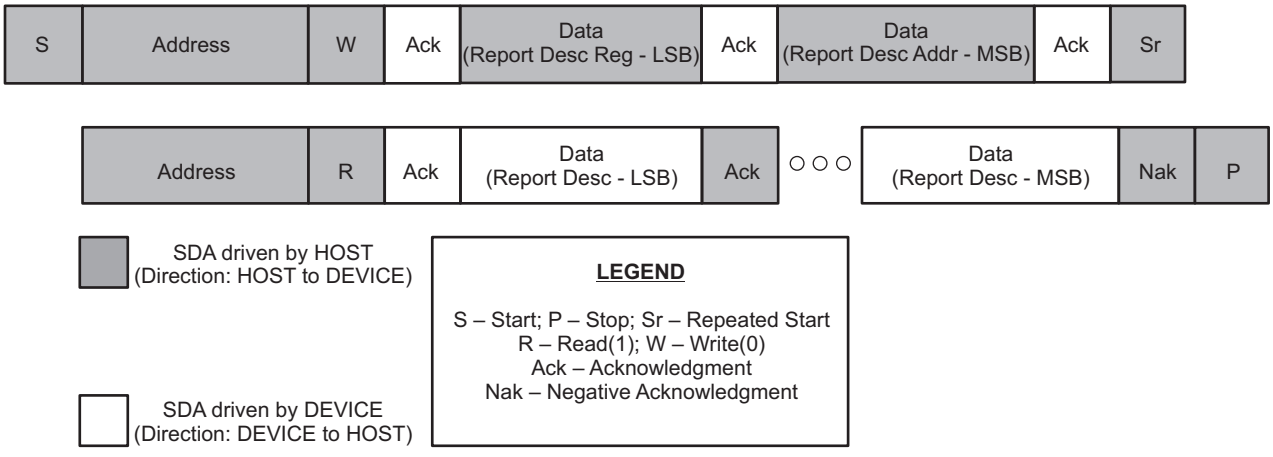
Table 3. Report Descriptor (continued)

	Register Address	Power up Default
Report descriptor (0030h-00F1h)	A6	D5
	A7	D6
	A8	D7
	A9	D8
	AA	D9
	AB	DA
	AC	DB
	AD	DC
	AE	DD
	AF	DE
	B0	DF
	B1	E0
	B2	E1
	B3	E2
	B4	E3
	B5	E4
	B6	E5
	B7	E6
	B8	E7
	B9	E8
	BA	E9
	BB	EA
	BC	EB
	BD	EC
	BE	ED
	BF	EE
	C0	EF
	C1	F0
	C2	F1
	C3	F2
	C4	F3
	C5	F4
	C6	F5
	C7	F6
	C8	F7
	C9	F8
	CA	F9
	CB	FA
	CC	FB
	CD	FC
	CE	FD
	CF	FE
	D0	FF
	D1	0
	D2	1
	D3	2
	D4	3

Table 3. Report Descriptor (continued)

	Register Address	Power up Default
Report descriptor (0030h-00F1h)	D5	4
	D6	5
	D7	6
	D8	7
	D9	8
	DA	9
	DB	0A
	DC	0B
	DD	0C
	DE	0D
	DF	0E
	E0	0F
	E1	10
	E2	11
	E3	12
	E4	13
	E5	14
	E6	15
	E7	16
	E8	17
	E9	18
	EA	19
	EB	1A
	EC	1B
	ED	1C
	EE	1D
	EF	1E
	F0	1F

REPORT DESCRIPTOR RETREIVAL



INPUT REPORT

Input reports are used to communicate key presses and releases to the host controller. The TCA8424 is capable of communicating up to six simultaneous key presses and up to eight modifier keys. The standard modifier keys recognized by the TCA8424 are (Usage ID based on HID usage tables ver 1.11). The usage ID for each key is stored in the keyboard map section of NV memory.

- Left Ctrl (Usage ID – E0)
- Left shift (Usage ID – E1)
- Left Alt (Usage ID – E2)
- Left GUI (Usage ID – E3)
- Right Ctrl (Usage ID – E4)
- Right shift (Usage ID – E5)
- Right Alt (Usage ID – E6)
- Right GUI (Usage ID – E7)

Below is that format of a standard input report. The first two bytes are data length field indicating the length of input report.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	1	0	1	1
1	0	0	0	0	0	0	0	0
2	Report ID							
3	RightGUI	RightAlt	RightShift	RightCtrl	LeftGUI	LeftAlt	LeftShift	LeftCtrl
4	Reserved							
5	Key1 Usage ID							
6	Key2 Usage ID							
7	Key3 Usage ID							
8	Key4 Usage ID							
9	Key5 Usage ID							
10	Key6 Usage ID							

An input report is generated for every key press and also on every key release. If no keys are pressed after a key release then the report contains all zeroes except for the Data length field (first two bytes) and the Report ID. Input reports are also generated if only modifier keys are pressed (not accompanied by any other key). The data length field (first two bytes) for a standard key press is always 11.

SPECIAL MODIFIER (Fn key) AND ALTERNATE REPORT IDs

Other than the standard modifiers, the TCA8424 also supports one special modifier such as the function (FN) key. This operates different from the other modifier keys in that, it is not represented in the modifier byte of the input report. The TCA8424 only supports a single key press in combination with the FN key.

When the FN key is pressed the TCA8424 generates a default input report indicating that all keys have been released. A FN key release will generate an input report with the current Report ID and cleared usage codes. The TCA8424 only supports a single key press in combination with the FN key. Any key pressed after the FN key that does not have a non-zero Usage ID will be ignored. Once the FN key is pressed and a key that has an Usage ID in the alternate keyboard map has been pressed, additional key presses will be ignored until either the FN key is released or the second key that had an Usage ID in the alternate keyboard map is released.

In addition to standard function keys, many keyboards support special functions such as volume up, volume down, skip track, previous track etc. Report IDs are used as a way for the host processor to identify whether the usage ID corresponds to a standard function key or a special function key. The TCA8424 supports Five different report IDs. **Report IDs must be non-zero.**

1. Default Report ID – located at address 0202h. This ID is populated in the input report when there is a normal key press or a regular function key.
2. Report ID 1 – located at address 0203h. This ID is populated in the report when the Usage ID of the key press detected by the TCA8424 corresponds to a usage ID located in the memory range (0207h-020Eh)
3. Report ID 2 – located at address 0204h. This ID is populated in the report when the Usage ID of the key

press detected by the TCA8424 corresponds to a usage ID located in the memory range (020Fh-0216h)

4. Report ID 3 – located at address 0204h. This ID is populated in the report when the Usage ID of the key press detected by the TCA8424 corresponds to a usage ID located in the memory range (0217h-021Eh)
5. Report ID 4 – located at address 0204h. This ID is populated in the report when the Usage ID of the key press detected by the TCA8424 corresponds to a usage ID located in the memory range (021Fh-0226h)

As can be inferred from the above description, whenever a key press is detected, the TCA8424 looks up the usage ID from the alternate keyboard map and then compares this usage ID with the usage IDs corresponding to Report ID 1, Report ID 2, Report ID 3, and Report ID 4. If there is a match, then corresponding report ID is populated in the special input report. If not the default input report is used with the default Report ID. (1)

Below is the format of the special input report. The format is similar to the bit field representation used to represent the modifier byte in the standard input report. Usage ID byte location 0 will correspond to the first Usage ID in memory for the respective Report ID (2) and descend with Usage ID byte location 7 corresponding to the last Usage ID in memory.(2)

Table 4. Special Input Report

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0
2	Report ID							
3	Usage ID byte location 7	Usage ID byte location 6	Usage ID byte location 5	Usage ID byte location 4	Usage ID byte location 3	Usage ID byte location2	Usage ID byte location1	Usage ID byte location 0

(1) The last 5 key Usage IDs in the input report and the modifier byte will always read 00h when the function key is pressed in addition to another key.
(2) For Report ID1: Usage ID byte location 0 corresponds to memory location 0207h. Usage ID byte location 7 corresponds to memory location 020Eh.

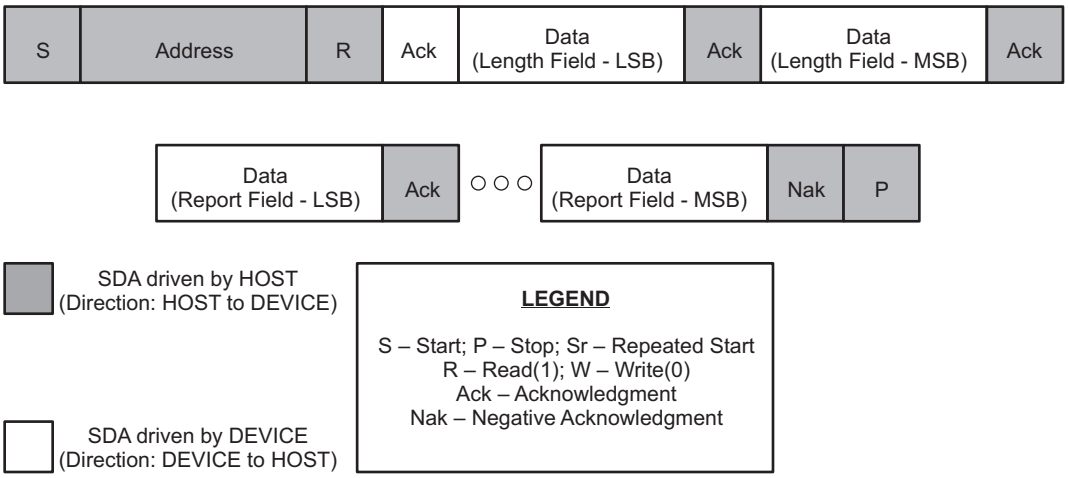


Figure 5. Input Report Retrieval

It is important to note that, unlike retrieval of other reports, where the first I2C transaction is a write, in the case of input report the first transaction itself is a read operation as indicated by Bit 8 of the I2C address.

OUTPUT REPORT

Output reports are used by the host to turn ON/OFF any indicator LEDs (caps lock, num lock etc.) on the keyboard. The TCA8424 can support from 2 to 4 LED indicators depending on the version of the device chosen. The output reports are single byte reports (8-bit) where each bit indicates the status of the corresponding LED. A '1' indicates that the LED is turned on where as a '0' turns off the LED. Below is the format of the output report received from the host. Just as in the case of the input report the first two bytes indicate the length of the output report.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	1	1
1	0	0	0	0	0	0	0	0
2	Reserved	Reserved	Reserved	Reserved	LED3	LED2	LED1	LED0

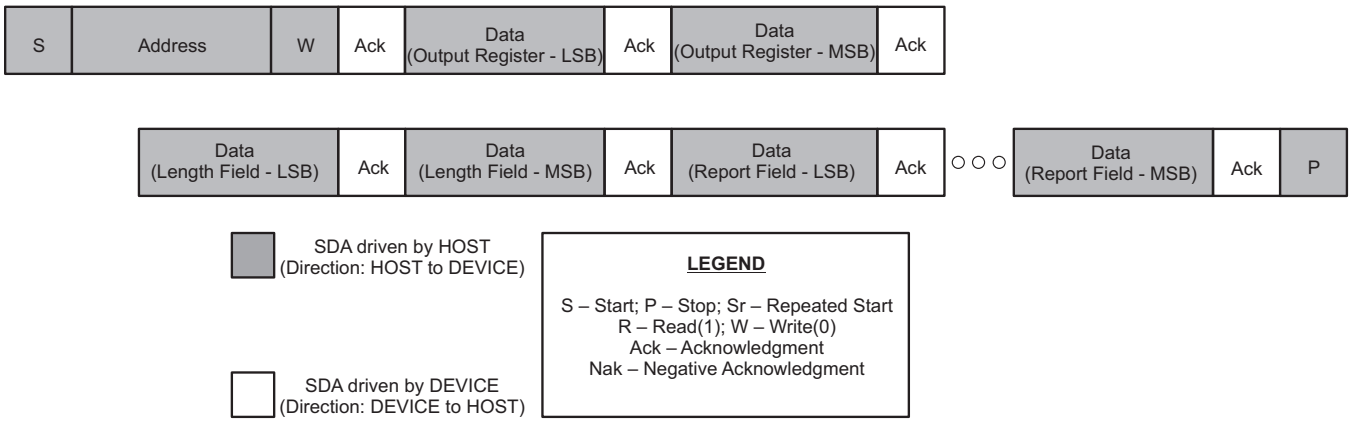


Figure 6. Output Report Retrieval

COMMAND and DATA REGISTER

The HID over I2C spec requires that all devices respond to certain commands. The commands are issued to the command register. The command is an opcode as defined by the HID over I2C spec. The operand for the command goes to the data register. Below is a list of commands supported by the TCA8424.

Op Code	Command Name	Effect on Device
0001b	RESET	Device is reset and all registers are returned to default value. This command has the same effect on the device as a power on reset.
0010b	GET_REPORT	Most recent input report is transferred to Data Register
0011b	SET_REPORT	Data register contents are used to turn on/off LED.
1000b	SET_POWER	All LEDs are turned off and device is in lowest current mode (will still detect key presses)

The I2C transactions used to issue these commands are exactly as described in the HID over I2C standard.

RESET

After receiving the RESET command, the device will go through a full power on reset and all registers are loaded with their default values. The TCA8424 takes ~600µs to reset and during this time all I2C traffic will be ignored by the device. After coming out of reset, the data length field in the input report is populated with 0000h and the INT signal is asserted.

GET_REPORT

The GET_REPORT command will retrieve the current input report from the device but will not clear the interrupt asserted from a key press or release.

SET_REPORT

The SET_REPORT command is used to set the contents of the output report. The Data shall be packaged with the length field as 0x0003, and the third byte shall describe the LED outputs as defined in the report descriptor.

SET_POWER

The SET_POWER=SLEEP command will turn off all the LED outputs and clear the input report including report ID and length field. If a key is pressed when SET_POWER=SLEEP command is received, keyscan will stop when the command is received. TCA8424 will wait for all keys to be released before any subsequent key press will assert an interrupt. If a key is pressed and not released while device is asleep and the SET_POWER=WAKE command is received, the key scanner will start and assert an interrupt that a key has been pressed. The SET_POWER=WAKE command is received the LED outputs will be returned to the state they were before the SET_POWER=SLEEP was received. If a command to change the output report is received during sleep, the LED status will indicate that of the last output report received upon SET_POWER=WAKE.

If keys are pressed while the device is entering sleep mode, a read of the input report or use of the GET_REPORT command before all keys are released, may not reflect the current state of the keyboard. Any key presses that happen after all keys are released will populate the input report and assert INT.

KEYBOARD MAP

The Non volatile memory contains a section that contains the keyboard map. Each byte location in the keyboard map, is mapped to a specific row column intersection on the key matrix, and contains the usage ID of the key located in that row column intersection. The keyboard map consists of two sections. Each row column intersection is mapped to one location in each section. The primary section contains the usage ID of the key and the alternate section contains the alternate usage ID of the key that will be reported when the special modifier (FN) is used. Only keys with non-zero usage codes will be recognized, **including the function key**.

The device is available with some pre defined keyboard maps. It is also available with the keyboard map not programmed so that the end user may program the keyboard map based on the keyboard being used. Alternately you may contact TI for custom variations of the part with different keyboard maps programmed by special request.

The table below illustrates the column-row intersections and the memory locations they are mapped to.

KEYBOARD MAP (PRIMARY)								
	C0	C1	C2	C3	C4	C5	C6	C7
R0	A1	B1	C1	D1	E1	F1	81	91
R1	A2	B2	C2	D2	E2	F2	82	92
R2	A3	B3	C3	D3	E3	F3	83	93
R3	A4	B4	C4	D4	E4	F4	84	94
R4	A5	B5	C5	D5	E5	F5	85	95
R5	A6	B6	C6	D6	E6	F6	86	96
R6	A7	B7	C7	D7	E7	F7	87	97
R7	A8	B8	C8	D8	E8	F8	88	98
R8	A9	B9	C9	D9	E9	F9	89	99
R9	AA	BA	CA	DA	EA	FA	8A	9A
R10	AB	BB	CB	DB	EB	FB	8B	9B
R11	AC	BC	CC	DC	EC	FC	8C	9C
R12	AD	BD	CD	DD	ED	FD	8D	9D
R13	AE	BE	CE	DE	EE	FE	8E	9E
R14	AF	BF	CF	DF	EF	FF	8F	9F
R15	B0	C0	D0	E0	F0	80	90	A0

KEYBOARD MAP (SECONDARY)								
	C0	C1	C2	C3	C4	C5	C6	C7
R0	A1	B1	C1	D1	E1	F1	81	91
R1	A2	B2	C2	D2	E2	F2	82	92
R2	A3	B3	C3	D3	E3	F3	83	93
R3	A4	B4	C4	D4	E4	F4	84	94
R4	A5	B5	C5	D5	E5	F5	85	95
R5	A6	B6	C6	D6	E6	F6	86	96
R6	A7	B7	C7	D7	E7	F7	87	97
R7	A8	B8	C8	D8	E8	F8	88	98
R8	A9	B9	C9	D9	E9	F9	89	99
R9	AA	BA	CA	DA	EA	FA	8A	9A
R10	AB	BB	CB	DB	EB	FB	8B	9B
R11	AC	BC	CC	DC	EC	FC	8C	9C
R12	AD	BD	CD	DD	ED	FD	8D	9D
R13	AE	BE	CE	DE	EE	FE	8E	9E
R14	AF	BF	CF	DF	EF	FF	8F	9F
R15	B0	C0	D0	E0	F0	80	90	A0

KEYSCAN LOGIC

Functional Overview

Upon power up or when coming out of RESET, the devices initializes itself with all the registers having the power up default value. All the COLx pins are pulled up to V_{CC} by internal pull up resistors. All the ROWx pins are pulled low. The device is now in idle/standby mode (lowest power state). When any key is pressed, one of the COL pins gets connected to one of the ROW pins, thereby pulling down the corresponding COL pin. This initiates the keyscan.

When this occurs the internal oscillator turns on, and each ROWx pin goes low, one after the other, for approximately 800uS while the COLx inputs are sampled at each step. Then, for every key that is pressed, the corresponding usage ID from the keyboard map is registered. After approximately 25mS, the scan will repeat. If any previously pressed key is still pressed, then the corresponding code is written to the Input register. The scan continues to repeat as long as there are keys pressed. Now, when a previously pressed key is released another input report is generated with the keys that are still pressed, or if no keys are pressed, then an input report with all zero Usage codes is reported.

Once the input report has been populated into the input register, the $\overline{INT}$ is asserted to indicate to the host that an input report is now available.

Interrupt ($\overline{INT}$) Output

An interrupt is generated when the device has an input report ready for the HOST to read. Resetting the interrupt is achieved by reading the INPUT Register. Using the GET_REPORT command will not clear the interrupt. The interrupt will clear after the 2nd read byte of the empty input report on reset. After reset, a default input report read will clear the input report after the last byte is read. If a special input report is read, the interrupt clears after the 4^{th} byte is read.

The interrupt status is updated in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit following the rising edge of the SCL signal after the last byte of the input report has been read. The INPUT register will keep getting updated with the most recent key press reports even while the $\overline{INT}$ signal stays asserted. In order avoid missing of key presses it is recommended that host processor respond to interrupt service request in <50ms (debounce time)

The $\overline{INT}$ output has an open-drain structure and requires a pull-up resistor to V_{CC}. When the device comes out of power on reset, the /INT signal is asserted to indicate to the host that the device has come out of reset (as required by the HID over I2C). The value in the data length field of the input report is set to 0000h when the device comes out of POR (as required by the HID over I2C).

Power-On Reset

When power (from 0V) is applied to V_{CCP}, an internal power-on reset holds the TCA8424 in a reset condition until V_{CCP} has reached V_{POR}. At that time, the reset condition is released, and the TCA8424 registers and I2C state machine initialize to their default states. After that, V_{CCP} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle.

- During power up, if V_{CCI} ramps before V_{CCP}, a power on reset event occurs and the I^2C registers are reset.
- If V_{CCP} ramps up before V_{CCI}, then the device with reset as if $\overline{RESET}$ = 0
- The device is reset regardless of which V_{CCx} ramps first.

Power-On Reset Requirements

In the event of a glitch or data corruption, TCA8424 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 7 and Figure 8.

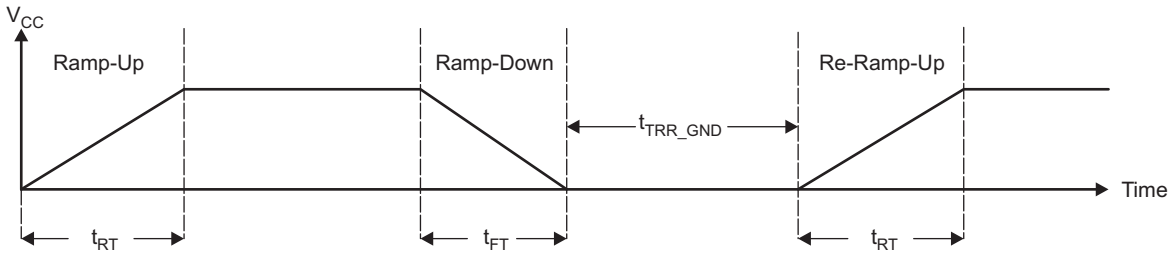


Figure 7. V_{CC} is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}

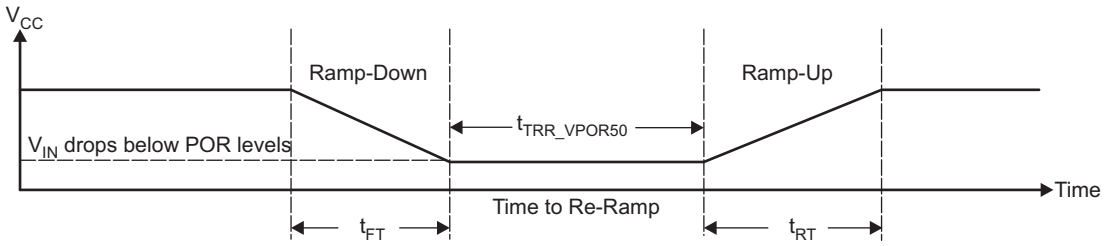


Figure 8. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (t_{GW}) and height (t_{GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 9 provides more information on how to measure these specifications.

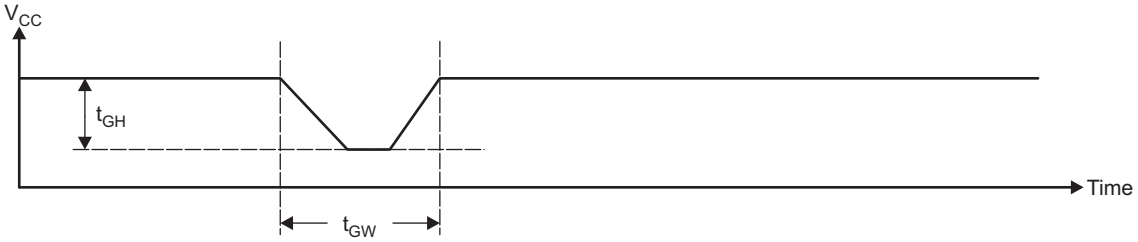


Figure 9. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 10 provides more details on this specification.

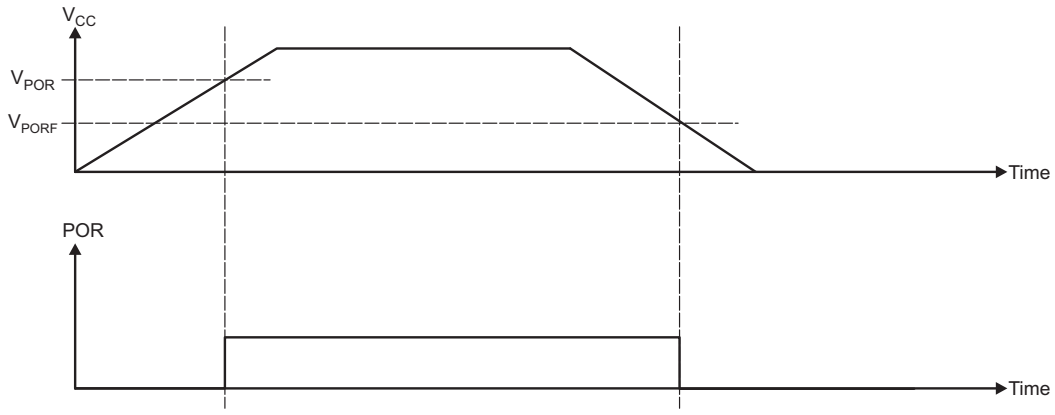


Figure 10. V_{POR}

The table below specifies the performance of the power-on reset feature for TCA8424 for both types of power-on reset.

RECOMMENDED SUPPLY SEQUENCING AND RAMP RATES AT T_A = 25°C(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
t_{FT}	Fall rate	1		100	ms
t_{RT}	Rise rate	0.1		100	ms
t_{RR_GND}	Time to re-ramp (when V_{CC} drops to GND)	40			µs
t_{RR_POR50}	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	40			µs
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 µs			1.2	V
t_{GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}			10	µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}	0.86		1.22	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}	1.1		1.34	V

(1) Not tested. Specified by design

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CCI}	Supply voltage range			–0.3	4	V
V_I	Input voltage range			–0.3	4	V
V_{ILED}	Input voltage range LED outputs			–0.3	5.5	V
V_{ITEST}	Input voltage range test pin				7.7	V
I_{IK}	Input clamp current	SCL	V_I < 0		±10	mA
I_{OK}	Output clamp current	INT	V_O < 0		±10	mA
I_{IOK}	Input/output clamp current	SDA	V_O < 0 or V_O > V_{CC}		±10	mA
I_{OL}	Continuous output low current	SDA	V_O = 0		±30	mA
		$\overline{INT}$	V_O = 0		±10	mA
		LEDx	V_O = 0		±20	mA
T_{stg}	Storage temperature range			–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCI}	Supply voltage		1.65	3.6	V
V_{test}	Voltage on test pin	During normal operation (in application)	GND	GND	V
V_{ILED}	Voltage on LED output			5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CCI}	3.6	V
V_{IL}	Low-level input voltage	SCL, SDA	–0.3	0.3 × V_{CCI}	V
I_{OL}	Low-level output current	SDA		20	mA
		$\overline{INT}$		3	mA
		LEDx		12	mA
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

All values are specified at 25°C operating temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	1.65 V to 3.6 V	–1.2			V
V_{OL}	ROWx, $\overline{INT}$	I_{OL} = 3 mA	1.65 V			0.4	V
			1.8 V			0.4	
			2.5 V			0.4	
			3.3 V			0.4	
			3.6 V			0.4	
	SDA	I_{OL} = 20 mA	1.65 V			0.4	V
			1.8 V			0.4	
			2.5 V			0.4	
			3.3 V			0.4	
			3.6 V			0.4	
V_{OL}	LEDx	I_{OL} = 12 mA	1.8 V			0.4	V
			3.3 V			0.4	
			5 V			0.4	
I_{OL}	LEDx	V_{OL} = 0.4 V	1.65 V – 5.5 V	12			mA
R int	Internal pull up resistance			80	100	120	kΩ
I_{ccsh0}	Current consumption	Fscl = 0 kHz, oscillator off	1.65 V		0.25	8	µA
			1.8 V		0.27	8	
			2.5 V		0.4	12	
			3.3 V		0.54	16	
			3.6 V		0.6	20	
$I_{cc4khz1}$	Current consumption	Fscl = 400 kHz, oscillator on	1.65 V		17	18	µA
			1.8 V		18	20	
			2.5 V		25	30	
			3.3 V		33	40	
			3.6 V		39	50	
$I_{cc1Mhz1}$	Current consumption	Fscl = 1 MHz, oscillator on	1.65 V		36	40	µA
			1.8 V		39	50	
			2.5 V		48	60	
			3.3 V		65	70	
			3.6 V		60	80	
ΔIcc	Incremental current for duration of key press	One key pressed	1.65 V – 3.6 V		39	45	µA
Cin	SCL, SDA				5	10	pF

I²C INTERFACE TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

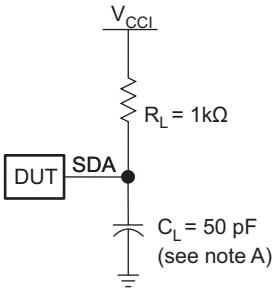
PARAMETER		STANDARD MODE I²C BUS		FAST MODE I²C BUS		FAST MODE PLUS (FM+) I²C BUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency	0	100	0	400	0	1000	kHz
t_{sch}	I²C clock high time	4		0.6		0.26		µs
t_{scl}	I²C clock low time	4.7		1.3		0.5		µs
t_{sp}	I²C spike time		50		50		50	ns
t_{sds}	I²C serial data setup time	250		100		50		ns
t_{sdh}	I²C serial data hold time	0		0		0		ns
t_{icr}	I2C input rise time		1000	20	300		120	ns
t_{icf}	I²C input fall time		300	20 x (V_{DD}/ 5.5 V)	300	20 x (V_{DD}/ 5.5 V)	120	ns
t_{ocf}	I²C output fall time; 10 pF to 400 pF bus		300	20 x (V_{DD}/ 5.5 V)	300	20 x (V_{DD}/ 5.5 V)	120	µs
t_{buf}	I²C bus free time between Stop and Start	4.7		1.3		0.5		µs
t_{sts}	I²C Start or repeater Start condition setup time	4.7		0.6		0.26		µs
t_{sth}	I²C Start or repeater Start condition hold time	4		0.6		0.26		µs
t_{sps}	I²C Stop condition setup time	4		0.6		0.26		µs
$t_{vd(data)}$	Valid data time; SCL low to SDA output valid		3.45	0.3	0.9		0.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low		3.45	0.3	0.9		0.45	µs

SWITCHING CHARACTERISTICS

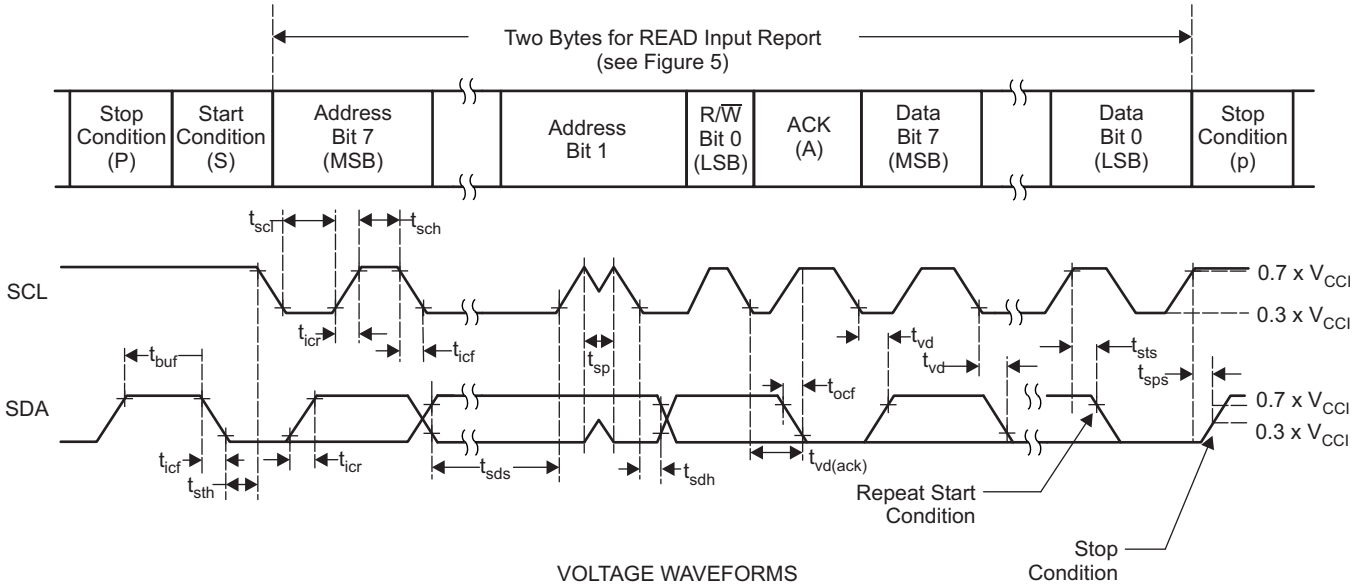
over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{ir}	Interrupt reset delay time	SCL	INT		600	ns
t_{pv}	Output data valid	SCL	LEDx		155	ns

PARAMETER MEASUREMENT INFORMATION



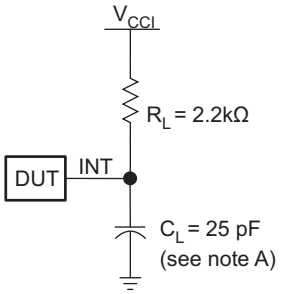
SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance. t_{ocf} is measured with C_L of 10 pF or 400 pF. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns. All parameters and waveforms are not applicable to all devices.

Figure 11. I²C Interface Load Circuit and Voltage Waveforms



INTERRUPT LOAD CONFIGURATION

A. C_L includes probe and jig capacitance. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns. All parameters and waveforms are not applicable to all devices.

Figure 12. Interrupt Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

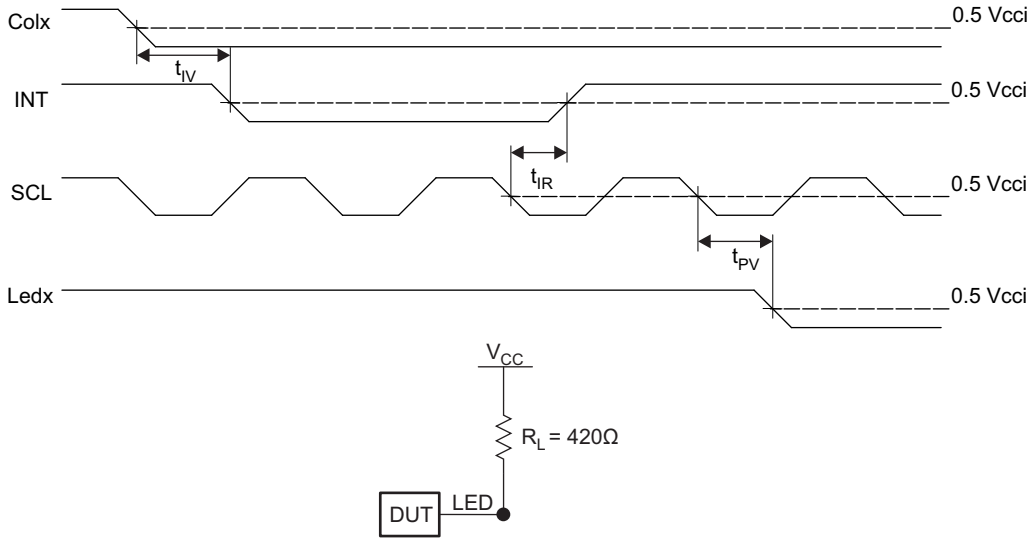


Figure 13. LED Load Configuration

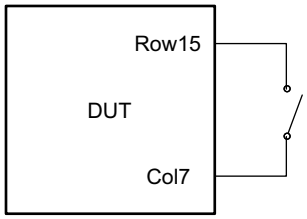


Figure 14. Row Pull-down Load Configuration

C_L includes probe and jig capacitance. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns. The outputs are measured one at a time, with one transition per measurement. All parameters and waveforms are not applicable to all devices.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA8424RHAR	NRND	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	PZ 424	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

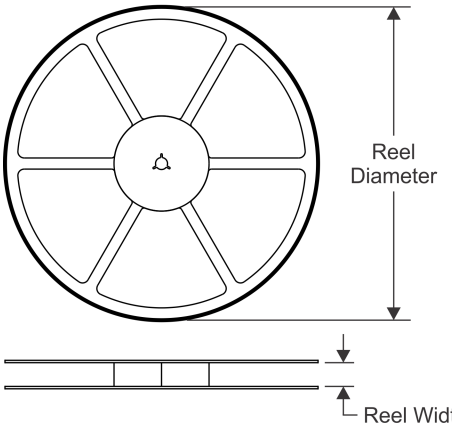
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

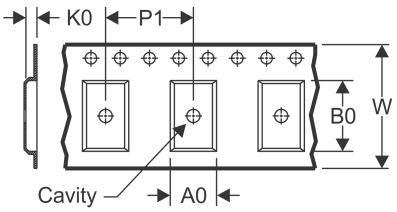
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

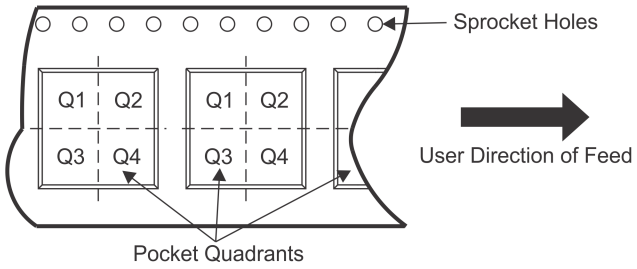


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

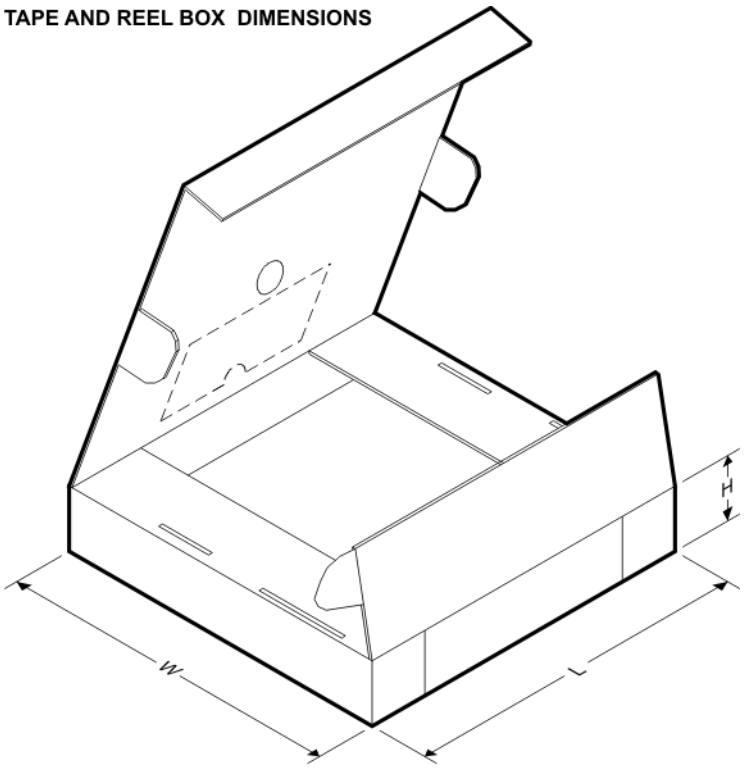
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA8424RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

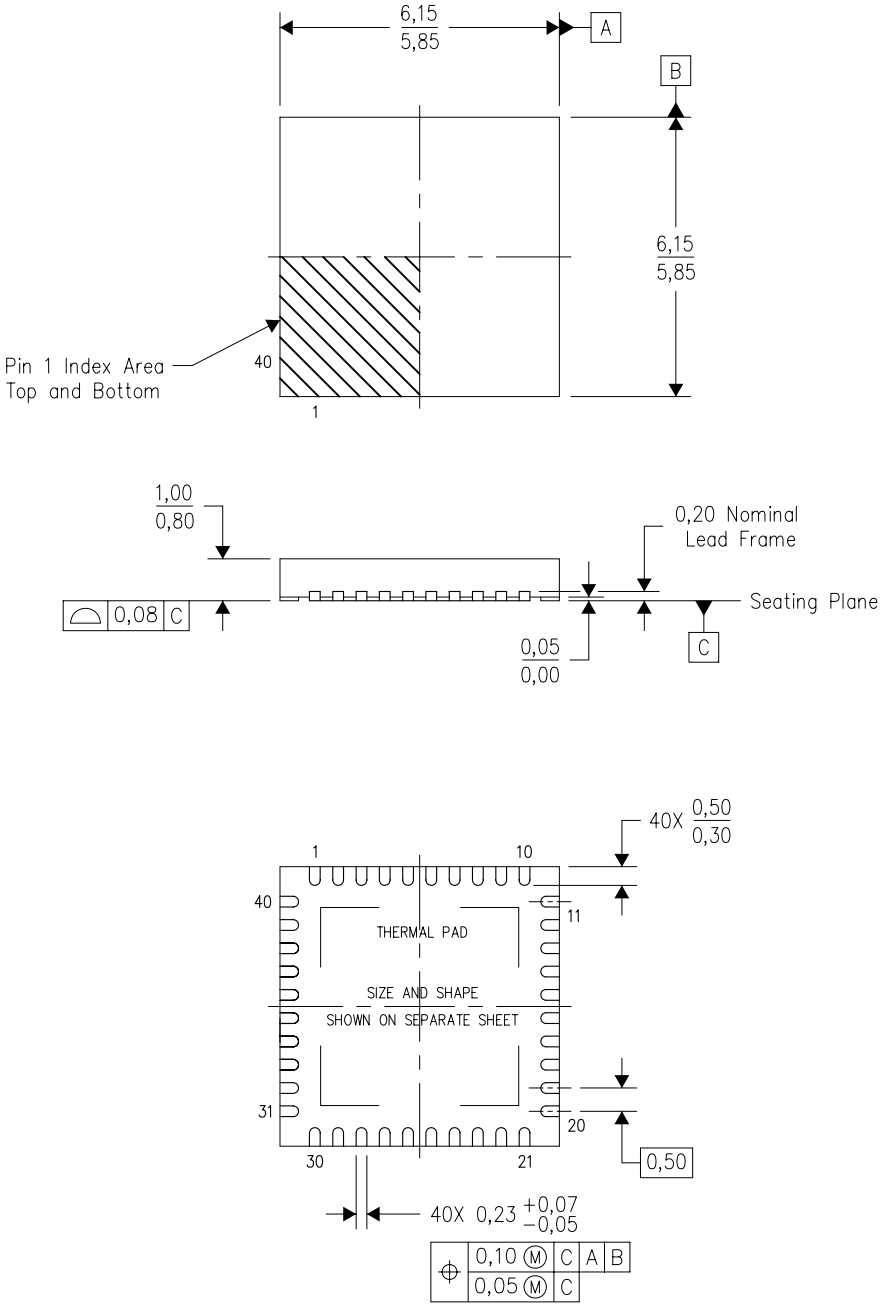
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA8424RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

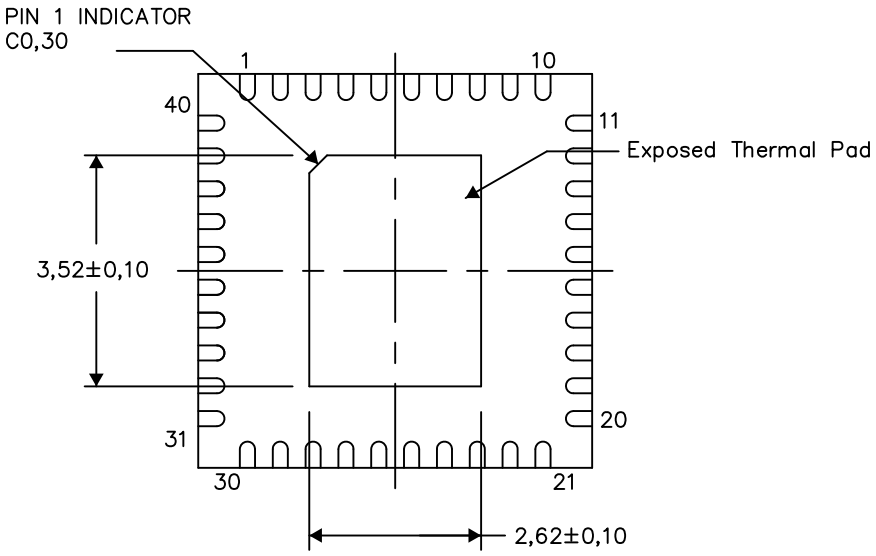
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



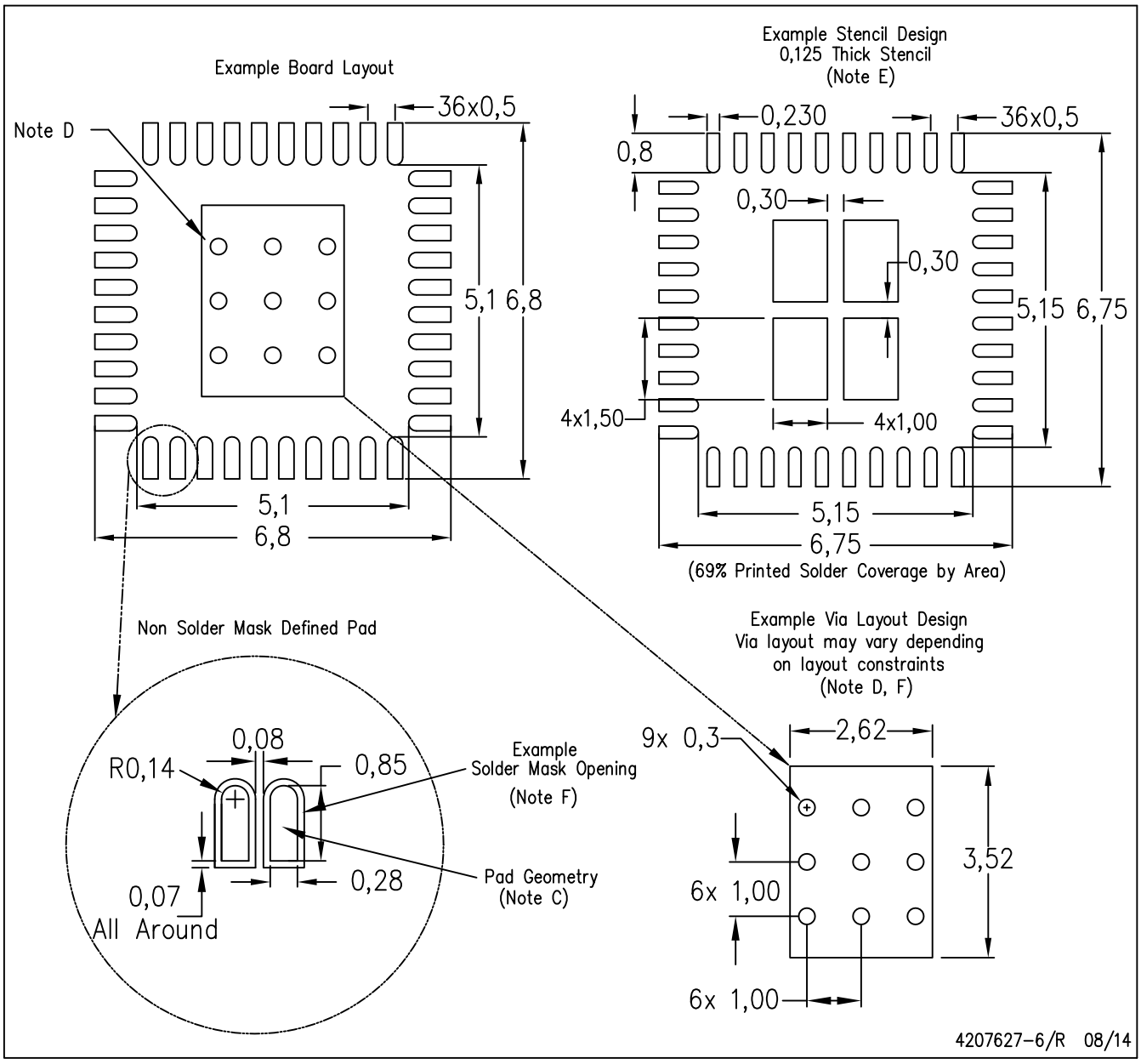
Bottom View

Exposed Thermal Pad Dimensions

4206355–9/X 08/14

NOTES: A. All linear dimensions are in millimeters

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265