

# High Voltage, High Gain BiMOSFET™

## IXBL64N250

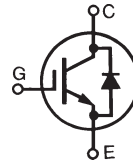
$$V_{CES} = 2500V$$

$$I_{C110} = 46A$$

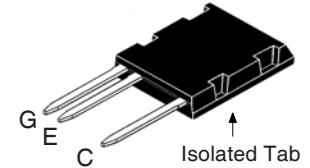
$$V_{CE(sat)} \leq 3.0V$$

### Monolithic Bipolar MOS Transistor

(Electrically Isolated Tab)



#### ISOPLUS i5-Pak™



G = Gate      C = Collector  
E = Emitter

Symbol	Test Conditions	Maximum Ratings	
$V_{CES}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$	2500	V
$V_{CGR}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$ , $R_{GE} = 1M\Omega$	2500	V
$V_{GES}$	Continuous	$\pm 25$	V
$V_{GEM}$	Transient	$\pm 35$	V
$I_{C25}$	$T_C = 25^\circ\text{C}$	116	A
$I_{C110}$	$T_C = 110^\circ\text{C}$	46	A
$I_{CM}$	$T_C = 25^\circ\text{C}$ , 1ms	750	A
<b>SSOA</b>	$V_{GE} = 15V$ , $T_{VJ} = 125^\circ\text{C}$ , $R_G = 1\Omega$	$I_{CM} = 160$	A
<b>(RBSOA)</b>	Clamped Inductive Load	$V_{CE} \leq 0.8 \cdot V_{CES}$	
<b><math>T_{SC}</math> (SCSOA)</b>	$V_{GE} = 15V$ , $T_J = 125^\circ\text{C}$ $R_G = 5\Omega$ , $V_{CE} = 1250V$ , Non-Repetitive	10	$\mu\text{s}$
$P_C$	$T_C = 25^\circ\text{C}$	500	W
$T_J$		-55 ... +150	$^\circ\text{C}$
$T_{JM}$		150	$^\circ\text{C}$
$T_{stg}$		-55 ... +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
$T_{SOLD}$	1.6 mm (0.062 in.) from Case for 10	260	$^\circ\text{C}$
$V_{ISOL}$	50/60Hz, 1 minute	2500	V~
$F_C$	Mounting Force with Clip	30..170 / 7..36	Nm/lb-in.
<b>Weight</b>		8	g

#### Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 2500V~ Electrical Isolation
- High Blocking Voltage
- Low Switching Losses
- High Current Handling Capability
- Anti-Parallel Diode

#### Advantages

- High Power Density
- Low Gate Drive Requirement

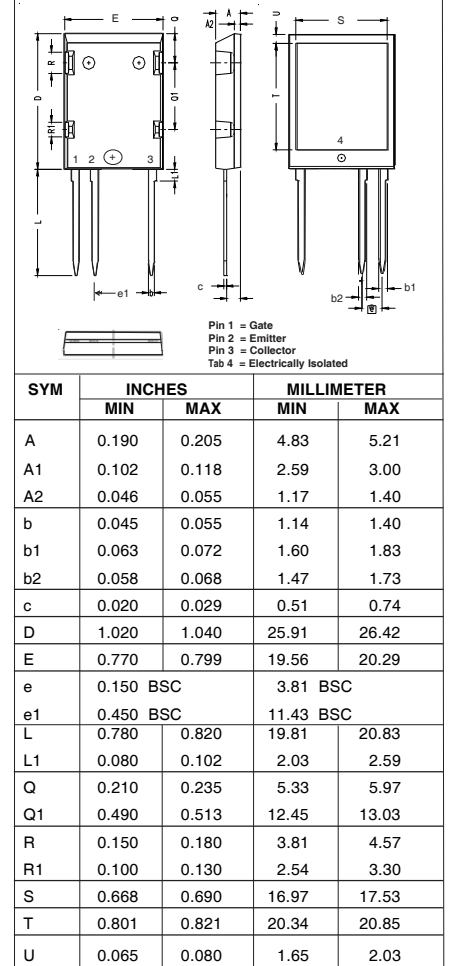
#### Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Uninterrupted Power Supplies (UPS)
- Capacitor Discharge Circuits
- Laser Generators

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{CES}$	$I_C = 1\text{mA}$ , $V_{GE} = 0V$	2500		V
$V_{GE(th)}$	$I_C = 4\text{mA}$ , $V_{CE} = V_{GE}$	3.0		5.0 V
$I_{CES}$	$V_{CE} = 0.8 \cdot V_{CES}$ , $V_{GE} = 0V$ Note 2, $T_J = 125^\circ\text{C}$			50 $\mu\text{A}$ 6 mA
$I_{GES}$	$V_{CE} = 0V$ , $V_{GE} = \pm 25V$			$\pm 200$ nA
$V_{CE(sat)}$	$I_C = 64A$ , $V_{GE} = 15V$ , Note 1 $T_J = 125^\circ\text{C}$		2.5 3.1	3.0 V V

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$I_C = 64\text{A}, V_{CE} = 10\text{V}$ , Note 1	40	72	S
$C_{ies}$	$V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$		8900	pF
$C_{oes}$			345	pF
$C_{res}$			118	pF
$Q_g$	$I_C = 64\text{A}, V_{GE} = 15\text{V}, V_{CE} = 600\text{V}$		400	nC
$Q_{ge}$			46	nC
$Q_{gc}$			155	nC
$t_{d(on)}$	<b>Resistive Switching Times, <math>T_J = 25^\circ\text{C}</math></b> $I_C = 128\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 1250\text{V}, R_G = 1\Omega$		49	ns
$t_r$			318	ns
$t_{d(off)}$			232	ns
$t_f$			170	ns
$t_{d(on)}$	<b>Resistive Switching Times, <math>T_J = 125^\circ\text{C}</math></b> $I_C = 128\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 1250\text{V}, R_G = 1\Omega$		54	ns
$t_r$			578	ns
$t_{d(off)}$			222	ns
$t_f$			175	ns
$R_{thJC}$				0.25 °C/W
$R_{thCS}$		0.15		°C/W

ISOPLUS i5-Pak™ HV (IXBL) Outline



### Reverse Diode

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max
$V_F$	$I_F = 64\text{A}, V_{GE} = 0\text{V}$ , Note 1			3.0 V
$t_{rr}$	$I_F = 64\text{A}, V_{GE} = 0\text{V}, -di_F/dt = 650\text{A}/\mu\text{s}$		160	ns
$I_{RM}$		$V_R = 600\text{V}, V_{GE} = 0\text{V}$		480

### Notes:

1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .
2. Part must be heatsunk for high-temp  $I_{ces}$  measurement.

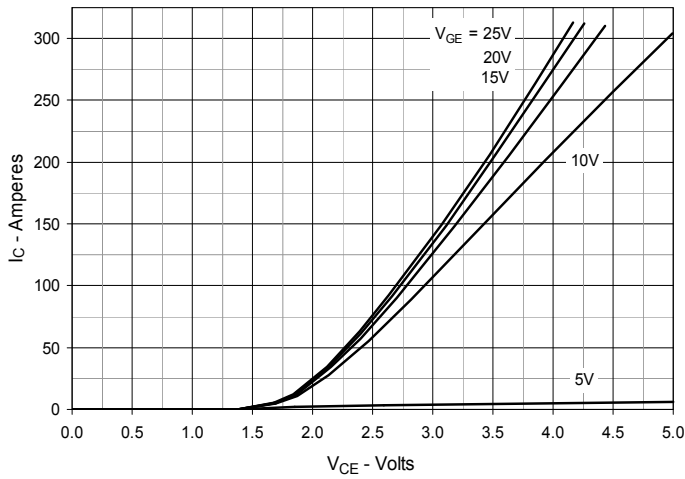
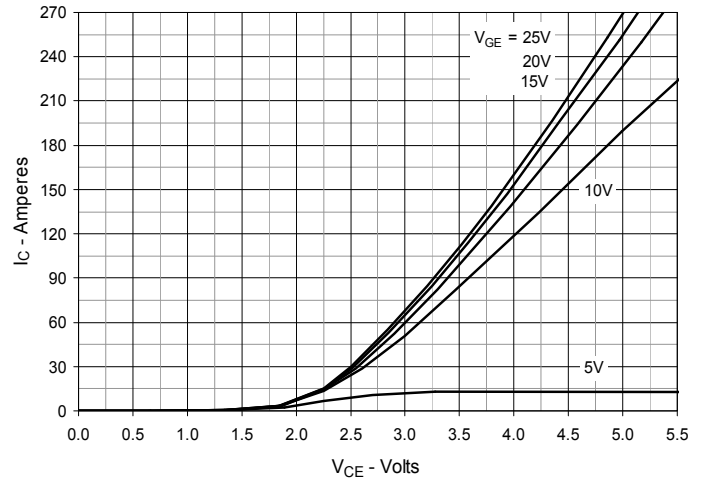
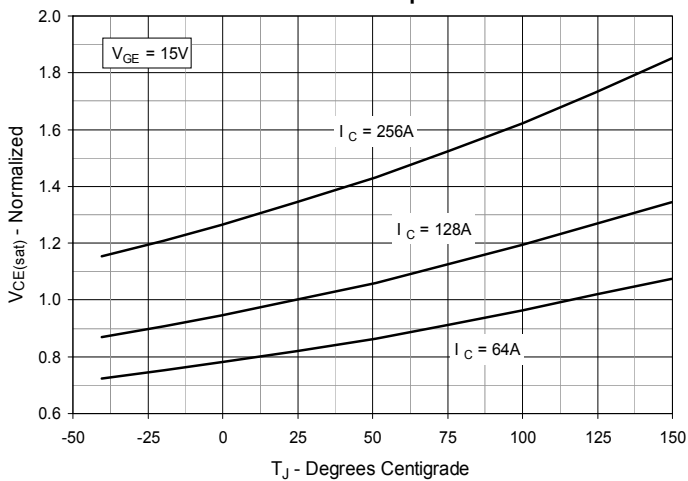
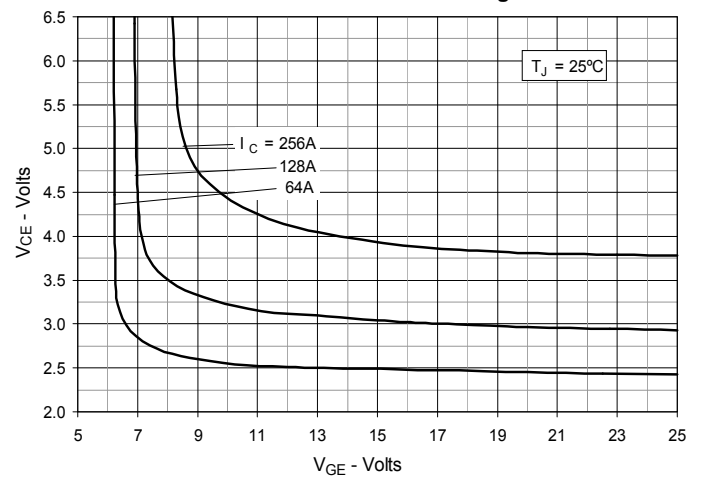
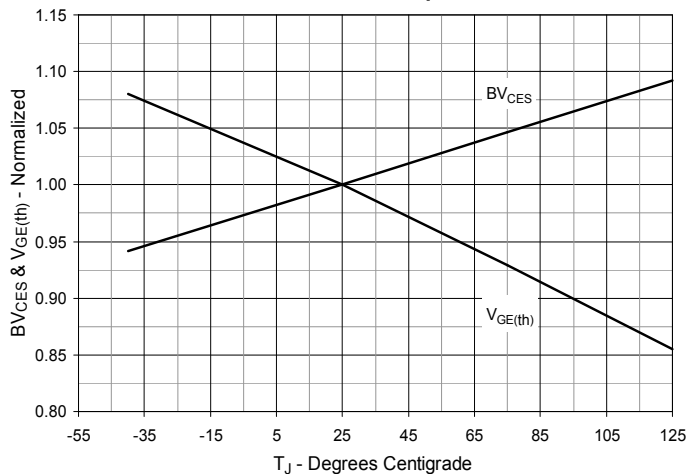
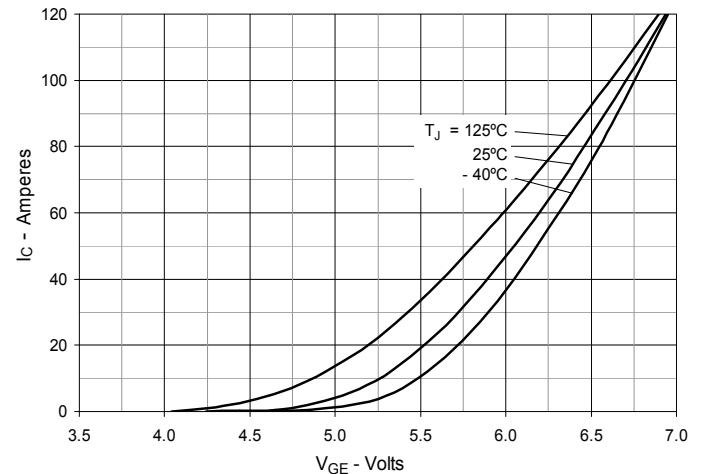
Additional provisions for lead-to-lead isolation are required at  $V_{CE} > 1200\text{V}$

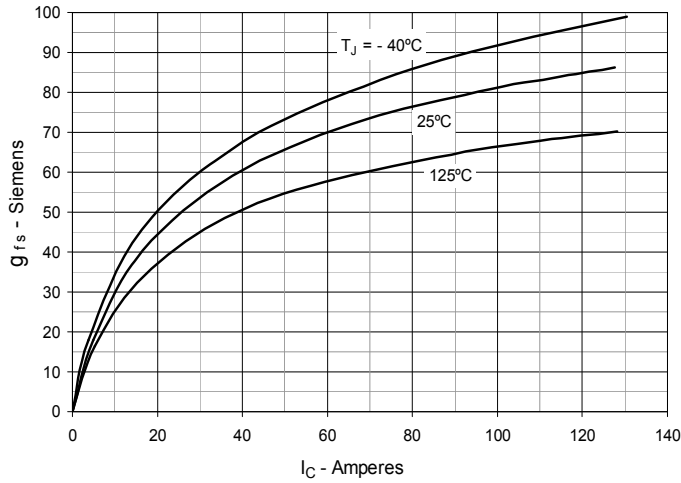
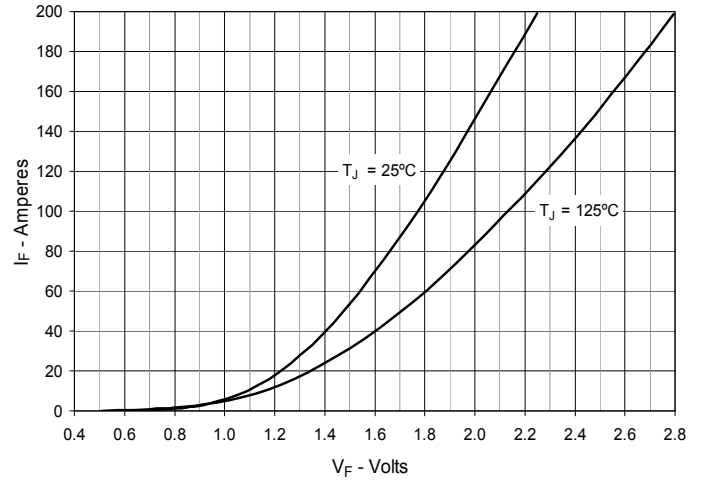
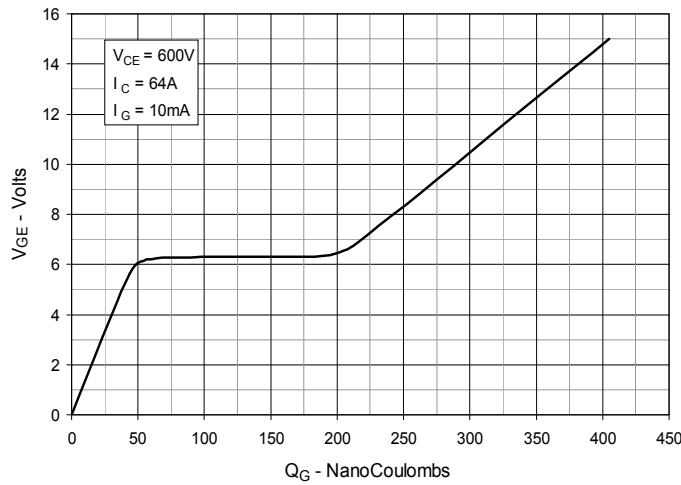
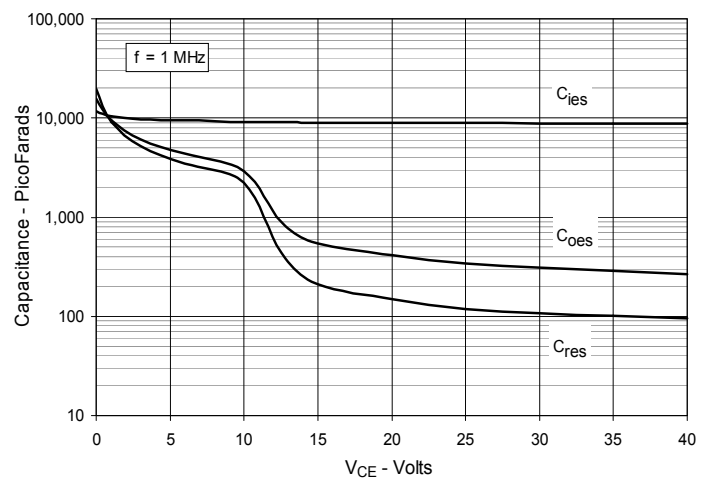
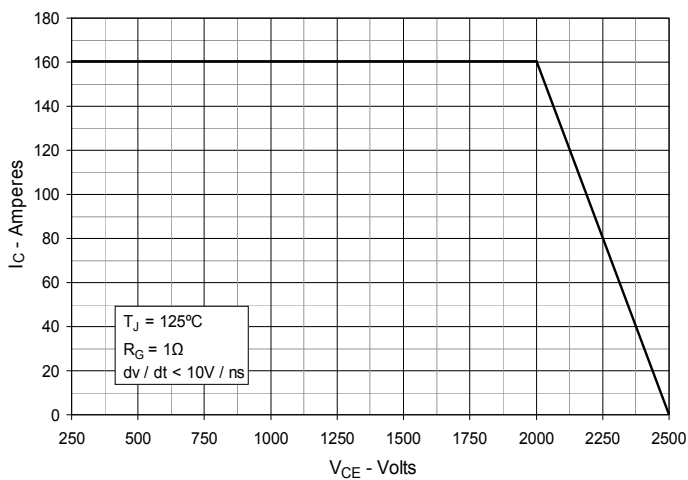
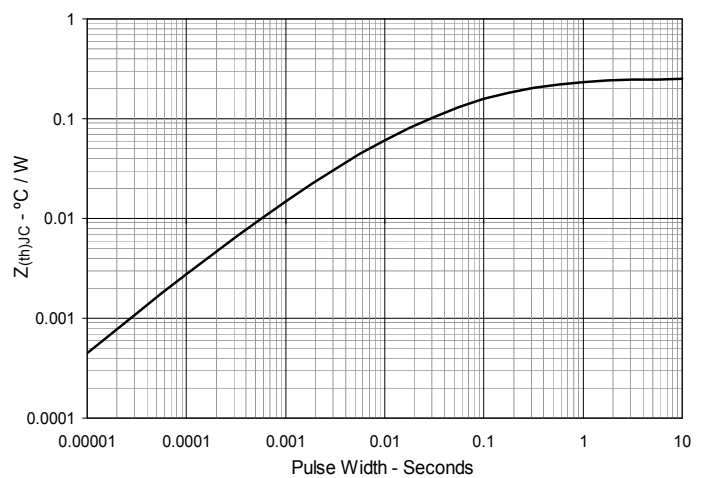
### ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

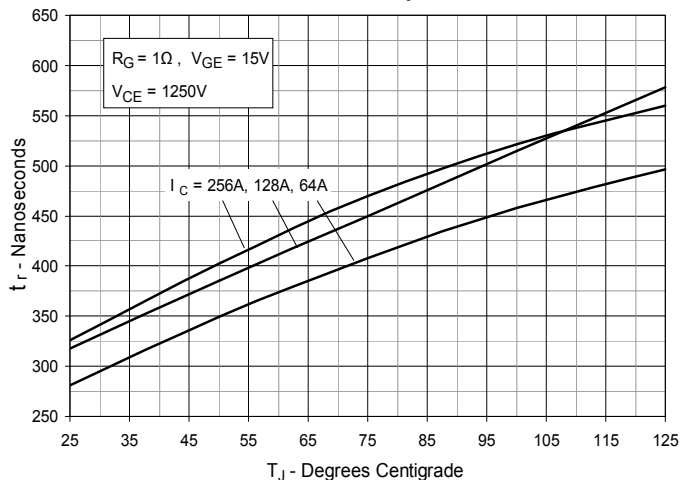
IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

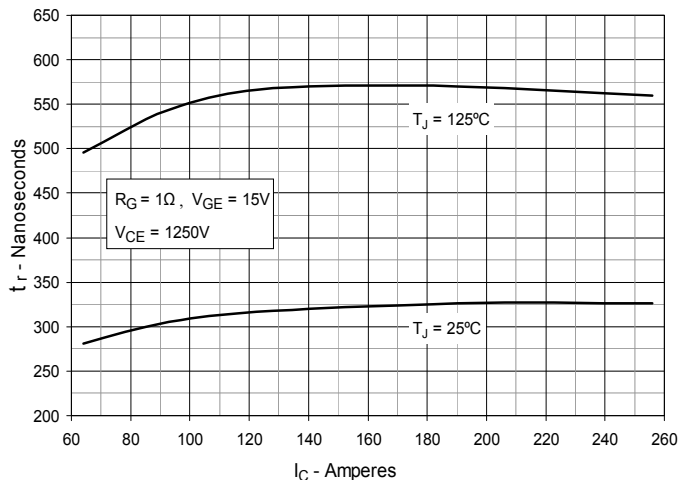
**Fig. 1. Output Characteristics @  $T_J = 25^\circ\text{C}$** 

**Fig. 2. Output Characteristics @  $T_J = 125^\circ\text{C}$** 

**Fig. 3. Dependence of  $V_{CE(sat)}$  on Junction Temperature**

**Fig. 4. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage**

**Fig. 5. Breakdown & Threshold Voltages vs. Junction Temperature**

**Fig. 6. Input Admittance**


**Fig. 7. Transconductance**

**Fig. 8. Forward Voltage Drop of Intrinsic Diode**

**Fig. 9. Gate Charge**

**Fig. 10. Capacitance**

**Fig. 11. Reverse-Bias Safe Operating Area**

**Fig. 12. Maximum Transient Thermal Impedance**


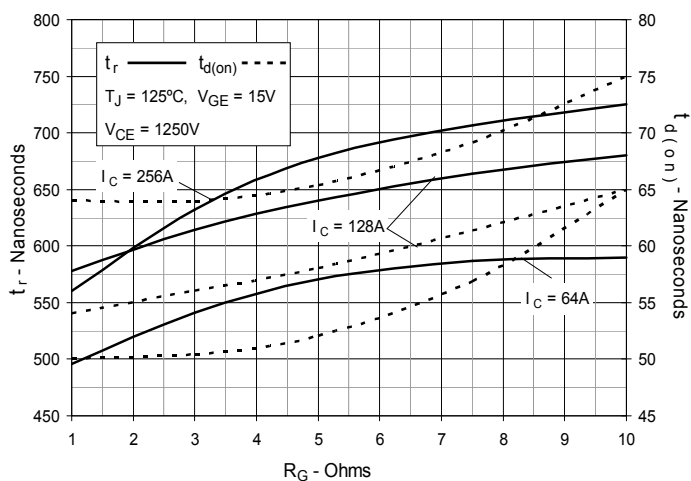
**Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature**



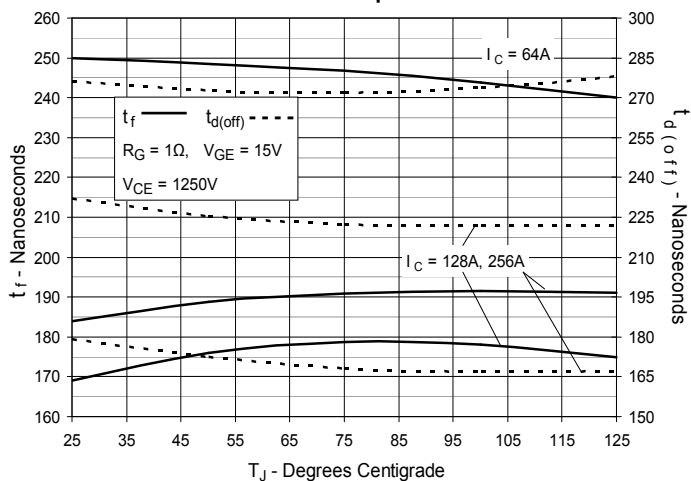
**Fig. 14. Resistive Turn-on Rise Time vs. Drain Current**



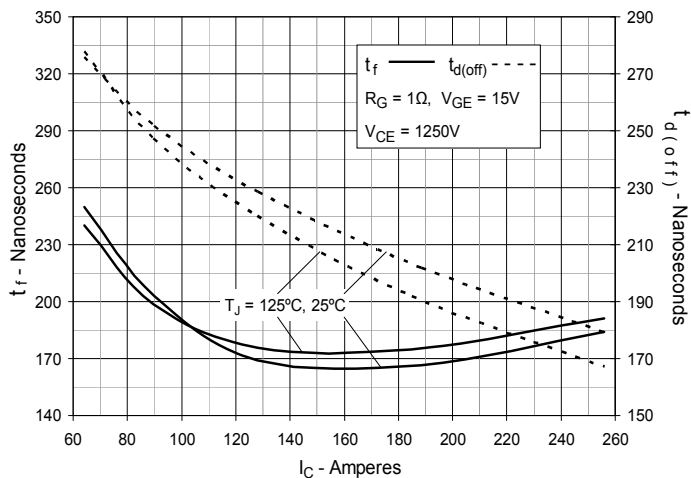
**Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance**



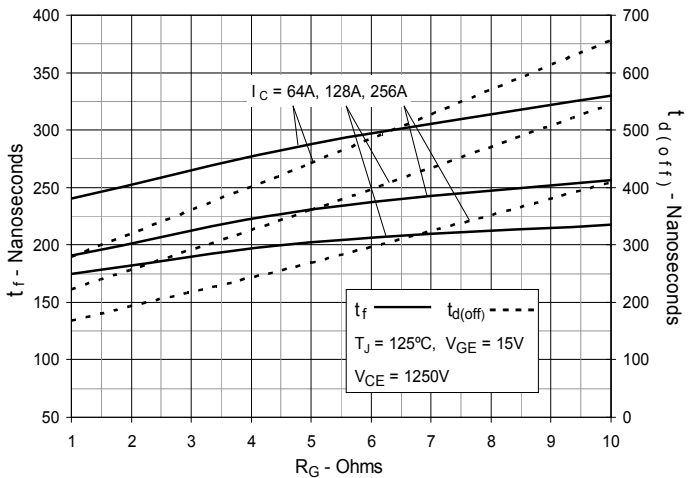
**Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature**



**Fig. 17. Resistive Turn-off Switching Times vs. Drain Current**



**Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance**



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