

# MC74HC160A

## Presettable Counters

### High-Performance Silicon-Gate CMOS

The MC74HC160A is identical in pinout to the LS160. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC160A is a programmable BCD counters with asynchronous Reset input.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates
- These are Pb-Free Devices

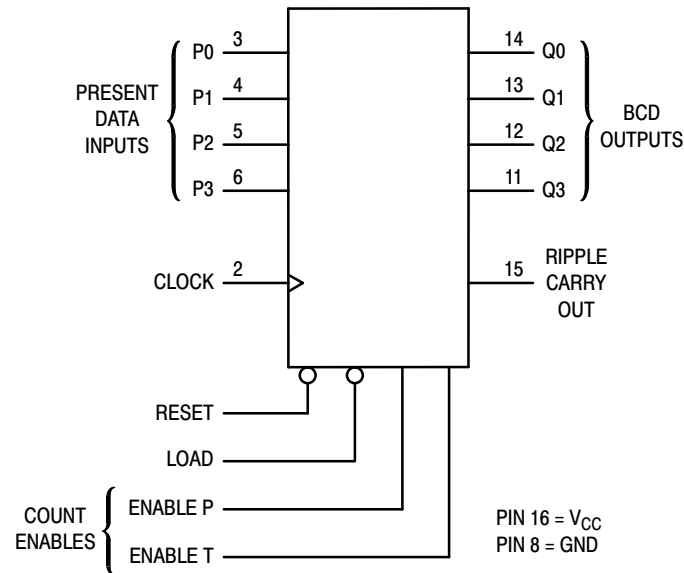


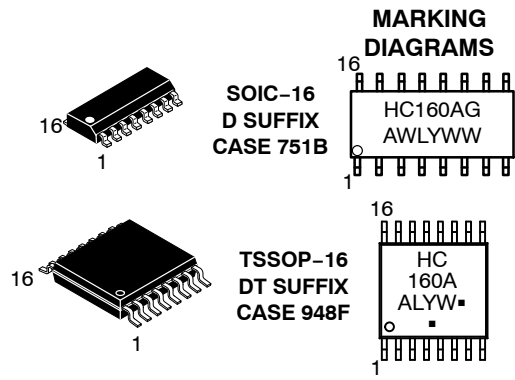
Figure 1. Logic Diagram

Device	Count Mode	Reset Mode
HC160	BCD	Asynchronous



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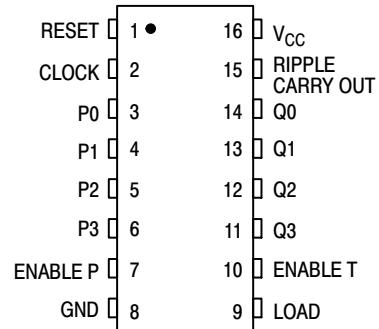
<http://onsemi.com>



A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN ASSIGNMENT



#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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## FUNCTION TABLE

Inputs					Outputs
Clock	Reset*	Load	Enable P	Enable T	Q
↘	L	X	X	X	Reset
↘	H	L	X	X	Load Preset Data
↘	H	H	H	H	Count
↘	H	H	L	X	No Count
↘	H	H	X	L	No Count

\*HC160 is an Asynchronous Reset Device.

H = High Level

L = Low Level

X = Don't Care

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	±20	mA
$I_{out}$	DC Output Current, per Pin	±25	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	±50	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating - SOIC Package: - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 3)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 1000 500 400	ns

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	3.0	2.48	2.34	2.20	
			4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4	40	160	μA

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## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle)* (Figures 3 and 8)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t <sub>PLH</sub>	Maximum Propagation Delay, Clock to Q (Figures 3 and 8)	2.0	170	215	255	ns
		4.5	34	43	51	
		6.0	29	37	43	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q (HC160A Only) (Figures 4 and 8)	2.0	205	255	310	ns
		4.5	41	51	62	
		6.0	35	43	53	
t <sub>PLH</sub>	Maximum Propagation Delay, Enable T to Ripple Carry Out (Figures 5 and 8)	2.0	160	200	240	ns
		4.5	32	40	48	
		6.0	27	34	41	
t <sub>PHL</sub>	Maximum Propagation Delay, Enable T to Ripple Carry Out (Figures 5 and 8)	2.0	195	245	295	ns
		4.5	39	49	59	
		6.0	33	42	50	
t <sub>PLH</sub>	Maximum Propagation Delay, Clock to Ripple Carry Out (Figures 3 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Ripple Carry Out (Figures 3 and 8)	2.0	215	270	325	ns
		4.5	43	54	65	
		6.0	37	46	55	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Ripple Carry Out (HC160A Only) (Figures 4 and 8)	2.0	220	275	330	ns
		4.5	44	55	66	
		6.0	37	47	56	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 3 and 8)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	-	10	10	10	pF

\*Applies to noncascaded/nonsynchronously clocked configurations only. With synchronously cascaded counters, (1) Clock to Ripple Carry Out propagation delays, (2) Enable T or Enable P to Clock setup times, and (3) Clock to Enable T or Enable P hold times determine f<sub>max</sub>. However, if Ripple Carry Out of each stage is tied to the Clock of the next stage (nonsynchronously clocked), the f<sub>max</sub> in the table above is applicable. See Applications Information in this data sheet.

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
		60	pF

\*Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

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## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
$t_{su}$	Minimum Setup Time, Preset Data Inputs to Clock (Figure 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
$t_{su}$	Minimum Setup Time, Load to Clock (Figure 6)	2.0	135	170	205	ns
		4.5	27	34	41	
		6.0	23	29	35	
$t_{su}$	Minimum Setup Time, Enable T or Enable P to Clock (Figure 7)	2.0	200	250	300	ns
		4.5	40	50	60	
		6.0	34	43	51	
$t_h$	Minimum Hold Time, Clock to Preset Data Inputs (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
$t_h$	Minimum Hold Time, Clock to Load (Figure 6)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
$t_h$	Minimum Hold Time, Clock to Enable T or Enable P (Figure 7)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Clock (Figure 4)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
$t_{rec}$	Minimum Recovery Time, Load Inactive to Clock (Figure 6)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
$t_w$	Minimum Pulse Width, Clock (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_w$	Minimum Pulse Width, Reset (Figure 4)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 3)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

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## FUNCTION DESCRIPTION

The HC160A is a programmable 4-bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading, and count-enable controls. The HC160A is a BCD counter with asynchronous Reset.

### INPUTS

#### Clock (Pin 2)

The internal flip-flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as loading occur with the rising edge of the Clock input.

#### Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6)

These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip-flops and appear at the counter outputs. P0 (pin 3) is the least-significant bit and P3 (pin 6) is the most-significant bit.

### OUTPUTS

#### Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11)

These are the counter outputs (BCD or binary). Q0 (pin 14) is the least-significant bit and Q3 (pin 11) is the most-significant bit.

#### Ripple Carry Out (Pin 15)

When the counter is in its maximum state (1001 for the BCD counters or 1111 for the binary counters), this output goes high, providing an external look-ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equation for this output is:

$$\text{Ripple Carry Out} = \text{Enable T} \cdot \text{Q0} \cdot \overline{\text{Q1}} \cdot \overline{\text{Q2}} \cdot \text{Q3}$$

for BCD counters

### CONTROL FUNCTIONS

#### Resetting

A low level on the Reset pin (pin 1) resets the internal flip-flops and sets the outputs (Q0 through Q3) to a low level. The HC160A resets asynchronously.

### Loading

With the rising edge of the Clock, a low level on Load (pin 9) loads the data from the Preset Data Input pins (P0, P1, P2, P3) into the internal flip-flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

Although the HC160A is a BCD counters, they may be programmed to any state. If they are loaded with a state disallowed in BCD code, they will return to their normal count sequence within two clock pulses (see the Output State Diagram).

### Count Enable/Disable

These devices have two count-enable control pins: Enable P (pin 7) and Enable T (pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

$$\text{Count Enable} = \text{Enable P} \cdot \text{Enable T} \cdot \text{Load}$$

The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count-enable control; Enable T is both a count-enable and a Ripple-Carry Output control.

Table 1. COUNT ENABLE/DISABLE

Control Inputs		Result at Outputs		
Load	Enable P	Enable T	Q0 - Q3	Ripple Carry Out
H	H	H	Count	High when Q0 - Q3 are maximum*
L	H	H	No Count	
X	L	H	No Count	High when Q0 - Q3 are maximum*
X	X	L	No Count	L

\*Q0 through Q3 are maximum for the HC160A when Q3 Q2 Q1 Q0 = 1001.

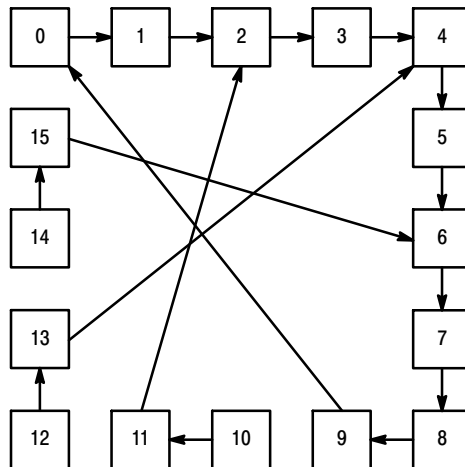


Figure 2. Output State Diagrams HC160A BCD Counters

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## SWITCHING WAVEFORMS

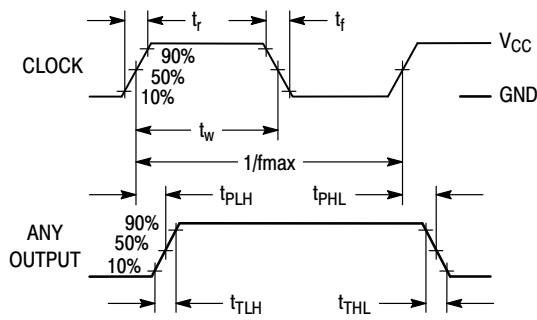


Figure 3.

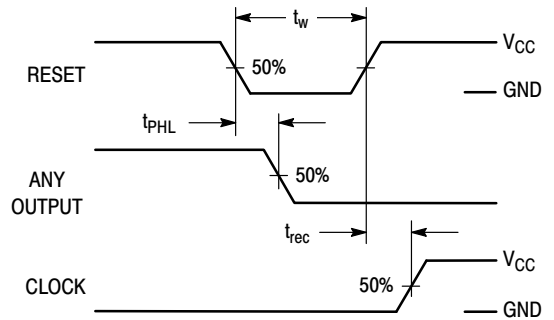


Figure 4.

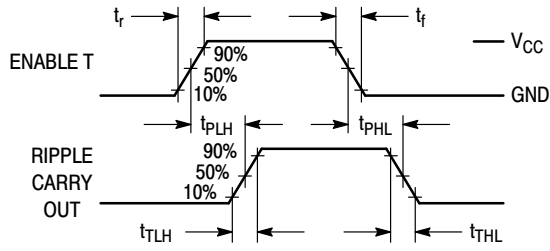


Figure 5.

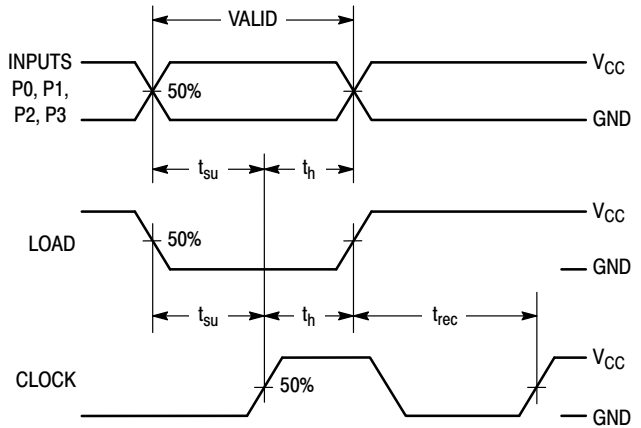


Figure 6.

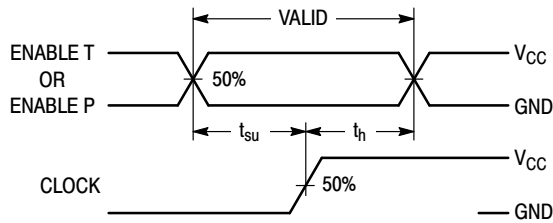
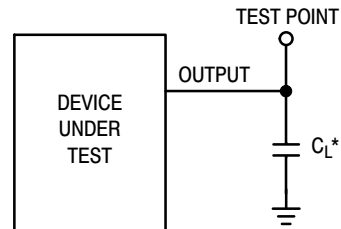


Figure 7.

### TEST CIRCUIT

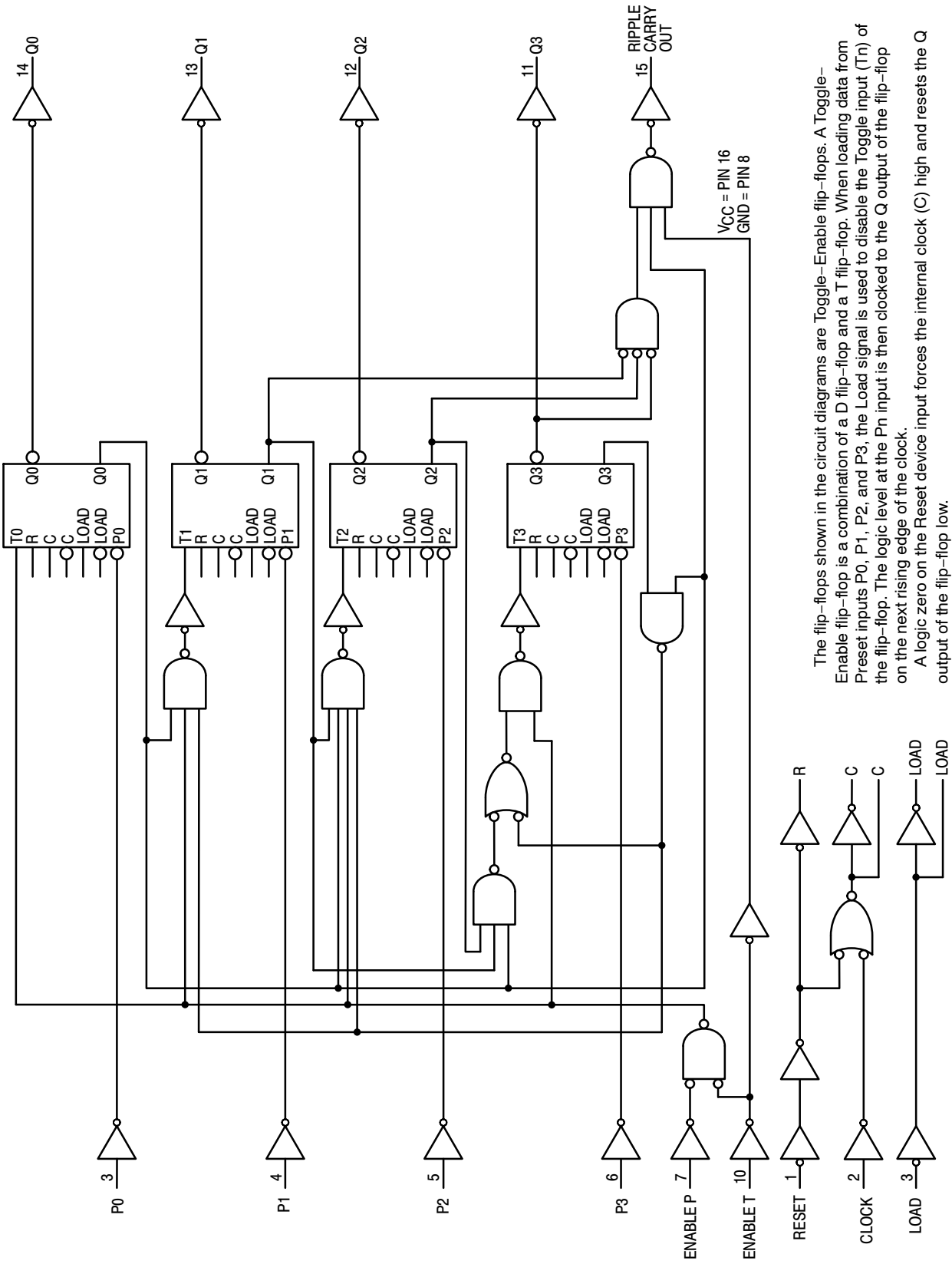


\*Includes all probe and jig capacitance

Figure 8.

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## MC74HC160A BCD Counter with Asynchronous Reset



The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.  
A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.



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Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit.

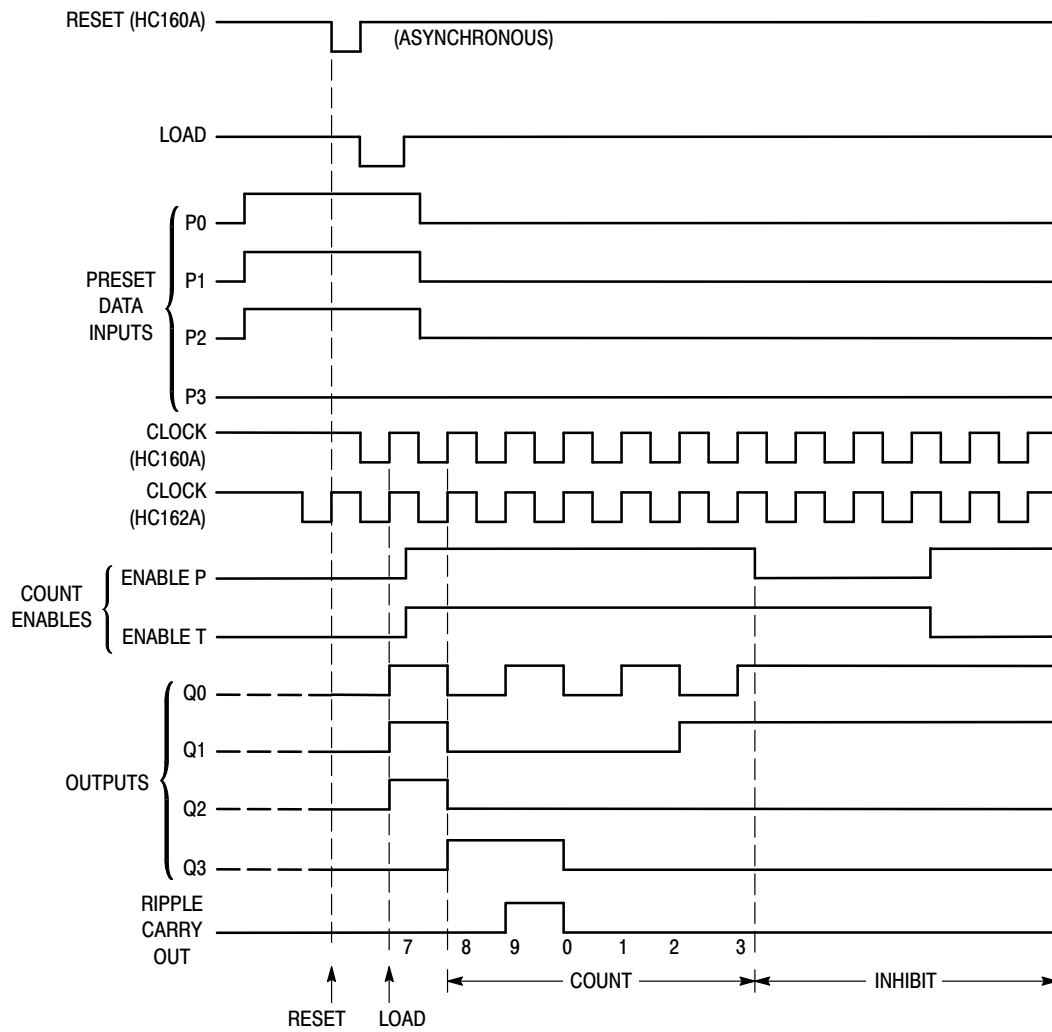
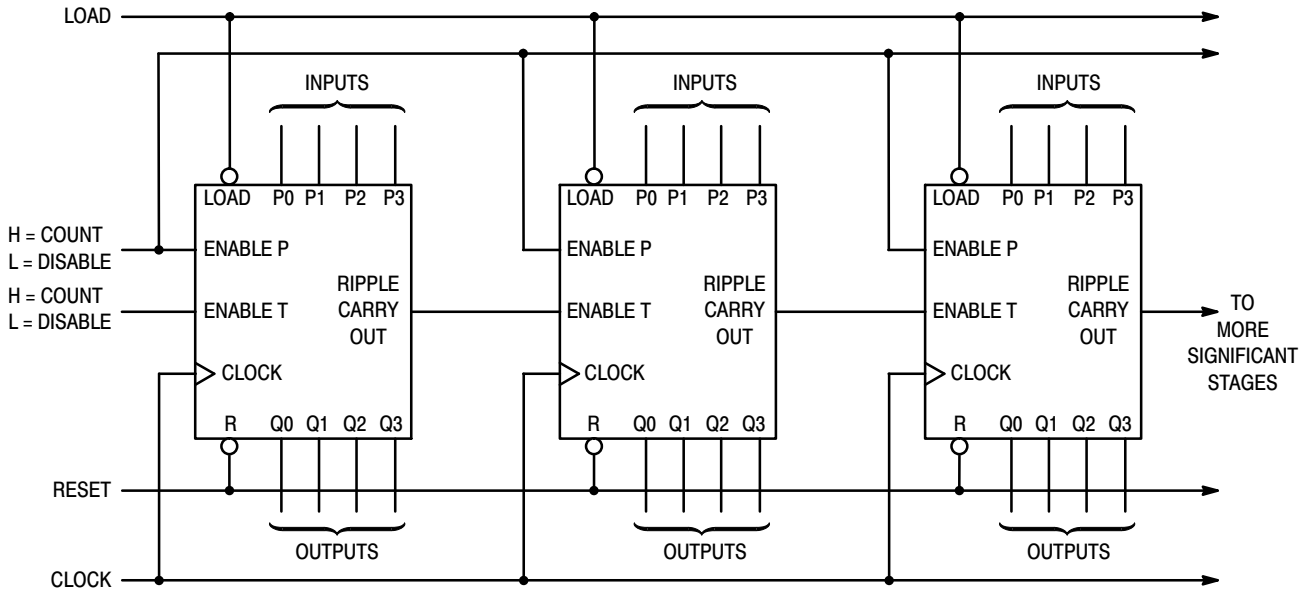


Figure 9. MC74HC160A Timing Diagram

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## TYPICAL APPLICATIONS CASCADING



NOTE: When used in these cascaded configurations the clock  $f_{max}$  guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and Clock.

Figure 10. N-Bit Synchronous Counters

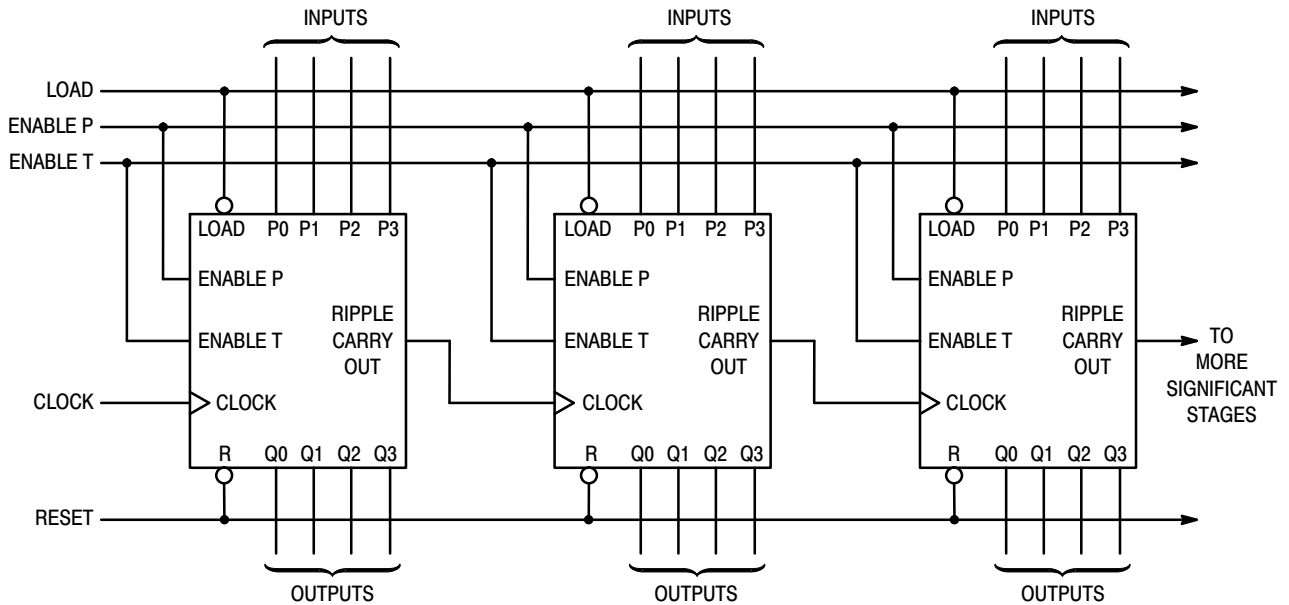


Figure 11. Nibble Ripple Counter

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74HC160ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC160ADR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74HC160ADTG	TSSOP-16*	96 Units / Rail
MC74HC160ADTR2G	TSSOP-16*	2500 Tape & Reel

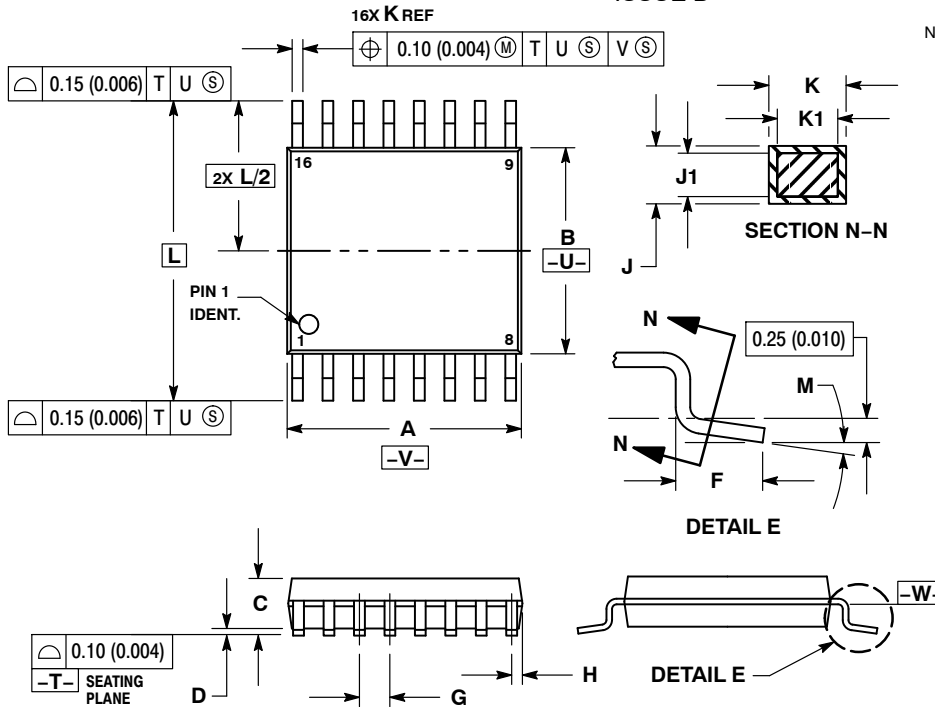
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

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## PACKAGE DIMENSIONS

TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE B

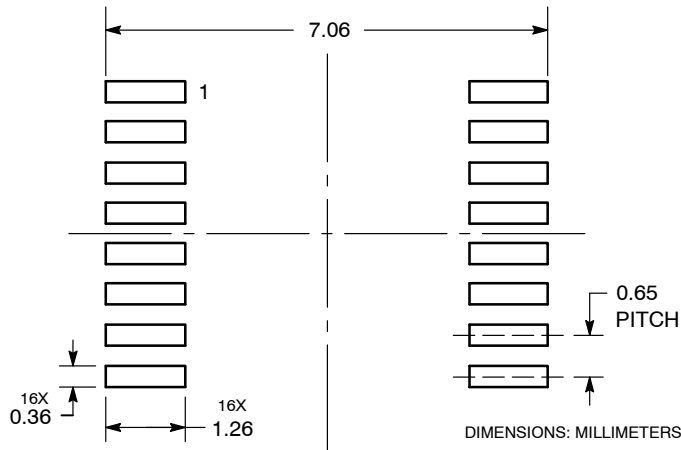


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT\*

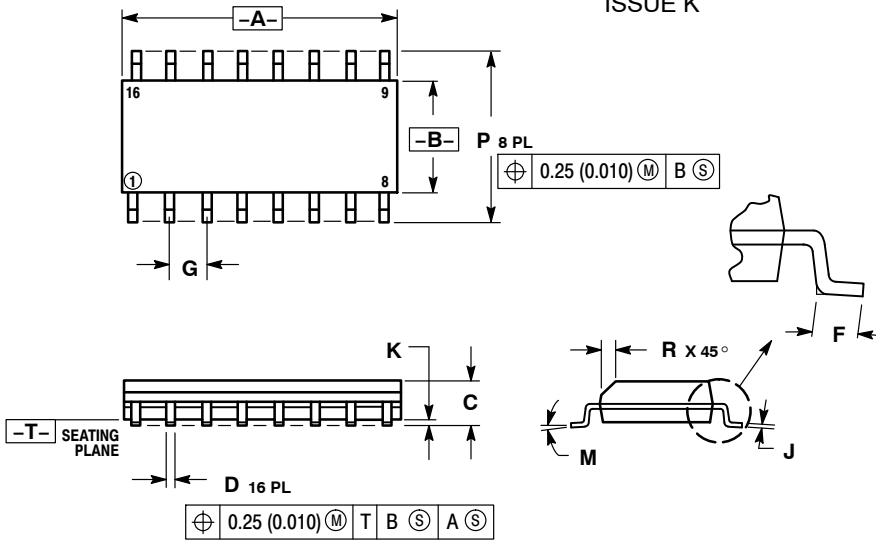


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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## PACKAGE DIMENSIONS

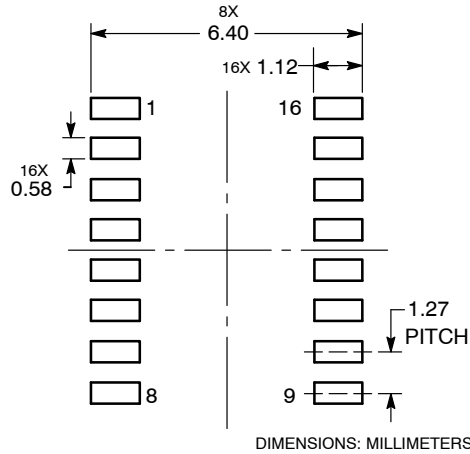
SOIC-16  
CASE 751B-05  
ISSUE K



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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