

# 74ABT16244A

16-bit buffer/line driver; 3-state

Rev. 8 — 3 November 2011

Product data sheet

## 1. General description

The 74ABT16244A high-performance Bipolar CMOS (BiCMOS) device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16244A is a 16-bit buffer that is ideal for driving bus lines. The device features four output enable inputs ( $1\overline{OE}$ ,  $2\overline{OE}$ ,  $3\overline{OE}$ ,  $4\overline{OE}$ ), each controlling four of the 3-state outputs.

## 2. Features and benefits

- 16-bit bus interface
- Multiple  $V_{CC}$  and GND pins minimize switching noise
- Power-up 3-state
- 3-state buffers
- Output capability: +64 mA and -32 mA
- Live insertion and extraction permitted
- Latch-up performance: JESD 78 Class II
- ESD protection:
  - ◆ HBM JESD-A114E exceeds 2000 V
  - ◆ CDM JESD 22-C101-C exceeds 1000 V

## 3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74ABT16244ADGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm		SOT362-1
74ABT16244ADL	-40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm		SOT370-1

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## 4. Functional diagram

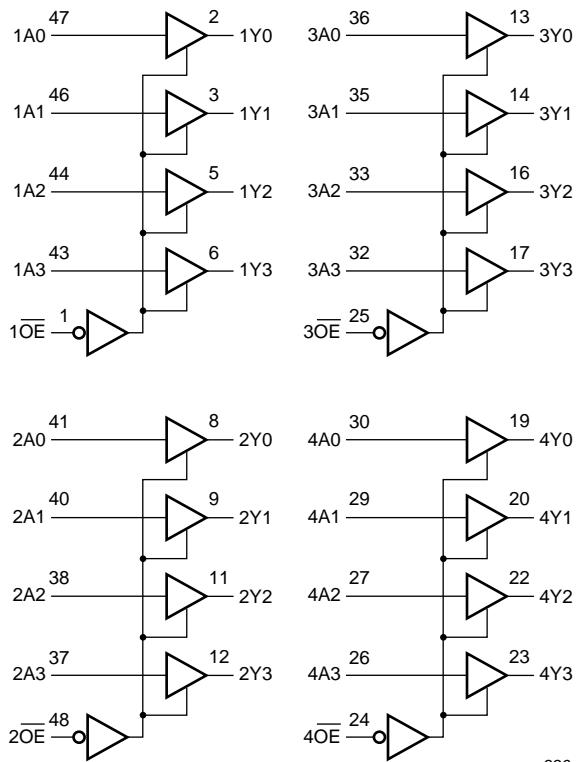


Fig 1. Logic symbol

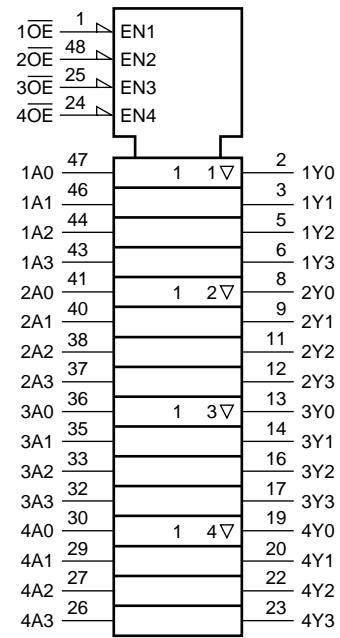


Fig 2. IEC logic symbol

## 5. Pinning information

### 5.1 Pinning

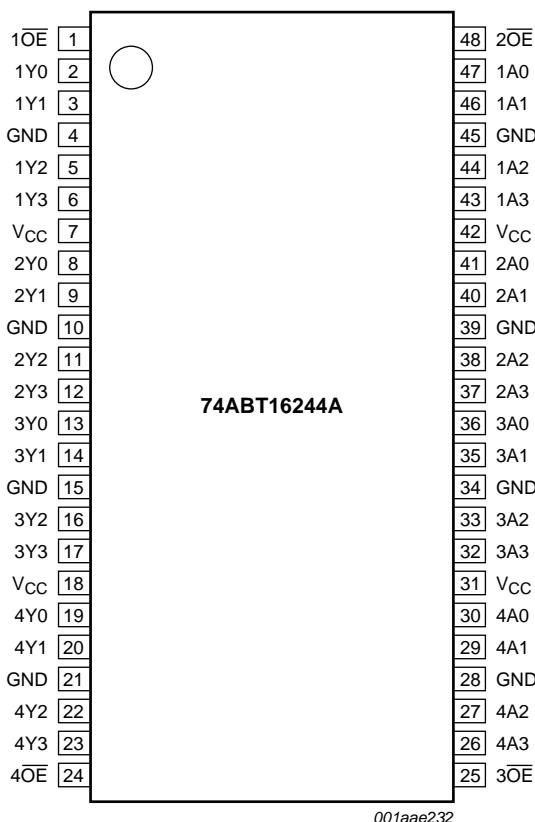


Fig 3. Pin configuration

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE	1	1 output enable (LOW active)
1Y[0:3]	2, 3, 5, 6	1 data output 0 to output 3
GND	4	ground (0 V)
V <sub>CC</sub>	7	supply voltage
2Y[0:3]	8, 9, 11, 12	2 data output 0 to output 3
GND	10	ground (0 V)
3Y[0:3]	13, 14, 16, 17	3 data output 0 to output 3
GND	15	ground (0 V)
V <sub>CC</sub>	18	supply voltage
4Y[0:3]	19, 20, 22, 23	4 data output 0 to output 3
GND	21	ground (0 V)

**Table 2.** Pin description ...continued

Symbol	Pin	Description
4OE	24	4 output enable (LOW active)
3OE	25	3 output enable (LOW active)
GND	28	ground (0 V)
4A[0:3]	30, 29, 27, 26	4 data input 0 to input 3
V <sub>CC</sub>	31	supply voltage
GND	34	ground (0 V)
3A[0:3]	36, 35, 33, 32	3 data input 0 to input 3
GND	39	ground (0 V)
2A[0:3]	41, 40, 38, 37	2 data input 0 to input 3
V <sub>CC</sub>	42	supply voltage
GND	45	ground (0 V)
1A[0:3]	47, 46, 44, 43	1 data input 0 to input 3
2OE	48	2 output enable (LOW active)

## 6. Functional description

**Table 3. Function table<sup>[1]</sup>**

Control	Input	Output
nOE	nAn	nYn
L	L	L
	H	H
H	X	Z

[1] H = HIGH voltage level;

L = LOW voltage level;

X = don't care;

Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		<sup>[1]</sup> -1.2	+7.0	V
V <sub>O</sub>	output voltage	output in OFF-state or HIGH-state	<sup>[1]</sup> -0.5	+5.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-18	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
T <sub>j</sub>	junction temperature		<sup>[2]</sup> -	150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		4.5	-	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	V
V <sub>IL</sub>	LOW-level Input voltage		-	-	0.8	V
I <sub>OH</sub>	HIGH-level output current		-32	-	-	mA
I <sub>OL</sub>	LOW-level output current		-	-	64	mA
Δt/ΔV	input transition rise and fall rate		-	-	10	ns/V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C

## 9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		Unit	
			Min	Typ	Max	Min	Max		
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5 \text{ V}; I_{IK} = -18 \text{ mA}$	-	-0.9	-1.2	-	-1.2	V	
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IL} \text{ or } V_{IH}$							
		$V_{CC} = 4.5 \text{ V}; I_{OH} = -3 \text{ mA}$	2.5	2.9	-	2.5	-	V	
		$V_{CC} = 5.0 \text{ V}; I_{OH} = -3 \text{ mA}$	3.0	3.4	-	3.0	-	V	
		$V_{CC} = 4.5 \text{ V}; I_{OH} = -32 \text{ mA}$	2.0	2.4	-	2.0	-	V	
$V_{OL}$	LOW-level output voltage	$V_{CC} = 4.5 \text{ V}; I_{OL} = 64 \text{ mA}; V_I = V_{IL} \text{ or } V_{IH}$	-	0.42	0.55	-	0.55	V	
$I_I$	input leakage current	$V_{CC} = 5.5 \text{ V}; V_I = V_{CC} \text{ or } GND$	-	±0.01	±1.0	-	±1.0	μA	
$I_{OFF}$	power-off leakage current	$V_{CC} = 0 \text{ V}; V_I \text{ or } V_O \leq 4.5 \text{ V}$	-	±5.0	±100	-	±100	μA	
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} = 2.0 \text{ V}; V_O = 0.5 \text{ V}; V_I = GND \text{ or } V_{CC}; nOE = HIGH$	[1]	-	±5.0	±50	-	±50	μA
$I_{OZ}$	OFF-state output current	$V_{CC} = 5.5 \text{ V}; V_I = V_{IL} \text{ or } V_{IH}$							
		output HIGH-state at $V_O = 5.5 \text{ V}$	-	0.1	10	-	10	μA	
		output LOW-state at $V_O = 0 \text{ V}$	-	-0.1	-10	-	-10	μA	
$I_{LO}$	output leakage current	HIGH-state; $V_O = 5.5 \text{ V}; V_{CC} = 5.5 \text{ V}; V_I = GND \text{ or } V_{CC}$	-	5.0	50	-	50	μA	
$I_O$	output current	$V_{CC} = 5.5 \text{ V}; V_O = 2.5 \text{ V}$	[2]	-50	-100	-180	-50	-180	mA
$I_{CC}$	supply current	$V_{CC} = 5.5 \text{ V}; V_I = GND \text{ or } V_{CC}$							
		outputs HIGH-state	-	0.45	1.0	-	1.0	mA	
		outputs LOW-state	-	10	19	-	19	mA	
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 5.5 \text{ V}$ ; one input at 3.4 V and other inputs at $V_{CC}$ or GND	[3][4]	-	100	250	-	250	μA
				-	100	250	-	250	μA
				-	100	250	-	250	μA
$C_I$	input capacitance	$V_I = 0 \text{ V} \text{ or } V_{CC}$	-	4	-	-	-	pF	
$C_{I/O}$	input/output capacitance	outputs disabled; $V_O = 0 \text{ V} \text{ or } V_{CC}$	-	7	-	-	-	pF	

[1] This parameter is valid for any  $V_{CC}$  between 0 V and 2.1 V, with a transition time of up to 10 ms. From  $V_{CC} = 2.1 \text{ V}$  to  $V_{CC} = 5 \text{ V} \pm 10 \%$ , a transition time of up to 100 μs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

[4] This data sheet limit may vary among suppliers.

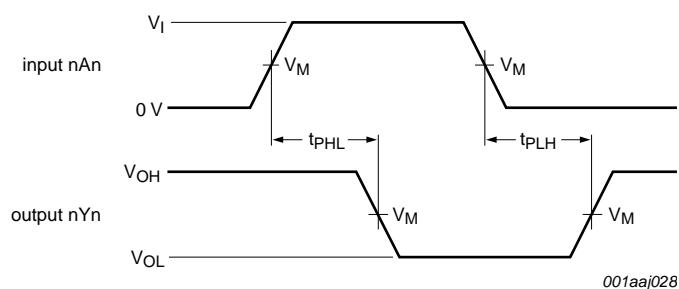
## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

GND = 0 V. For test circuit, see [Figure 6](#).

Symbol	Parameter	Conditions	25 °C; V <sub>CC</sub> = 5.0 V			–40 °C to +85 °C; V <sub>CC</sub> = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	nAn to nYn, see <a href="#">Figure 4</a>	1.1	1.7	2.6	1.1	2.8	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nAn to nYn, see <a href="#">Figure 4</a>	1.3	2.1	2.9	1.3	3.4	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	n $\overline{OE}$ to nYn; see <a href="#">Figure 5</a>	1.6	2.7	3.7	1.6	4.5	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	n $\overline{OE}$ to nYn; see <a href="#">Figure 5</a>	2.3	3.5	4.0	2.3	4.8	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	n $\overline{OE}$ to nYn; see <a href="#">Figure 5</a>	1.5	3.0	4.0	1.5	4.6	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	n $\overline{OE}$ to nYn; see <a href="#">Figure 5</a>	1.6	2.4	3.2	1.6	4.1	ns

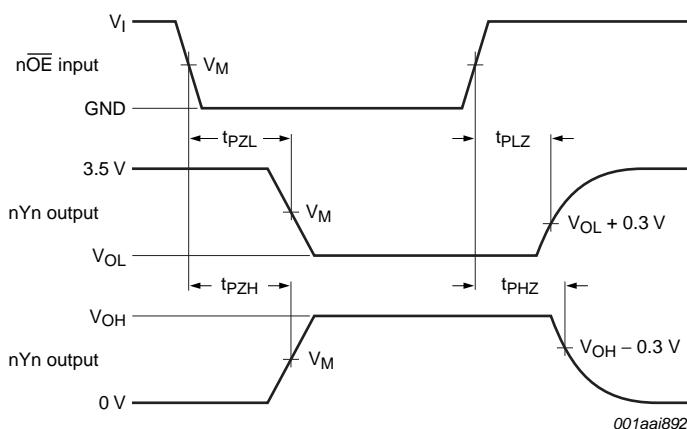
## 11. Waveforms



$V_M = 1.5 \text{ V}$

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 4. Input (nAn) to output (nYn) propagation delay**

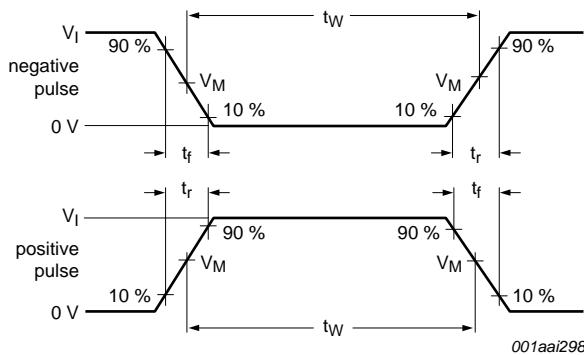


$V_M = 1.5 \text{ V}$

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

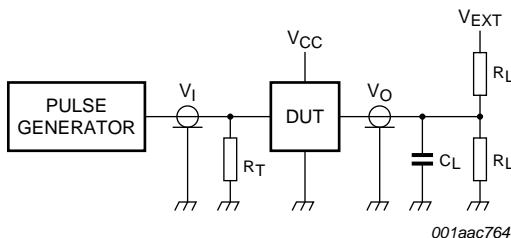
**Fig 5. 3-state output enable and disable times**

## 12. Test information



$$V_M = 1.5 \text{ V}$$

### a. Input pulse definition



Test data is given in [Table 8](#).

Definitions test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

### b. Test circuit for 3-state outputs

**Fig 6. Load circuitry for switching times**

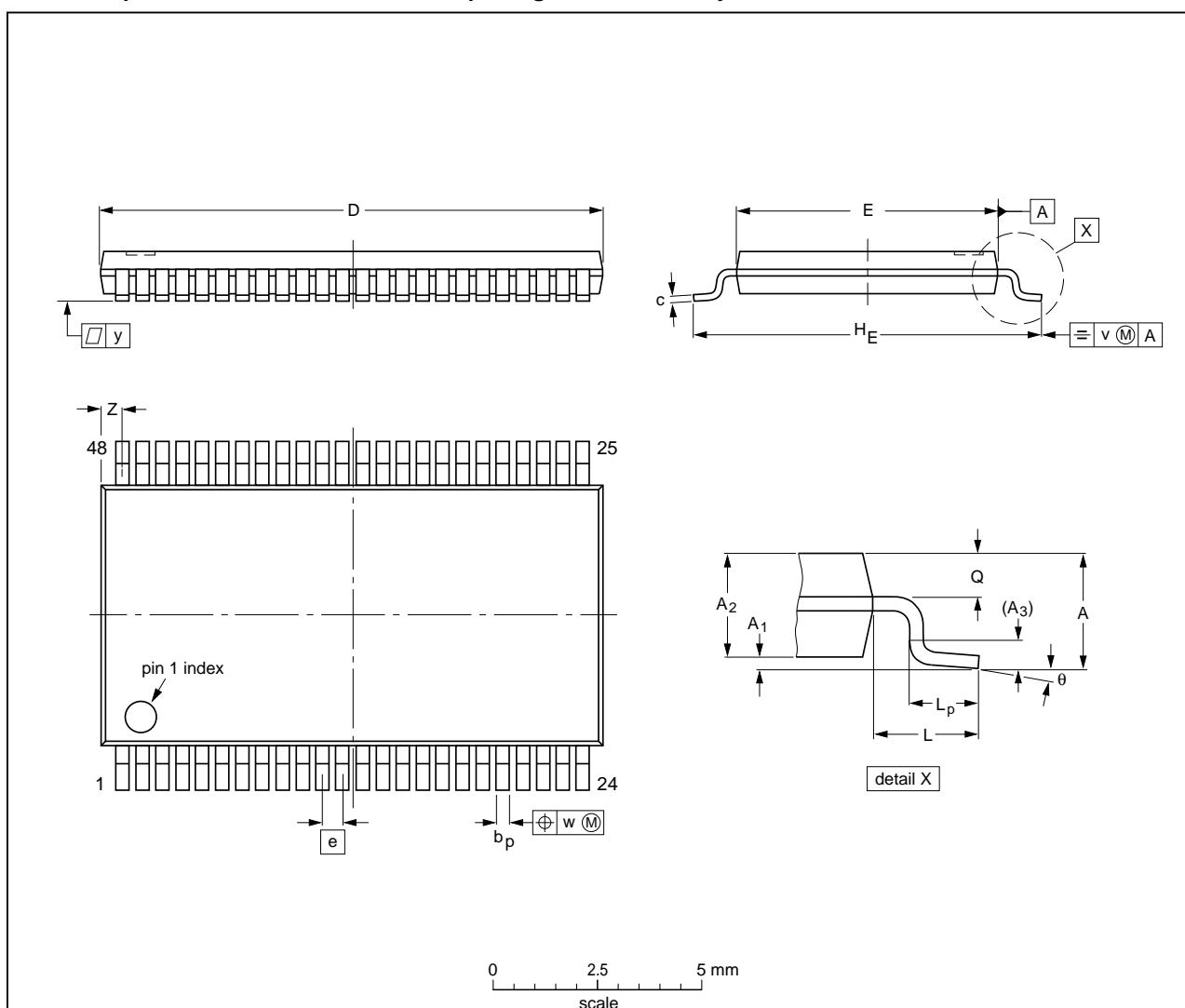
**Table 8. Test data**

Input				Load			$V_{EXT}$		
$V_I$	$f_i$	$t_W$	$t_r, t_f$	$C_L$	$R_L$		$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
3.0 V	1 MHz	500 ns	2.5 ns	50 pF	500 $\Omega$	open	7.0 V	open	

## 13. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



### DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z	θ
mm	1.2 0.05	0.15 0.85	1.05	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

### Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT362-1		MO-153			99-12-27 03-02-19

Fig 7. Package outline SOT362-1 (TSSOP48)

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

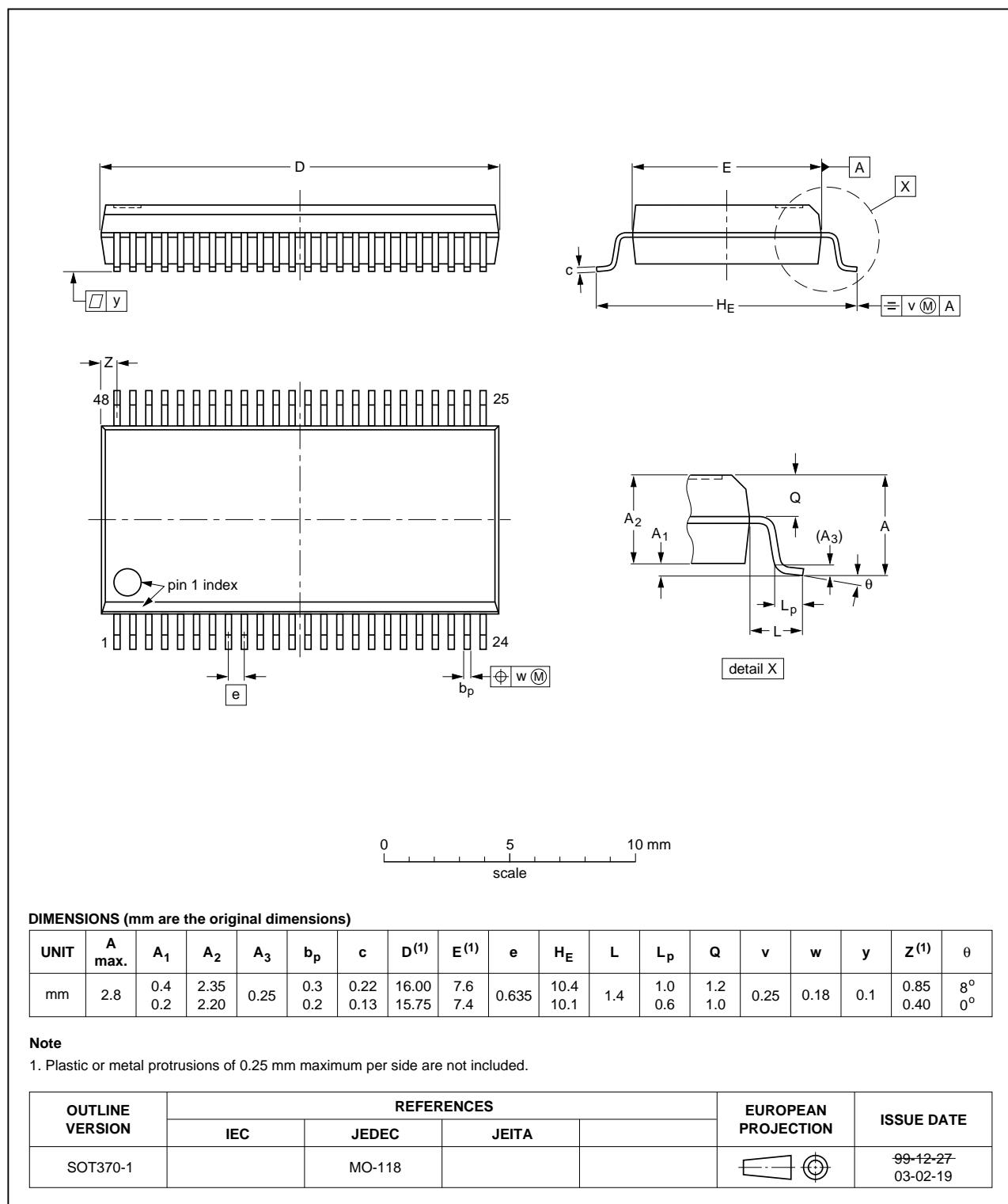


Fig 8. Package outline SOT370-1 (SSOP48)

## 14. Revision history

**Table 9. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT16244A v.8	20111103	Product data sheet	-	74ABT16244A v.7
Modifications:		• Legal pages updated		
74ABT16244A v.7	20100525	Product data sheet	-	74ABT16244A v.6
74ABT16244A v.6	20090323	Product data sheet	-	74ABT16244A v.5
74ABT16244A v.5	20060210	Product data sheet	-	74ABT_H16244A v.4
74ABT_H16244A v.4	19981007	Product specification	-	74ABT_H16244A v.3
74ABT_H16244A v.3	19980225	Product specification	-	74ABT_H16244A v.2

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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