19-1977; Rev 4; 1/09

0.5Ω/0.8Ω Low-Voltage, Dual SPDT Analog Switches in UCSP

General Description

The MAX4684/MAX4685 low on-resistance (R_{ON}), low-voltage, dual single-pole/double-throw (SPDT) analog switches operate from a single +1.8V to +5.5V supply. The MAX4684 features a 0.5Ω (max) R_{ON} for its NC switch and a 0.8Ω (max) R_{ON} for its NO switch at a +2.7V supply. The MAX4685 features a 0.8Ω max on-resistance for both NO and NC switches at a +2.7V supply.

Both parts feature break-before-make switching action (2ns) with t_{ON} = 50ns and t_{OFF} = 40ns at +3V. The digital logic inputs are 1.8V logic-compatible with a +2.7V to +3.3V supply.

The MAX4684/MAX4685 are packaged in the chipscale package (UCSP)™, significantly reducing the required PC board area. The chip occupies only a 2.0mm × 1.50mm area. The 4 × 3 array of solder bumps are spaced with a 0.5mm bump pitch.

Features

- **12-Bump, 0.5mm-Pitch UCSP**
- **NC Switch R_{ON}**
  0.5Ω max (+2.7V Supply) (MAX4684)
  0.8Ω max (+2.7V Supply) (MAX4685)
- **NO Switch R_{ON}**
  0.8Ω max (+2.7V Supply)
- **R_{ON} Match Between Channels**
  0.06Ω (max)
- **R_{ON} Flatness Over Signal Range**
  0.15Ω (max)
- **+1.8V to +5.5V Single-Supply Operation**
- **Rail-to-Rail Signal Handling**
- **1.8V Logic Compatibility**
- **Low Crosstalk: -68dB (100kHz)**
- **High Off-Isolation: -64dB (100kHz)**
- **THD: 0.03%**
- **50nA (max) Supply Current**
- **Low Leakage Currents**
  1nA (max) at T_A = +25°C

Applications

Speaker Headset Switching
MP3 Players
Power Routing
Battery-Operated Equipment
Relay Replacement
Audio and Video Signal Routing
Communications Circuits
PCMCIA Cards
Cellular Phones
Modems

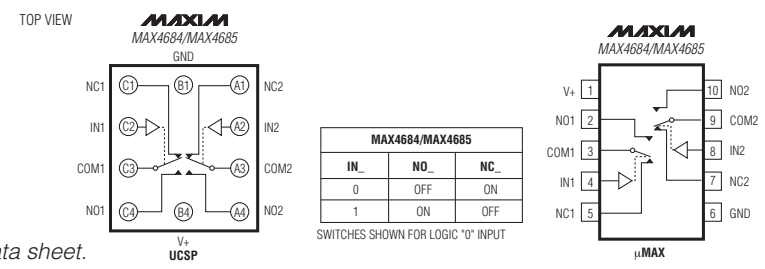
UCSP is a trademark of Maxim Integrated Products, Inc.
µMAX is a registered trademark of Maxim Integrated Products, Inc.

Ordering Information

PART	TEMP RANGE	PIN/BUMP-PACKAGE	TOP MARK
MAX4684EBC+T	-40°C to +85°C	12 UCSP*	AAF
MAX4684ETB+T	-40°C to +85°C	10 TDFN-EP**	AAG
MAX4684EUB+T	-40°C to +85°C	10 µMAX®	—
MAX4685EBC+T	-40°C to +85°C	12 UCSP*	AAG
MAX4685ETB+T	-40°C to +85°C	10 TDFN-EP**	AAH
MAX4685EUB+T	-40°C to +85°C	10 µMAX	—

+Denotes a lead(Pb)-free/RoHS-compliant package.
***Note:** Requires special solder temperature profile described in the Absolute Maximum Ratings section.*
**UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. Refer to the UCSP Reliability Notice in the UCSP Reliability section of this data sheet for more information.*
***EP = Exposed Pad*
T = Tape and reel.

Pin Configurations/Functional Diagrams/Truth Table



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0.5Ω/0.8Ω Low-Voltage, Dual SPDT Analog Switches in UCSP

ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND)
V+, IN_.....-0.3V to +6V
COM_, NO_, NC_ (Note1) ..... -0.3V to (V+ + 0.3V)
Continuous Current NO_, NC_, COM_ ..... ±300mA
Peak Current NO_, NC_, COM_
(pulsed at 1ms, 50% duty cycle).....±400mA
Peak Current NO_, NC_, COM_
(pulsed at 1ms, 10% duty cycle).....±500mA

Continuous Power Dissipation (T_A = +70°C)
10-Pin TDFN (derate 18.5mW/°C above +70°C).....1482mW
12-Bump UCSP (derate 11.4mW/°C above +70°C) ...909mW
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
Operating Temperature Ranges.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Bump Temperature (soldering) (Note 2)
Infared (15s).....+220°C
Vapor Phase (60s) .....+215°C

Note 1: Signals on NO_, NC_, and COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Note 2: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—+3V SUPPLY

(V+ = +2.7V to +3.3V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at +3V and +25°C.) (Notes 3, 9, 10)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	$V_{NO\_}$, $V_{NC\_}$, $V_{COM\_}$			E	0		V+	V
NC_ On-Resistance (Note 4)	$R_{ON(NC)}$	V+ = 2.7V; $I_{COM\_}$ = 100mA; $V_{NC\_}$ = 0 to V+	MAX4684	+25°C		0.3	0.5	Ω
				E			0.5	
			MAX4685	+25°C		0.45	0.8	
				E			0.8	
NO_ On-Resistance (Note 4)	$R_{ON(NO)}$	V+ = 2.7V; $I_{COM\_}$ = 100mA; $V_{NO\_}$ = 0 to V+		+25°C		0.45	0.8	Ω
				E			0.8	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR_{ON}	V+ = 2.7V; $I_{COM\_}$ = 100mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.5V		+25°C			0.06	Ω
				E			0.06	
NC_ On-Resistance Flatness (Note 6)	$R_{FLAT (NC)}$	V+ = 2.7V; I_{COM} = 100mA; $V_{NC\_}$ = 0 to V+	MAX4684	E			0.15	Ω
			MAX4685	E			0.35	
NO_ On-Resistance Flatness (Note 6)	$R_{FLAT (NO)}$	V+ = 2.7V; I_{COM} = 100mA; $V_{NO\_}$ = 0 to V+		E			0.35	Ω
NO_ or NC_ Off-Leakage Current (Note 7)	$I_{NO\_}$(OFF) or $I_{NC\_}$(OFF)	V+ = 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 3V, 0.3V; $V_{COM\_}$ = 0.3V, 3V		+25°C	-1		1	nA
				E	-10		10	
COM_ On-Leakage Current (Note 7)	$I_{COM\_}$(ON)	V+ = 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 3V, 0.3V, or unconnected; $V_{COM\_}$ = 3V, 0.3V, or unconnected		+25°C	-2		2	nA
				E	-20		20	
DYNAMIC CHARACTERISTICS								
Turn-On Time	t_{ON}	V+ = 2.7V, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V; R_L = 50Ω; C_L = 35pF; Figure 2		+25°C		30	50	ns
				E			60	

ELECTRICAL CHARACTERISTICS—+3V SUPPLY (continued)

(V+ = +2.7V to +3.3V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at +3V and +25°C.) (Notes 3, 9, 10)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Turn-Off Time	t_{OFF}	V+ = 2.7V, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V; R_L = 50Ω; C_L = 35pF; Figure 2	+25°C		25	30	ns
			E			40	
Break-Before-Make Delay	t_{BBM}	V+ = 2.7V, $V_{NO\_}$, or $V_{NC\_}$ = 1.5V; R_L = 50Ω; C_L = 35pF; Figure 3	E	2	15		ns
Charge Injection	Q	COM_ = 0; R_S = 0; C_L = 1nF; Figure 4	+25°C		200		pC
Off-Isolation (Note 8)	V_{ISO}	C_L = 5pF; R_L = 50Ω; f = 100kHz; $V_{COM\_}$ = $1V_{RMS}$; Figure 5	+25°C		-64		dB
Crosstalk	V_{CT}	C_L = 5pF; R_L = 50Ω; f = 100kHz; $V_{COM\_}$ = $1V_{RMS}$; Figure 5	+25°C		-68		dB
Total Harmonic Distortion	THD	R_L = 600Ω, IN_ = 2Vp-p, f = 20Hz to 20kHz	+25°C		0.03		%
NC_ Off-Capacitance	$C_{NC\_(OFF)}$	f = 1MHz; Figure 6	+25°C		84		pF
NO_ Off-Capacitance	$C_{NO\_(OFF)}$	f = 1MHz; Figure 6	+25°C		37		pF
NC_ On-Capacitance	$C_{NC\_(ON)}$	f = 1MHz; Figure 6	+25°C		190		pF
NO_ On-Capacitance	$C_{NO\_(ON)}$	f = 1MHz; Figure 6	+25°C		150		pF
DIGITAL I/O							
Input Logic High	V_{IH}		E	1.4			V
Input Logic Low	V_{IL}		E			0.5	V
IN_ Input Leakage Current	$I_{IN\_}$	$V_{IN\_}$ = 0 or V+	E	-1		1	µA
POWER SUPPLY							
Power-Supply Range	V+		E	1.8		5.5	V
Supply Current (Note 4)	I+	V+ = 5.5V; $V_{IN\_}$ = 0 or V+	+25°C	-50	0.04	50	nA
			E	-200		200	

Note 3: The algebraic convention used in this data sheet is where the most negative value is a minimum and the most positive value a maximum.

Note 4: Guaranteed by design.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$, between NC1 and NC2 or between NO1 and NO2.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Leakage parameters are 100% tested at T_A = +85°C, and guaranteed by correlation over rated temperature range.

Note 8: Off-isolation = $20\log_{10} (V_{COM} / V_{NO})$, V_{COM} = output, V_{NO} = input to off switch.

Note 9: UCSP and TDFN parts are 100% tested at +25°C only and guaranteed by design and correlation at the full hot-rated temperature.

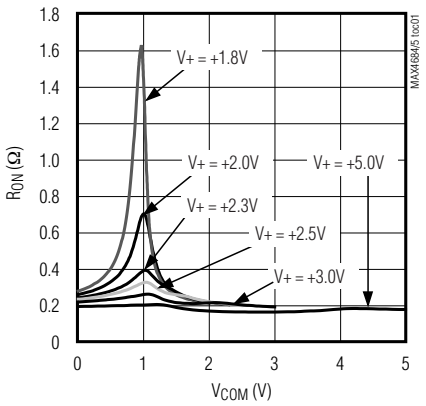
Note 10: -40°C specifications are guaranteed by design.

0.5Ω/0.8Ω Low-Voltage, Dual SPDT Analog Switches in UCSP

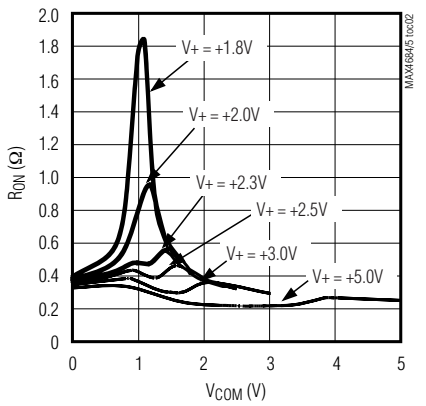
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

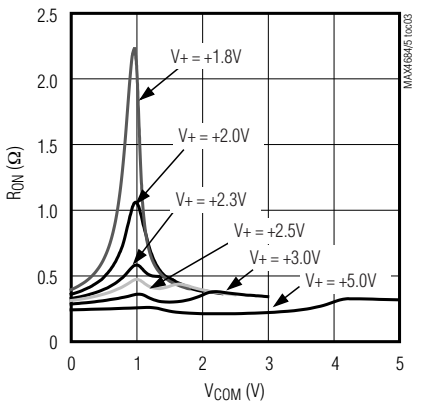
MAX4684
NC ON-RESISTANCE vs. COM VOLTAGE



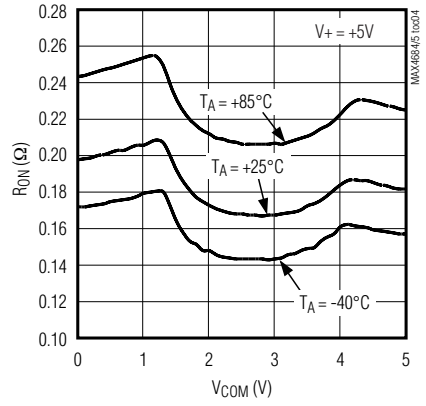
MAX4685
NC ON-RESISTANCE vs. COM VOLTAGE



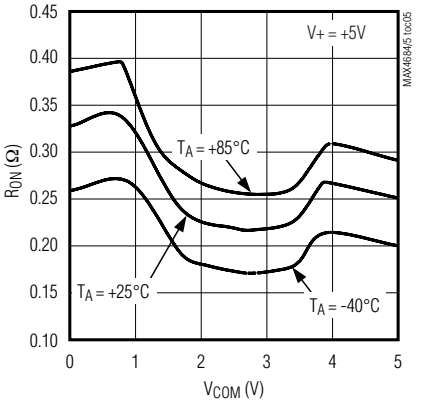
NO ON-RESISTANCE vs. COM VOLTAGE



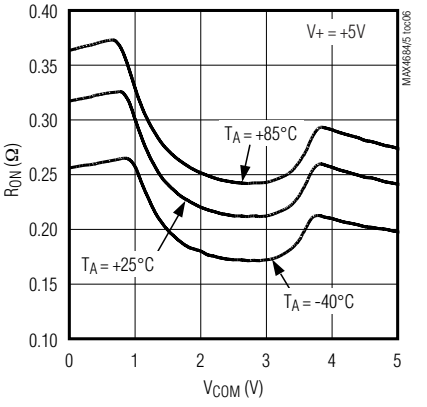
MAX4684
NC ON-RESISTANCE vs. COM VOLTAGE



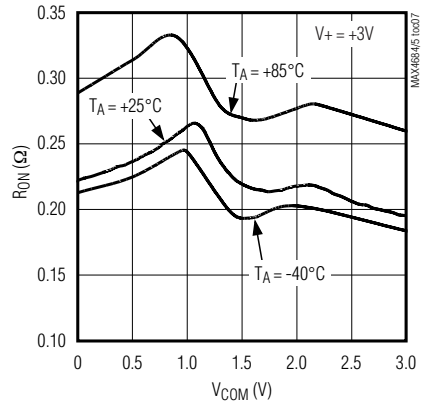
MAX4685
NC ON-RESISTANCE vs. COM VOLTAGE



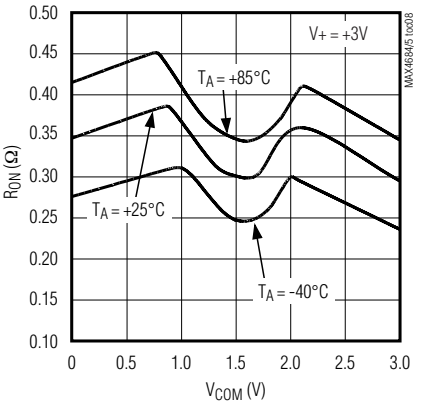
NO ON-RESISTANCE vs. COM VOLTAGE



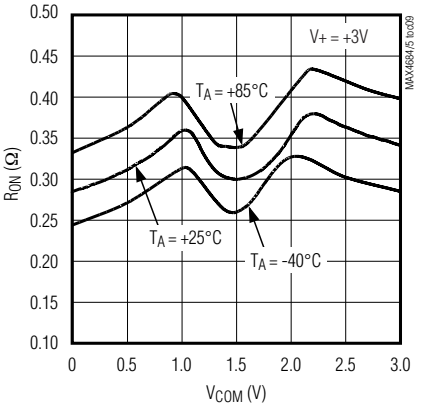
MAX4684
NC ON-RESISTANCE vs. COM VOLTAGE



MAX4685
NC ON-RESISTANCE vs. COM VOLTAGE



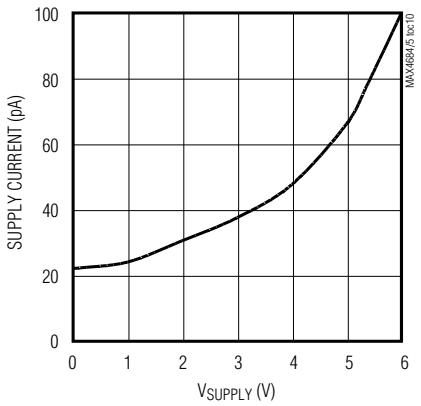
NO ON-RESISTANCE vs. COM VOLTAGE



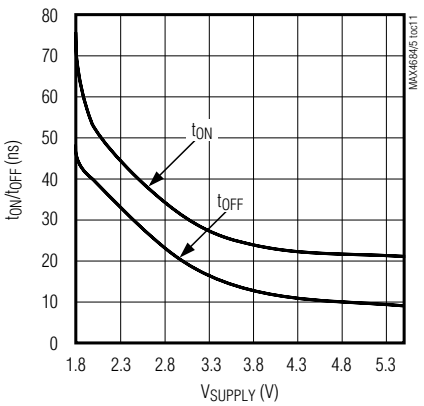
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

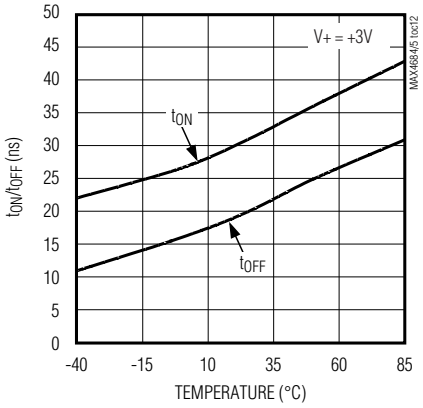
SUPPLY CURRENT vs. SUPPLY VOLTAGE



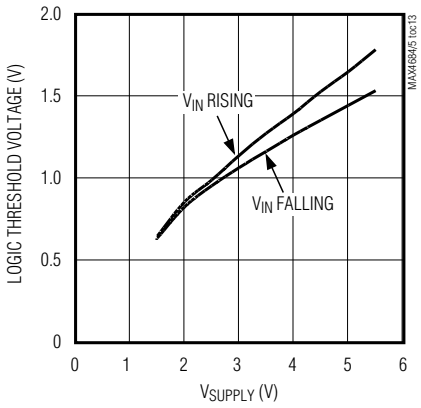
TURN-ON/TURN-OFF TIMES vs. SUPPLY VOLTAGE



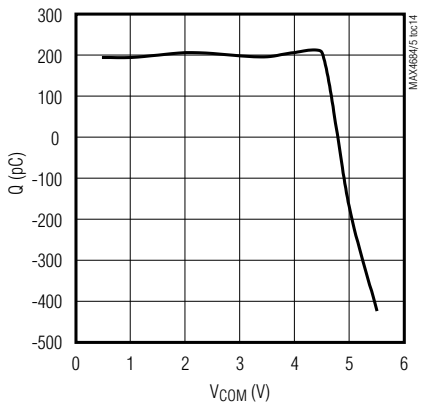
TURN-ON/TURN-OFF TIMES vs. TEMPERATURE



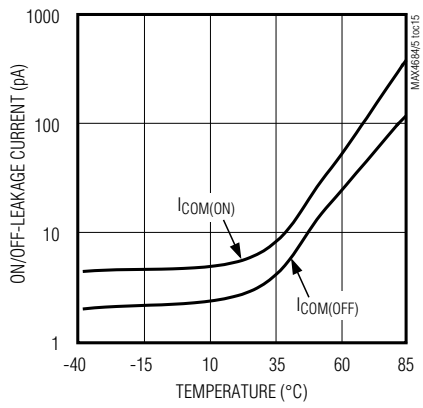
LOGIC THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



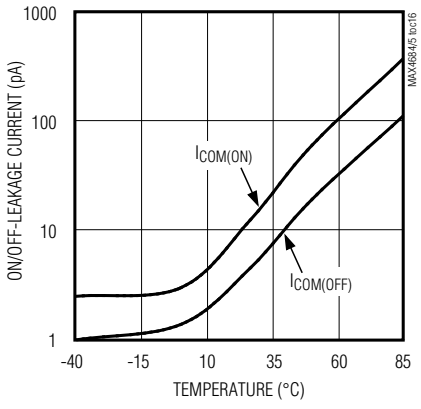
CHARGE INJECTION vs. COM VOLTAGE



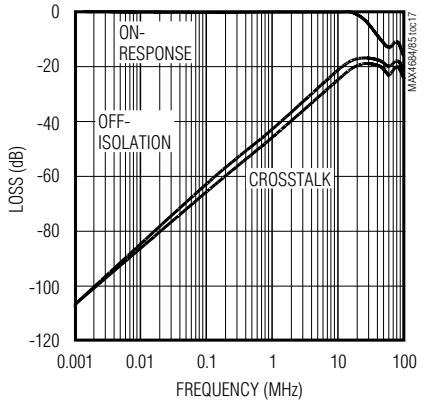
MAX4684 ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



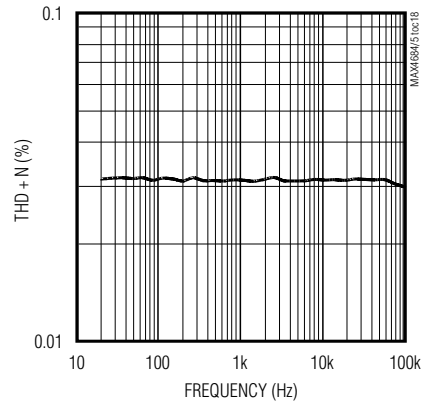
MAX4685 ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



FREQUENCY RESPONSE (µMAX)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



0.5Ω/0.8Ω Low-Voltage, Dual SPDT Analog Switches in UCSP

Pin Description

NAME	PIN		FUNCTION
	UCSP	µMAX/TDFN	
NC_	A1, C1	5, 7	Analog Switch—Normally Closed Terminal
IN_	A2, C2	4, 8	Digital Control Input
COM_	A3, C3	3, 9	Analog Switch—Common Terminal
NO_	A4, C4	2, 10	Analog Switch—Normally Open Terminal
V+	B4	1	Positive Supply Voltage Input
GND	B1	6	Ground
EP	—	—	Exposed Pad. Connect EP to GND (for TDFN only.)

Detailed Description

The MAX4684/MAX4685 are low on-resistance, low-voltage, dual SPDT analog switches that operate from a +1.8V to +5.5V supply. The devices are fully specified for nominal 3V applications. The MAX4684/MAX4685 have break-before-make switching and fast switching speeds (t_{ON} = 50ns max, t_{OFF} = 40ns max).

The MAX4684 offers asymmetrical normally closed (NC) and normally open (NO) R_{ON} for applications that require asymmetrical loads (examples include speaker headsets and internal speakers). The part features a 0.5Ω max R_{ON} for its NC switch and a 0.8Ω max RON for its NO switch at the 2.7V supply. The MAX4685 features a 0.8Ω max on-resistance for both NO and NC switches at the +2.7V supply.

Applications Information

Digital Control Inputs

The MAX4684/MAX4685 logic inputs accept up to +5.5V regardless of supply voltage. For example, with a +3.3V supply, IN_ may be driven low to GND and high to 5.5V. Driving IN_ rail-to-rail minimizes power consumption. Logic levels for a +1.8V supply are 0.5V (low) and 1.4V (high).

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) are passed with very little change in on-resistance (see *Typical Operating Characteristics*). The switches are bidirectional, so the NO_, NC_, and COM_ pins can be either inputs or outputs.

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to <20mA, add a small signal diode (D1) as shown in Figure 1. Adding a protection diode reduces the analog range to a diode drop (about 0.7V) below V+ (for D1). R_{ON} increases slightly at low supply voltages. Maximum supply voltage (V+) must not exceed +6V. Protection diode D1 also protects against some overvoltage situations. No damage will result on Figure 1's circuit if the supply voltage is below the absolute maximum rating applied to an analog signal pin.

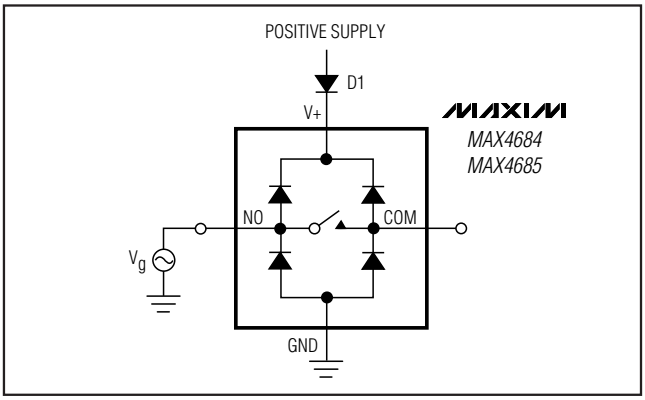


Figure 1. Overvoltage Protection Using Two External Blocking Diodes

0.5Ω/0.8Ω Low-Voltage, Dual SPDT Analog Switches in UCSP

UCSP Package Consideration

For general UCSP package information and PC layout considerations, please refer to the Maxim Application Note (Wafer-Level Ultra-Chip-Board-Scale Package).

UCSP Reliability

The chip-scale package (UCSP) represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a UCSP package. Performance through Operating Life Test and Moisture Resistance remains uncompromised as it is primarily determined by the wafer-fabrication process.

Mechanical stress performance is a greater consideration for a UCSP package. UCSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder joint contact integrity must be considered. Information on Maxim's qualification plan, test data, and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at www.maxim-ic.com.

Chip Information

PROCESS: BiCMOS

Test Circuits/Timing Diagrams

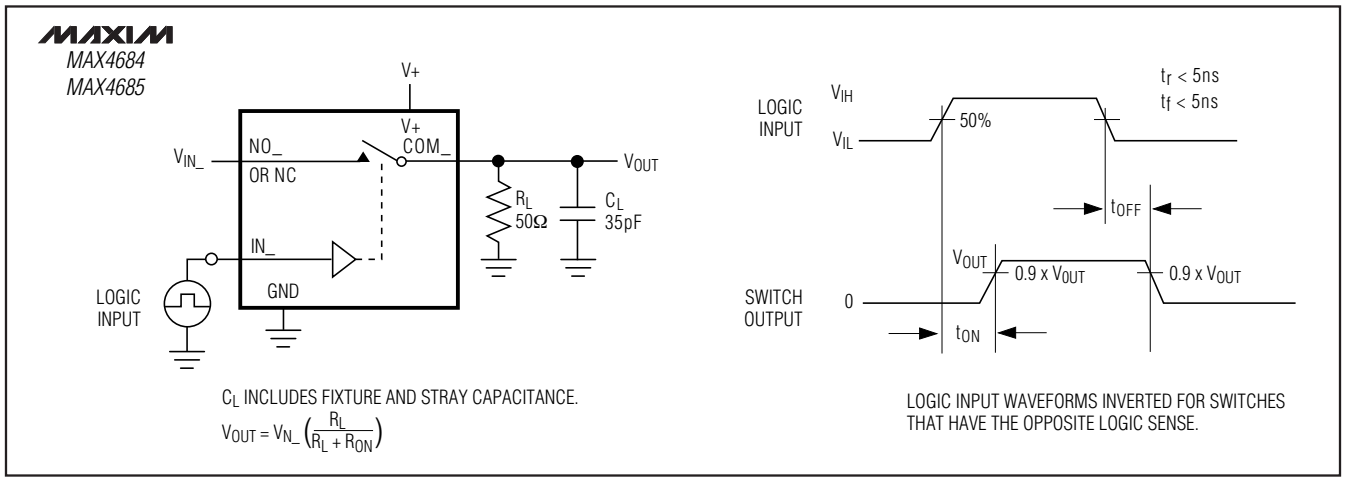


Figure 2. Switching Time

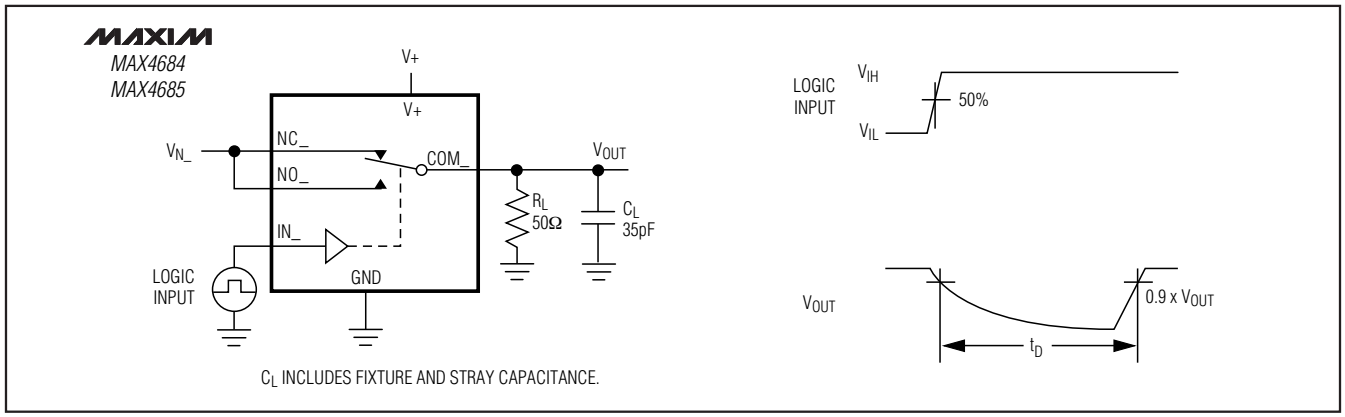


Figure 3. Break-Before-Make Interval

0.5Ω/0.8Ω Low-Voltage, Dual SPDT Analog Switches in UCSP

Test Circuits/Timing Diagrams (continued)

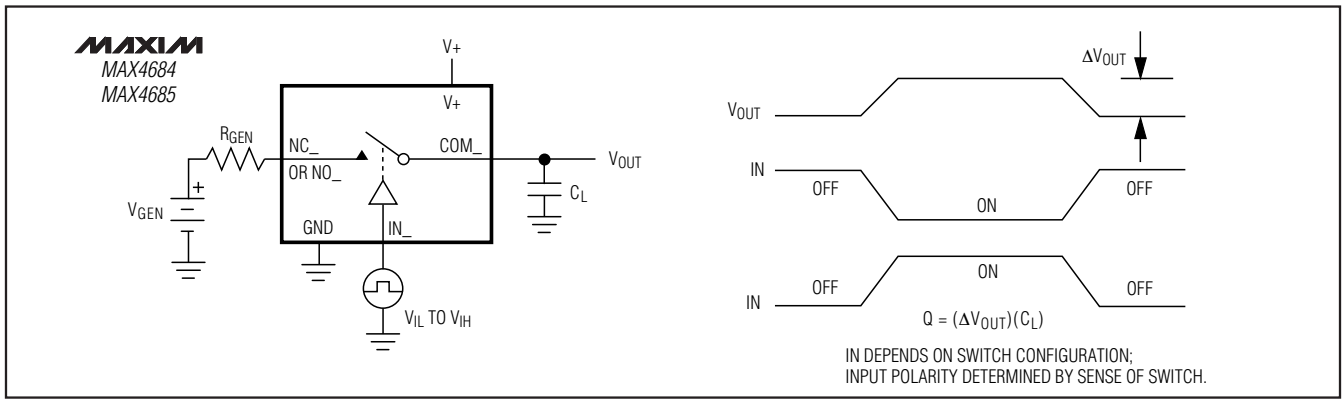


Figure 4. Charge Injection

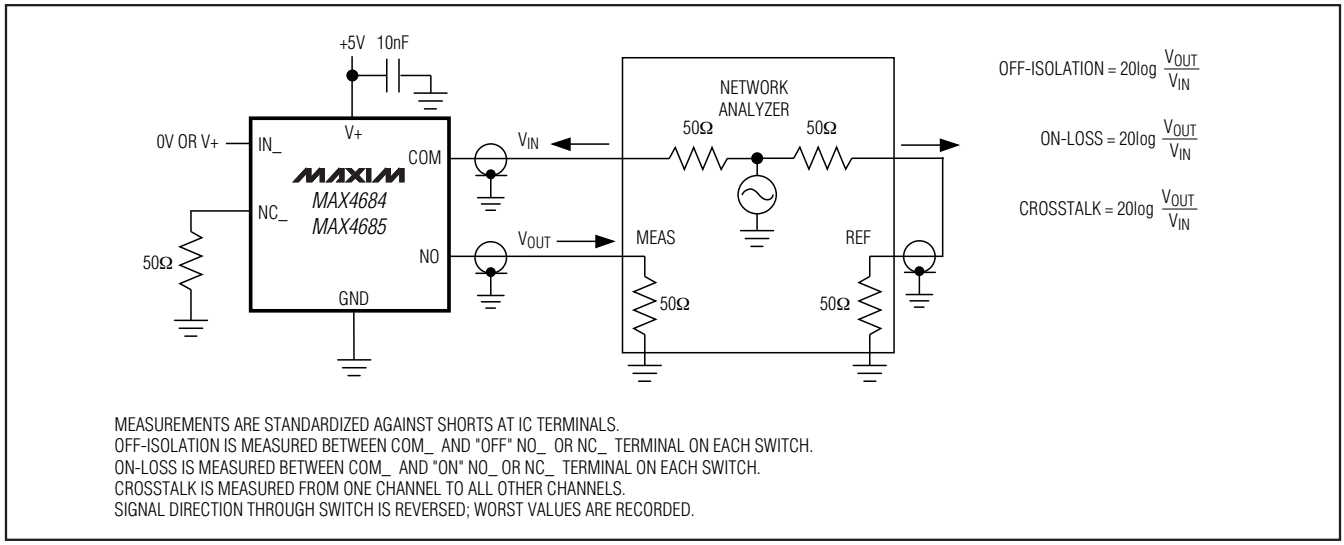


Figure 5. On-Loss, Off-Isolation, and Crosstalk

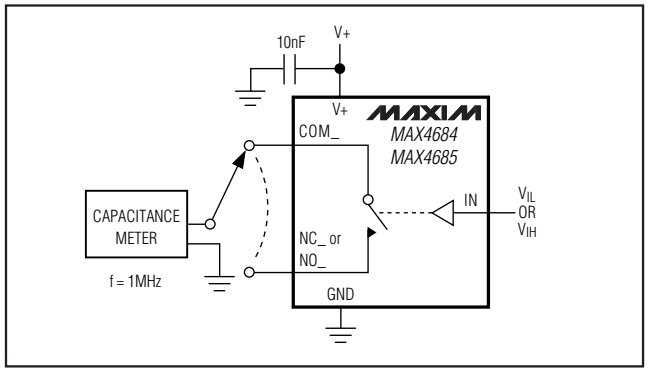
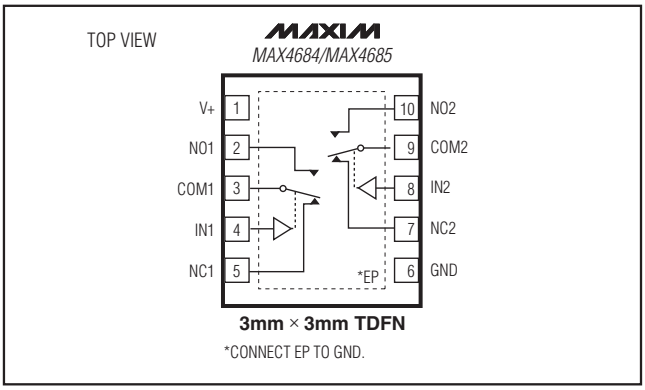


Figure 6. Channel Off/On-Capacitance

Pin Configurations (continued)



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
12 UCSP	B12-4	**21-0104**
10 TDFN-EP	T1033-1	**21-0137**
10 µMAX	U10-2	**21-0061**

0.5Ω/0.8Ω Low-Voltage, Dual SPDT Analog Switches in UCSP

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGES
3	2/03	Added TDFN packaging, noted parts are now UCSP qualified	—
4	1/09	Added lead-free packaging and exposed pad note	1, 2, 6–9

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