# DLPR410 Configuration PROM

## 1 Features

- Pre-Programmed Xilinx® PROM Configures the DLPC410 DMD Digital Controller
- I/O Pins Compatible With 1.8 V to 3.3 V
- 1.8 V Core Supply Voltage
- –40°C to 85°C Operating Temperature Range

## 2 Applications

- Direct Imaging Lithography
- 3D Printing [SLA and SLS]
- 3D Machine Vision
- 3D Scanners for Robotics & Inspection Systems
- Dynamic Grayscale Laser Marking and Coding
- Industrial Printing
- High Speed Projection and Advanced Imaging
- Ablation and Repair Systems
- Microscopes

## 3 Description

The DLPR410 device is a programmed PROM used to properly configure the DLPC410 Controller to operate five different digital micromirror device (DMD) options: the DLP9000X, the DLP9000XUV, and the DLP6500 family (S600 and Type A packages). The firmware in this device enables the DLPC410 Controller to provide system data throughput rates up to 48 Gigabits per second (Gbps) with the options for random row addressing and Load4 capabilities. Often this family of chips is designed into high speed UV and NIR optical systems such as direct imaging lithography, 3D printing and laser marking equipment that need fast throughput and pixel accurate control.

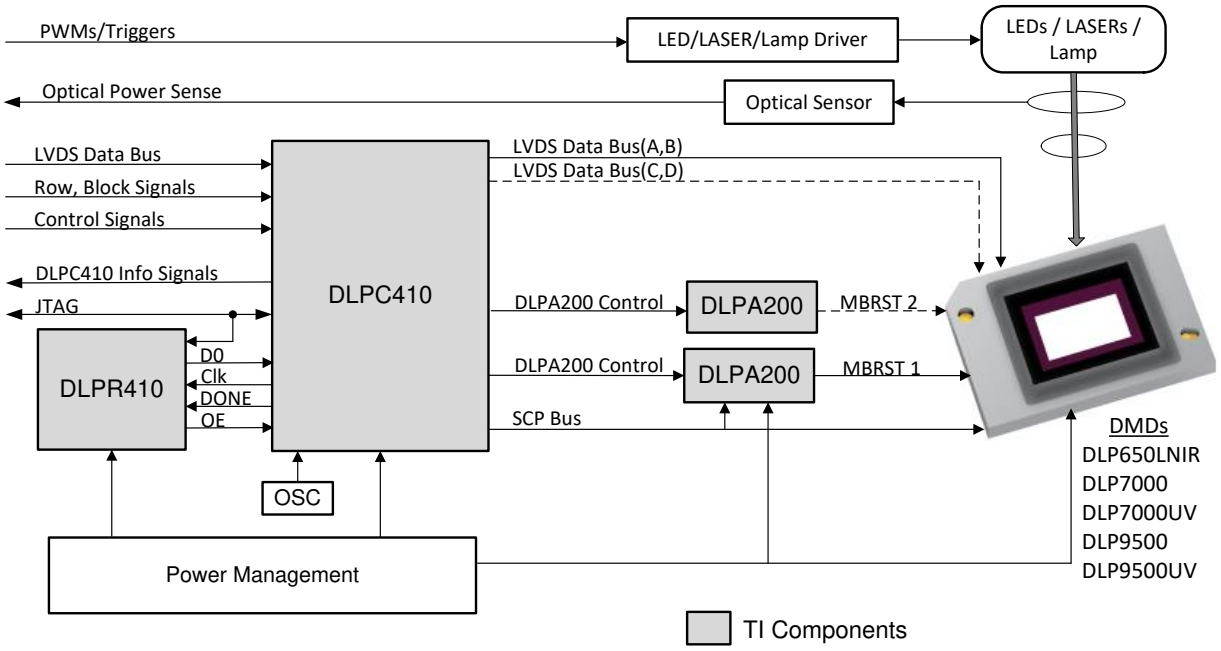
For complete electrical and mechanical specifications of the DLPR410, see the XCF16P product specification listed in Related Documentation.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| DLPR410 | DSBGA (48) | 8.00 mm × 9.00 mm × 1.20 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## 4 Simplified Application



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## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision E (December 2018) to Revision F** — **Page**

- Corrected spelling of Power Management in Simplified Application diagram. ... 1
- Corrected Max Tstg per Xilinx data sheet ... 6
- Pulled in specific layout information from referenced document and removed reference. ... 12
- Corrected DDC_Version(3:0) bus width to DDC_Version(2:0). ... 13
- Changed "Community" Resources Title to "Support" Resources ... 15

**Changes from Revision D (April 2015) to Revision E** — **Page**

- Updated *Applications* and *Description* to include new DLP650LNIR, removed data transfer rate ... 1
- Changed Application Diagram to include DLP650LNIR DMD ... 1
- Corrected Min Tstg per Xilinx data sheet ... 6
- Corrected Min VCCO per Xilinx data sheet ... 6
- Added support information for new DLP650LNIR DMD (multiple places) ... 8
- Updated Functional Block Diagram ... 8
- Corrected improper "DLPC910" reference to "DLPC410" ... 11
- Updated Figure 2 ... 11
- Added Device Compatibility table ... 13
- Updated Device Nomenclature ... 13
- Updated *Device Markings* section ... 13
- Added DLP650LNIR to Table 4 section ... 15
- Deleted DLP Discovery 4100 Chipset reference in Table 4 ... 15

**Changes from Revision C (March 2013) to Revision D** **Page**

- Updated *Features*, *Applications*, and *Description* ..... 1
- Deleted DLPR4101 (enhanced functionality PROM part number) throughout document ..... 1
- Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... 1
- Moved Block Diagram to new Typical Application section ..... 1
- Deleted 1.8 V and 3.3 V operation values from $V_{CCO}$, $V_{IL}$, and $V_{IH}$ - this implementation is 2.5 V ..... 6
- Changed Device Marking Image ..... 14
- Changed Device Marking Image ..... 14
- Deleted DLP® Discovery™ 4100 Chipset Datasheet from *Related Documentation* ..... 15
- Added Link to XCF16P data sheet at xilinx.com ..... 15

**Changes from Revision B (March 2013) to Revision C** **Page**

- Added Top View of Device ..... 1
- Added DLPR4101 "Load 4" enhanced functionality to Features ..... 1
- Added DLPR410 and DLPR4101 (enhanced functionality PROM part number) to DLPR410 throughout document ..... 1
- Added a link to the data sheet ..... 1
- Added the Version column to the *Ordering Information* table ..... 4
- Updated DLPC and DLP7000 / DLP7000UV Embedded Example Block Diagram ..... 11
- Added DLPR4101YVA as equivalent to TI part number 2510442-0006 ..... 13
- Added Reference to DLPC410 data sheet ..... 13
- Added DLPR410 to Figure 4 ..... 13
- Added Top View of Device to device marking ..... 13
- Added DLP7000UV Related Documentation ..... 15
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- Changed the top-side marking in the *Ordering Information* table ..... 4

**Changes from Original (August 2012) to Revision A** **Page**

- Changed the device From: Product Preview To: Production ..... 1

# 6 Pin Configuration and Functions

**YVA Package**
**48-Pin DSBGA**
**Top View**

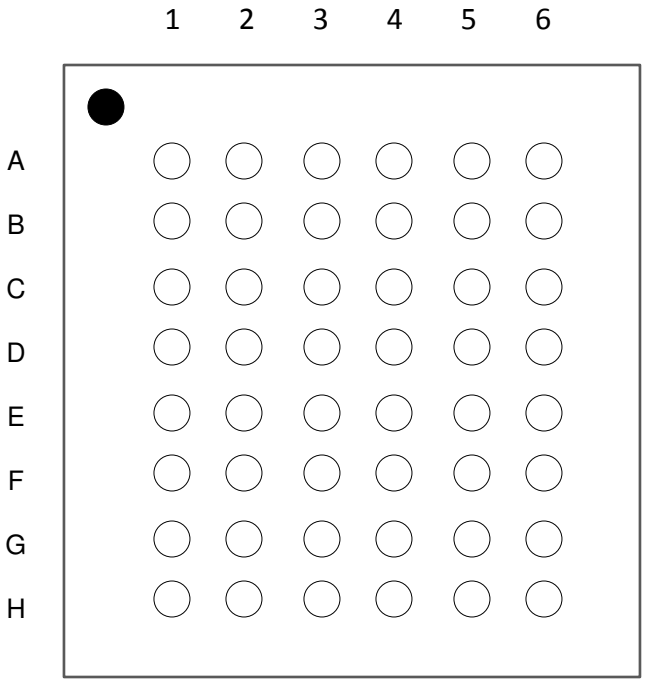



**Table 1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | A1 | G | Ground |
| GND | A2 | G | Ground |
| OE/$\overline{\text{RESET}}$ | A3 | I/O | Output Enable/$\overline{\text{RESET}}$ (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA and CLKOUT outputs are placed in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable. **Pin must be pulled High using an external 4.7-kΩ pull-up to $V_{CCO}$.** |
| DNC1 | A4 | — | Do Not Connect. Leave unconnected. |
| D6 | A5 | — | Do Not Connect. Leave unconnected. |
| D7 | A6 | — | Do Not Connect. Leave unconnected. |
| VCCINT1 | B1 | P | Positive 1.8-V supply voltage for internal logic. |
| VCCO1 | B2 | P | Positive 2.5-V supply voltage connected to the output voltage drivers and internal buffers. |
| CLK | B3 | I | Do Not Connect. Leave unconnected. |
| $\overline{\text{CE}}$ | B4 | I | Chip Enable Input. When $\overline{\text{CE}}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA and CLKOUT outputs are placed in a high impedance state. |
| D5 | B5 | — | Do Not Connect. Leave unconnected. |
| GND | B6 | G | Ground |
| BUSY | C1 | — | Do Not Connect. Leave unconnected. |
| CLKOUT | C2 | — | Configuration clock output. Each rising edge on the CLK input increments the internal address counter. **Pin must be pulled High and Low using an external 100-Ω pull-up to $V_{CCO}$ and an external 100-Ω pull-down to Ground. Place resistors close to pin.** |

(1) P = Power, G = Ground, I = Input, O = Output

**Table 1. Pin Functions (continued)**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DNC2 | C3 | — | Do Not Connect. Leave unconnected. |
| DNC3 | C4 | — | Do Not Connect. Leave unconnected. |
| D4 | C5 | — | Do Not Connect. Leave unconnected. |
| VCCO2 | C6 | P | Positive 2.5-V supply voltage connected to the output voltage drivers and internal buffers. |
| $\overline{CF}$ | D1 | I | Configuration pin. **The $\overline{CF}$ pin must be pulled High using an external 4.7-kΩ pull-up to $V_{CCO}$**. Selects serial mode configuration. |
| $\overline{CEO}$ | D2 | — | Do Not Connect. Leave unconnected. |
| DNC10 | D3 | — | Do Not Connect. Leave unconnected. |
| DNC11 | D4 | — | Do Not Connect. Leave unconnected. |
| D3 | D5 | — | Do Not Connect. Leave unconnected. |
| VCCO4 | D6 | P | Positive 2.5-V supply voltage connected to the output voltage drivers and internal buffers. |
| VCCINT2 | E1 | P | Positive 1.8-V supply voltage for internal logic. |
| TMS | E2 | I | JTAG Mode Select Input. TMS has an internal 50-kΩ resistive pull-up to $V_{CCJ}$. |
| DNC4 | E3 | — | Do Not Connect. Leave unconnected. |
| DNC5 | E4 | — | Do Not Connect. Leave unconnected. |
| D2 | E5 | — | Do Not Connect. Leave unconnected. |
| TDO | E6 | O | JTAG Serial Data Output. TDO has an internal 50-kΩ resistive pull-up to $V_{CCJ}$. |
| GND | F1 | G | Ground |
| DNC6 | F2 | — | Do Not Connect. Leave unconnected. |
| DNC7 | F3 | — | Do Not Connect. Leave unconnected. |
| DNC8 | F4 | — | Do Not Connect. Leave unconnected. |
| GND | F5 | G | Ground |
| GND | F6 | G | Ground |
| TDI | G1 | I | JTAG Serial Data Input. TDI has an internal 50k-Ω resistive pull-up to $V_{CCJ}$. |
| DNC9 | G2 | — | Do Not Connect. Leave unconnected. |
| REV_SEL0 | G3 | I | Revision Select [1:0] Inputs. When the $\overline{EN\_EXT\_SEL}$ is Low, the Revision Select pins are used to select the design revision to be enabled. The Revision Select [1:0] inputs have an internal 50-kΩ resistive pull-up to $V_{CCO}$. **The REV_SEL0 pin must be pulled Low using an external 10-kΩ pull-down to Ground**. **The REV_SEL1 pin must be connected to Ground**. |
| REV_SEL1 | G4 | I | |
| VCCO3 | G5 | P | Positive 2.5-V supply voltage connected to the output voltage drivers and internal buffers. |
| VCCINT3 | G6 | P | Positive 1.8-V supply voltage for internal logic. |
| GND | H1 | G | Ground |
| VCCJ | H2 | P | Positive 2.5-V JTAG I/O supply voltage connected to the TDO output voltage driver and TCK, TMS and TDI input buffers. |
| TCK | H3 | I | JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics. |
| $\overline{EN\_EXT\_SEL}$ | H4 | I | External Selection Input. $\overline{EN\_EXT\_SEL}$ has an internal 50-kΩ resistive pull- up to $V_{CCO}$. **The $\overline{EN\_EXT\_SEL}$ pin must be connected to Ground**. |
| D1 | H5 | — | Do Not Connect. Leave unconnected. |
| D0 | H6 | O | DATA output pin to provide data for configuring the DLPC410 in serial mode. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (see (1) (2))

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage | Relative to ground | –0.5 | 2.7 | V |
| $V_{CCO}$ | I/O supply voltage | Relative to ground | –0.5 | 4.0 | V |
| $V_{IN}$ | Input voltage with respect to ground | $V_{CCO}$ < 2.5 V | –0.5 | 3.6 | V |
| | | $V_{CCO}$ ≥ 2.5 V | –0.5 | 3.6 | V |
| $V_{TS}$ | Voltage applied to high-impedance output | $V_{CCO}$ < 2.5 V | –0.5 | 3.6 | V |
| | | $V_{CCO}$ ≥ 2.5 V | –0.5 | 3.6 | V |
| $T_J$ | Junction temperature | | | 125 | °C |
| $T_{stg}$ | Storage temperature, ambient | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA. During transitions, the device pins can undershoot to –2 V or overshoot to 7 V, provided this overshoot or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ (1) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2) (3) | 2000 | V |

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC Standard JESD22-A114A (C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CCINT}$ | Internal voltage supply | | 1.65 | 1.8 | 2.0 | V |
| $V_{CCO}$ | Supply voltage for output drivers | 2.5-V operation | 2.3 | 2.5 | 2.7 | V |
| $V_{IL}$ | Low-level input voltage | 2.5-V operation | 0 | | 0.7 | V |
| $V_{IH}$ | High-level input voltage | 2.5-V operation | 1.7 | | 3.6 | V |
| $V_O$ | Output voltage | | 0 | | $V_{CCO}$ | V |
| $t_{IN}$ | Input signal transition time (measured between 10% $V_{CCO}$ and 90% $V_{CCO}$) | | | | 500 | ns |
| $T_A$ | Operating ambient temperature | | –40 | | 85 | °C |

## 7.4 Thermal Information

Refer to the XCF16P product specifications at www.xilinx.com.

## 7.5 Electrical Characteristics

Refer to the XCF16P product specifications at www.xilinx.com.

## 7.6 Supply Voltage Requirements for Power-On Reset and Power-Down

(see (1))

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{VCC}$ | $V_{CCINT}$ rise time from 0 V to nominal voltage (2) | 0.2 | 50 | ms |
| $V_{CCPOR}$ | POR threshold for $V_{CCINT}$ supply | 0.5 | – | V |
| $t_{OER}$ | OE/$\overline{\text{RESET}}$ release delay following POR (3) | 0.5 | 30 | ms |
| $V_{CCPD}$ | Power-down threshold for $V_{CCINT}$ supply | | 0.5 | V |
| $t_{RST}$ | Time required to trigger a device reset when the $V_{CCINT}$ supply drops below the maximum $V_{CCPD}$ threshold | 10 | | ms |

(1) $V_{CCINT}$, $V_{CCO}$, and $V_{CCJ}$ supplies can be applied in any order.
(2) At power up, the device requires the $V_{CCINT}$ power supply to monotonically rise to the nominal operating voltage within the specified $T_{VCC}$ rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Figure 6, in the Xilinx XCF16P (v2.19) Product Specification for more information.
(3) If the $V_{CCINT}$ and $V_{CCO}$ supplies do not reach their respective recommended operating conditions before the OE/$\overline{\text{RESET}}$ pin is released, then the configuration data from the PROM is not available at the recommended threshold levels. The configuration sequence must be delayed until both $V_{CCINT}$ and $V_{CCO}$ have reached their recommended operating conditions.

## 7.7 Timing Requirements

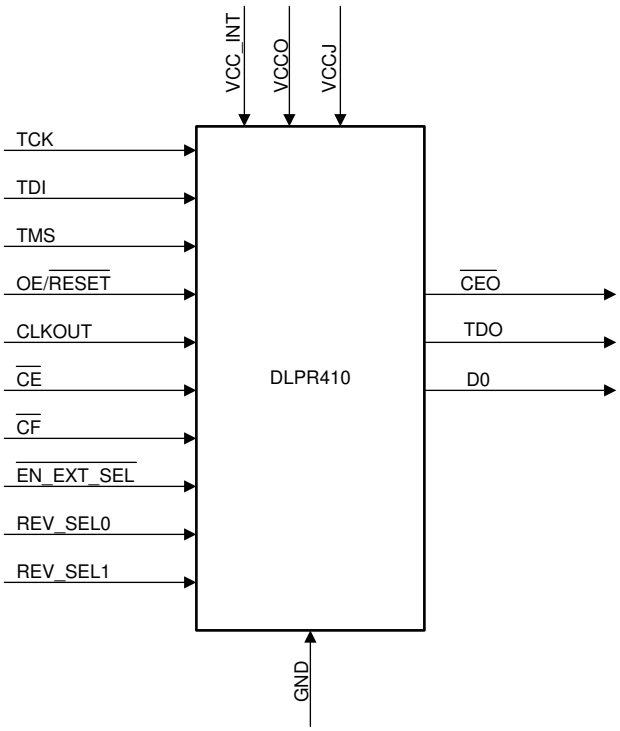
Refer to the XCF16P product specifications at www.xilinx.com.

# 8 Detailed Description

## 8.1 Overview

The configuration bit stream stored in the DLPR410 device supports reliable operation of the DLPC410 device with the DLP650LNIR, DLP7000, DLP7000UV, DLP9500, and DLP9500UV DMDs. The DLPC410 digital controller loads this configuration bit stream from the DLPR410 device.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Data Interface

#### *8.3.1.1 Data Outputs*

The DLPR410 device is configured for serial mode operation, where D0 is the data output pin. D0 output pin provides a serial connection to the DLPC410, where the configuration is read out by the DLPC410.

#### *8.3.1.2 Configuration Clock Input*

The configuration CLK is connected to the DLPC410 in Master Serial mode, where the DLPC410 provides the clock pulses to read the configuration from the DLPR410 device.

#### *8.3.1.3 Output Enable and Reset*

When the OE/$\overline{\text{RESET}}$ input is held low, the address counter is reset and the Data and CLKOUT outputs are placed in high-impedance state. **OE/$\overline{\text{RESET}}$ must be pulled High using an external 4.7-kΩ pull-up to $V_{CCO}$.**

## Feature Description (continued)

### 8.3.1.4 Chip Enable

The $\overline{CE}$ input is asserted by the DLPC410 to enable the Data and CLKOUT outputs. When $\overline{CE}$ is held high, the DLPR410 device address counter is reset, and the Data and CLKOUT outputs are placed in high-impedance states.

### 8.3.1.5 Configuration Pulse

The DLPR410 device is configured in serial mode when it holds configuration pulse pin, $\overline{CF}$, high and it enables the $\overline{CE}$ and OE pins. New data is available a short time after each rising clock edge.

### 8.3.1.6 Revision Selection

The device uses the REV_SEL_0, REV_SEL_1, and $\overline{EN\_EXT\_SEL}$ signals to select a revision to act as the default. Setting all three signals to GND defaults to revision 0 for simple DLPR410 device setup.

## 8.4 Device Functional Modes

To successfully program the DLPC410 upon power-up, the DLPR410 device must be configured and connected to the DLPC410 as shown in Figure 1.

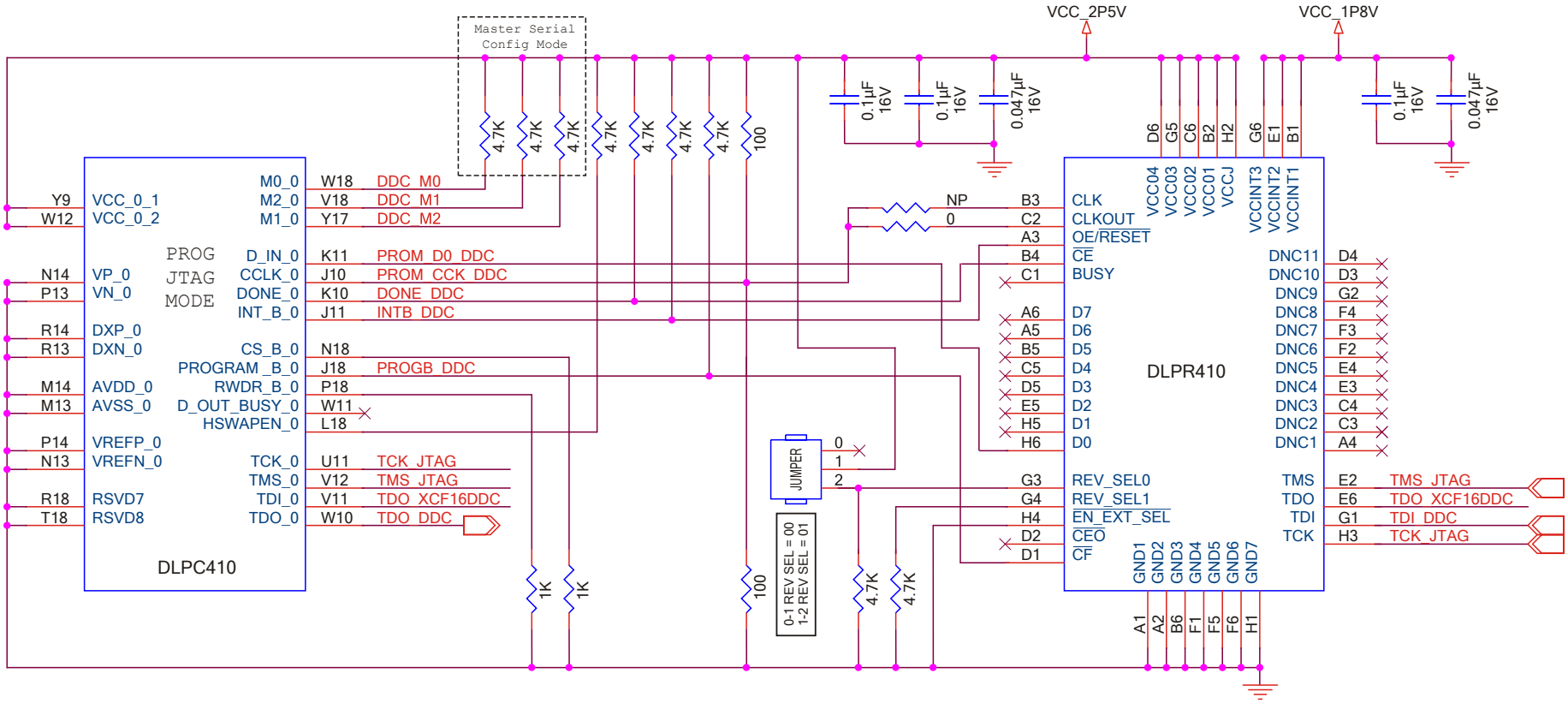



**Figure 1. DLPC410 and DLPR410 Connection Schematic**

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The DLPR410 device configuration PROM ships pre-programmed with configuration code for the DLPC410. Upon power-up, the DLPC410 and the DLPR410 device connect to enable configuration information to be sent from the DLPR410 device to the DLPC410, such that the DLPC410 can configure itself for proper operation within the application. Without the DLPR410 device properly connected to the DLPC410 in the application system, the DLPC410 does not boot and the system remains inoperable.

## 9.2 Typical Application

A typical embedded system application using the DLPR410 device to program the DLPC410 controller (to drive one of 5 different DMDs) is shown in Figure 2. For complete details of this typical application refer to the DLPC410 controller data sheet listed in *Table 4*.

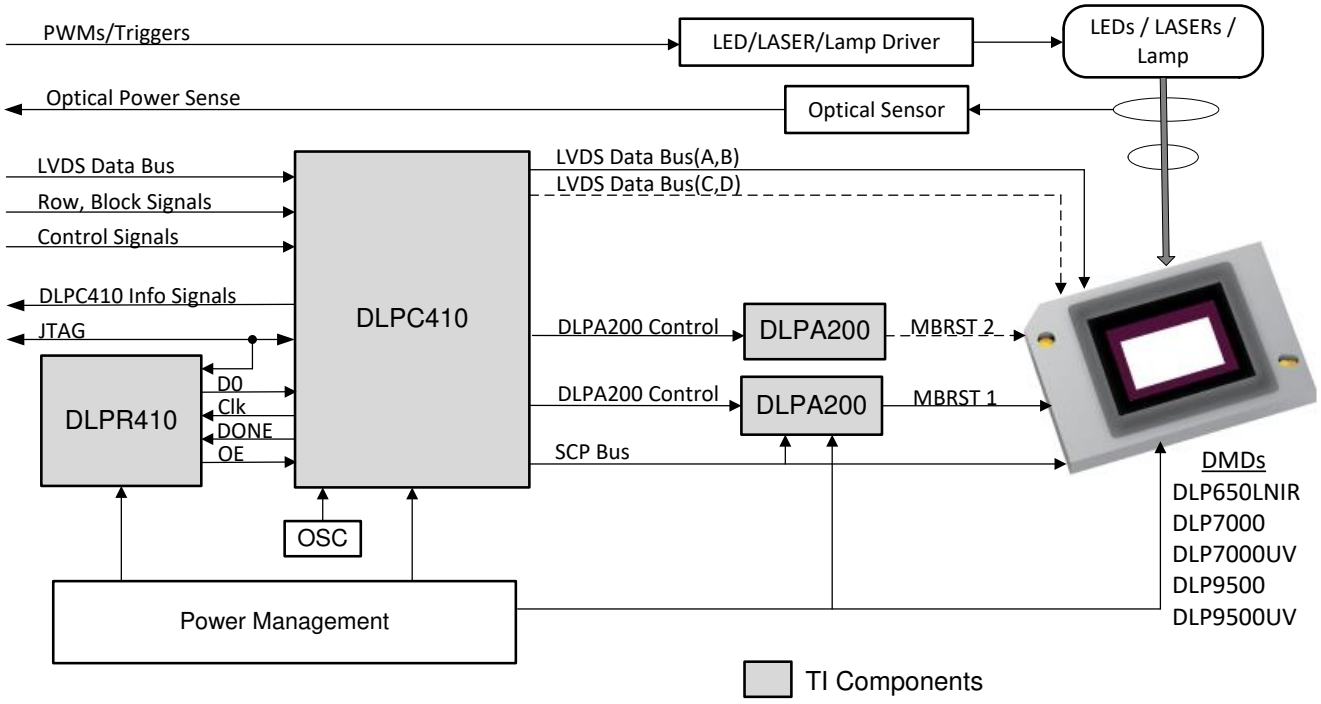



**Figure 2. DLPR410 and DLPC410 with DMD Example Block Diagram**

### 9.2.1 Design Requirements

The DLPR410 is part of a multi-chipset solution, and it is required to be coupled with the DLPC410 for reliable operation of the DLP650LNIR, DLP7000, DLP7000UV, DLP9500, and DLP9500UV DMDs. For more information, refer to the DLPC410 datasheet listed in *Related Documentation*.

# 10 Power Supply Recommendations

The DLPR410 uses two power supply rails as shown in Table 2.

**Table 2. DLPR410 Power Supply Rails**

| SUPPLY | POWER PINS | COMMENTS |
|---|---|---|
| 1.8 V | $V_{CCINT1}$, $V_{CCINT2}$, and $V_{CCINT3}$ | All $V_{CCINT}$ pins must be connected with a 0.1-µF decoupling capacitor to GND. |
| 2.5 V | $V_{CCO1}$,$V_{CCO2}$,$V_{CCO3}$, $V_{CCO4}$, and $V_{CCJ}$ | All $V_{CCO}$ and $V_{CCJ}$ pins must be connected with a 0.1-µF decoupling capacitor to GND. |

# 11 Layout

## 11.1 Layout Guidelines

The DLPR410 is part of a multi-chipset solution. It is required to be used with the DLPC410 Controller to provide reliable control of any attached DMDs. These guidelines are targeted at designing a PCB board with the DLPR410.

### 11.1.1 Component Placement

The DLPR410 should be placed adjacent to the DLPC410 Controller within a distance of about 4 inches.

### 11.1.2 Impedance Requirements

Signals between the DLPR410 and the DLPC410 Controller should be routed to have a matched impedance of 50 Ω ±10%.

### 11.1.3 PCB Signal Routing

When designing a PCB board which includes the DLPR410 and the DLPC410 Controller, the following are recommended:

Signal trace corners should be no sharper than 45°. Adjacent signal layers should have the predominate traces routed orthogonal to each other.

TI does not recommend signal routing on power or ground planes.

TI does not recommend ground plane slots.

High speed signal traces should not cross over slots in adjacent power and/or ground planes.

### 11.1.4 Fiducials

Fiducials for automatic component insertion should be 0.05-inch copper with a 0.1-inch cutout (antipad). Fiducials for optical auto insertion are placed on three corners of both sides of the PCB.

### 11.1.5 PCB Decoupling Guidelines

Decoupling capacitors should be utilized to provide instantaneous current sources to components, component decoupling capacitors, and to help avoid ground bounce.

#### *11.1.5.1 Bulk Decoupling*

Bulk decoupling capacitors for the board should be distributed around the PCB and should be sized to handle the current demands for the board.

##### 11.1.5.1.1 DLPR410 Decoupling Capacitors

Decoupling capacitors (0.1 µF recommended) should be placed to minimize the distance from the decoupling capacitor to the supply and ground pin of the component. It is recommended that the placement of and routing for the decoupling capacitors meet the following guidelines:

- The supply voltage pin of the capacitor should be located close to the device supply voltage pin(s). The

## Layout Guidelines (continued)

decoupling capacitor should have vias to ground and voltage planes. The device can be connected directly to the decoupling capacitor (no via) if the trace length is less than 0.1 inch. Otherwise, the component should be tied to the voltage or ground plane through separate vias.

- The trace lengths of the voltage and ground connections for decoupling capacitors and components should be less than 0.1 inch to minimize inductance.
- The trace width of the power and ground connection to decoupling capacitors and components should be as wide as possible to minimize inductance.
- Connecting decoupling capacitors to ground and power planes through multiple vias can reduce inductance and improve noise performance. Via sharing between components (discreet or integrated) is discouraged.
- Decoupling performance can be improved by utilizing low ESR and low ESL capacitors.

# 12 Device and Documentation Support

## 12.1 Device Support

### 12.1.1 Device Compatibility

| TI PART NUMBER | DDC_Version(2:0) (1) | Compatible DMDs (2) |
|---|---|---|
| DLPR410YVA | 5 | DLP7000BFLP, DLP7000UVFLP, DLP9500BFLN, DLP9500UVFLN |
| DLPR410AYVA | 7 | DLP650LNIRFYL, DLP7000BFLP, DLP7000UVFLP, DLP9500BFLN, DLP9500UVFLN |

(1) Refers to the DDC_Version(2:0) output pins of the DLPC410 Controller once configured by this Configuration PROM. See the DLPC410 datasheet (DLPS024) for more information.
(2) Refer to each individual DMD datasheet under Device and Documentation Support for more DMD information.

### 12.1.2 Device Nomenclature

The device nomenclature is as shown in Figure 3 The part number description for previous and currently available part numbers is shown in Table 3

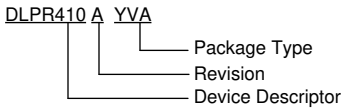



**Figure 3. Device Nomenclature**

**Table 3. Part Number Description**

| TI PART NUMBER | DESCRIPTION | REFERENCE NUMBER |
|---|---|---|
| DLPR410YVA | DLPR410 Configuration PROM | 2510442-0005 |
| DLPR410AYVA | DLPR410A Configuration PROM (Adds compatibility with DLP650LNIR) | DLPR410AYVA |

### 12.1.3 Device Markings

Figure 4 shows the previous device marking for the DLPR410 device. For the DLPR410A, this device marking nomenclature has been updated to use the DLPR410A device part number instead of the previous 2510442 marking, as shown in Figure 5.

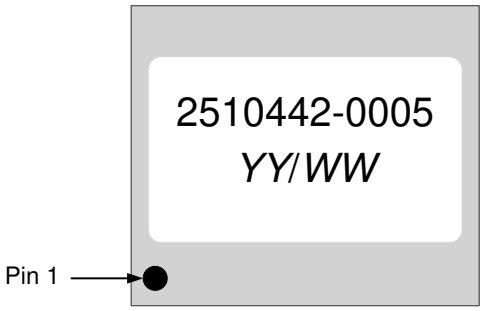



**Figure 4. DLPR410 Device Markings**

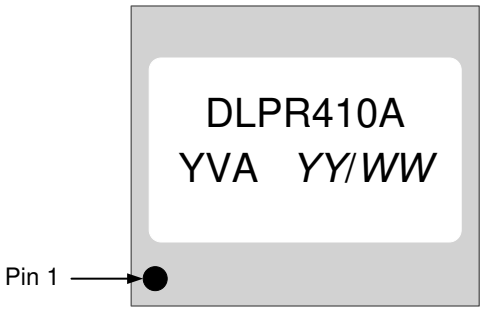



**Figure 5. DLPR410A Device Markings**

Where *YY/WW* is the year/week the part was programmed.

## 12.2 Documentation Support

### 12.2.1 Related Documentation

For related documentation, see the following:

**Table 4. Related Documentation**

| DOCUMENT | TI LITERATURE NUMBER |
|---|---|
| DLP650LNIR 0.65 NIR WXGA S450 DMD data sheet | DLPS136 |
| DLP7000 DLP 0.7 XGA 2xLVDS Type A DMD | DLPS026 |
| DLP7000UV DLP 0.7 UV XGA 2xLVDS Type-A DMD data sheet | DLPS061 |
| DLP9500 DLP 0.95 1080p 2xLVDS Type-A DMD data sheet | DLPS025 |
| DLP9500UV DLP 0.95 UV 1080p 2xLVDS Type-A DMD data sheet | DLPS033 |
| DLPA200 DMD Micromirror Driver data sheet | DLPS015 |
| DLPC410 DMD Digital Controller data sheet | DLPS024 |
| XCF16P data sheet | available at www.xilinx.com |

## 12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.
Xilinx is a registered trademark of Xilinx, Inc.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DLPR410AYVA | ACTIVE | DSBGA | YVA | 48 | 3 | TBD | Call TI | Call TI | | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

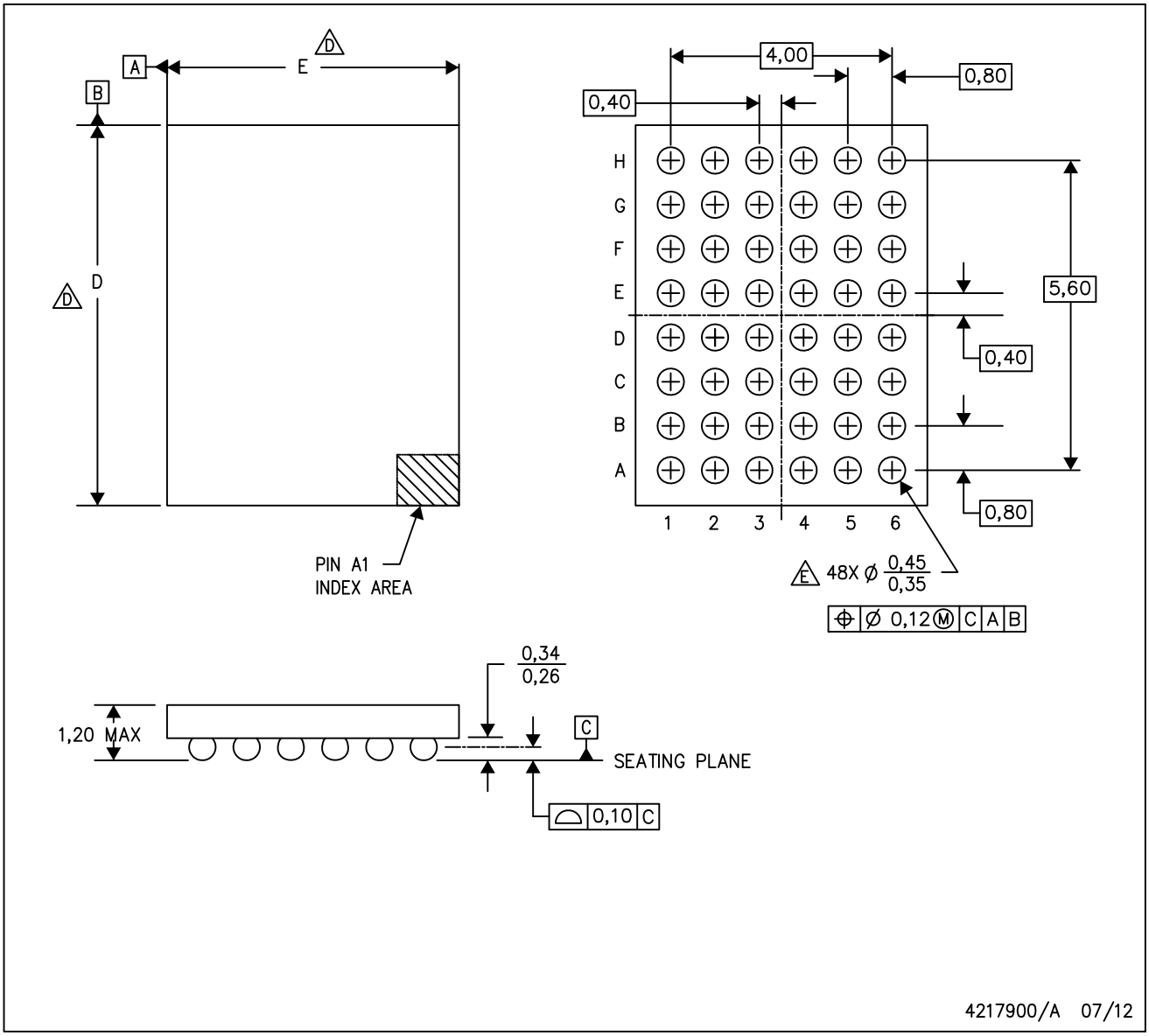
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

YVA (R–XBGA–N48) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population.
6 x 8 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

NanoFree is a trademark of Texas Instruments.

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