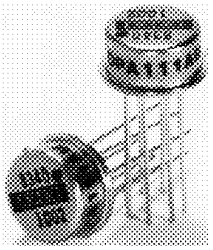
BURR - BROWN®



OPA111

Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 100% Tested, 8nV$\sqrt{Hz}$ max (10kHz)
- LOW BIAS CURRENT: 1pA max
- LOW OFFSET: 250μV max
- LOW DRIFT: 1μV/°C max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 100dB min

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- OPTOELECTRONICS
- MEDICAL EQUIPMENT—CAT SCANNER
- RADIATION HARD EQUIPMENT

DESCRIPTION

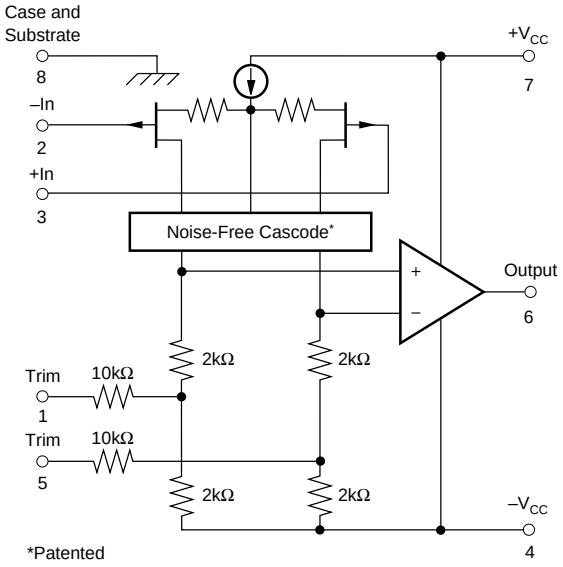
The OPA111 is a precision monolithic dielectrically isolated FET (***Difet***®) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with patented circuit design techniques. A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.



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PDS-526K
Printed in U.S.A. August, 1995

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITION	OPA111AM			OPA111BM			OPA111SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
NOISE											
Voltage, f_O = 10Hz	100% Tested		40	80		30	60		40	80	nV/√Hz
f_O = 100Hz	100% Tested		15	40		11	30		15	40	nV/√Hz
f_O = 1kHz	100% Tested		8	15		7	12		8	15	nV/√Hz
f_O = 10kHz	100% Tested		6	8		6	8		6	8	nV/√Hz
f_B = 10Hz to 10kHz	100% Tested		0.7	1.2		0.6	1		0.7	1.2	µVrms
f_B = 0.1Hz to 10Hz	(1)		1.6	3.3		1.2	2.5		1.6	3.3	µVp-p
Current, f_B = 0.1Hz to 10Hz	(1)		9.5	15		7.5	12		9.5	15	fAp-p
f_O = 0.1Hz thru 20kHz	(1)		0.5	0.8		0.4	0.6		0.5	0.8	fA/√Hz
OFFSET VOLTAGE(2)											
Input Offset Voltage	V_{CM} = 0VDC		±100	±500		±50	±250		±100	±500	µV
Average Drift	T_A = T_{MIN} to T_{MAX}		±2	±5		±0.5	±1		±2	±5	µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	90	110		100	110		90	110		dB
			±3	±31		±3	±10		±3	±31	µV/V
BIAS CURRENT(2)											
Input Bias Current	V_{CM} = 0VDC		±0.8	±2		±0.5	±1		±0.8	±2	pA
OFFSET CURRENT(2)											
Input Offset Current	V_{CM} = 0VDC		±0.5	±1.5		±0.25	±0.75		±0.5	±1.5	pA
IMPEDANCE											
Differential			10^{13} || 1			10^{13} || 1			10^{13} || 1		Ω || pF
Common-Mode			10^{14} || 3			10^{14} || 3			10^{14} || 3		Ω || pF
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	90	110		100	110		90	110		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	114	125		120	125		114	125		dB
FREQUENCY RESPONSE											
Unity Gain, Small Signal			2			2			2		MHz
Full Power Response	20Vp-p, R_L = 2kΩ	16	32		16	32		16	32		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	1	2		1	2		1	2		V/µs
Settling Time, 0.1%	Gain = –1, R_L = 2kΩ		6			6			6		µs
0.01%	10V Step		10			10			10		µs
Overload Recovery, 50% Overdrive(3)	Gain = –1		5			5			5		µs
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11	±12		±11	±12		±11	±12		V
Current Output	V_O = ±10VDC	±5.5	±10		±5.5	±10		±5.5	±10		mA
Output Resistance	DC, Open Loop		100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		2.5	3.5		2.5	3.5		2.5	3.5	mA
TEMPERATURE RANGE											
Specification	Ambient Temp.	–25		+85	–25		+85	–55		+125	°C
Operating	Ambient Temp.	–55		+125	–55		+125	–55		+125	°C
Storage	Ambient Temp.	–65		+150	–65		+150	–65		+150	°C
θ Junction-Ambient			200			200			200		°C/W

NOTES: (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

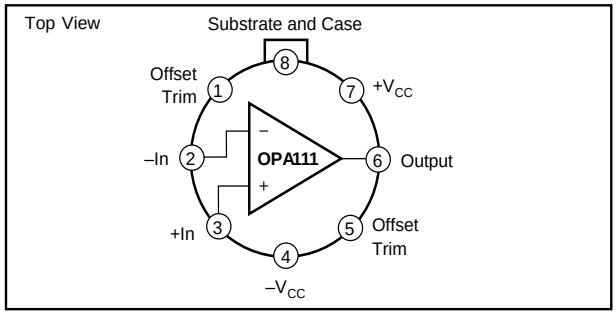
ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITION	OPA111AM			OPA111BM			OPA111SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range	Ambient Temp.	–25		+85	–25		+85	–55		+125	°C
INPUT											
OFFSET VOLTAGE(1)											
Input Offset Voltage	V_{CM} = 0VDC		±220	±1000		±110	±500		±300	±1500	µV
Average Drift			±2	±5		±0.5	±1		±2	±5	µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	86	100		90	100		86	100		dB
			±10	±50		±10	±32		±10	±50	µV/V
BIAS CURRENT(1)											
Input Bias Current	V_{CM} = 0VDC		±50	±250		±30	±130		±820	±4100	pA
OFFSET CURRENT(1)											
Input Offset Current	V_{CM} = 0VDC		±30	±200		±15	±100		±510	±3100	pA
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	100		90	100		86	100		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	110	120		114	120		110	120		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±10.5	±11		±11	±11.5		±11	±11.5		V
Current Output	V_O = ±10VDC	±5.25	±10		±5.25	±10		±5.25	±10		mA
Short Circuit Current	V_O = 0VDC	10	40		10	40		10	40		mA
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		2.5	3.5		2.5	3.5		2.5	3.5	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation(1)	750mW
Differential Input Voltage(2)	±36VDC
Input Voltage Range(2)	±18VDC
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit Duration(3)	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on θ_{JC} = 150°C/W or θ_{JA} = 300°C/W. (2) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to +18V > V_{IN} > $-V_{CC}$ – 6V. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

PACKAGE INFORMATION

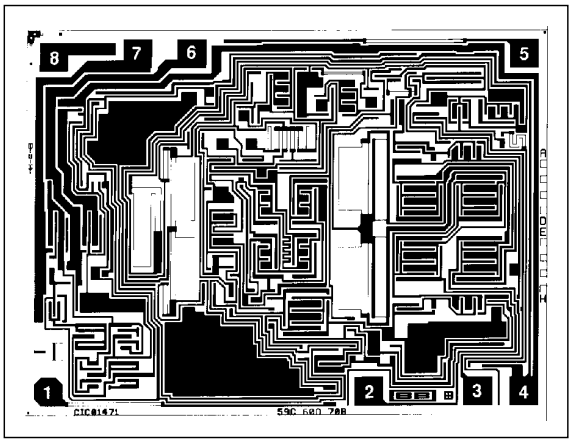
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA111AM	TO-99	001
OPA111BM	TO-99	001
OPA111SM	TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE, MAX (µV)
OPA111AM	TO-99	–25°C to +85°C	±500
OPA111BM	TO-99	–25°C to +85°C	±250
OPA111SM	TO-99	–55°C to +125°C	±500

DICE INFORMATION



OPA111AD DIE TOPOGRAPHY

PAD	FUNCTION
1	Offset Trim
2	–In
3	+In
4	$-V_S$
5	Offset Trim
6	Output
7	$+V_S$
8	Substrate

Substrate Bias: This Dielectrically-Isolated Substrate is normally connected to common.

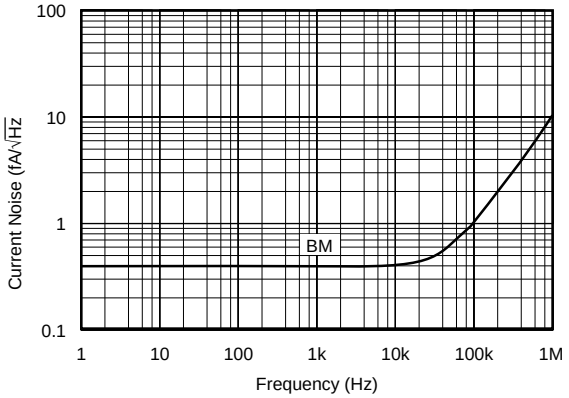
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	95 x 71 ±5	2.41 x 1.80 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing:		None
Transistor Count:		44

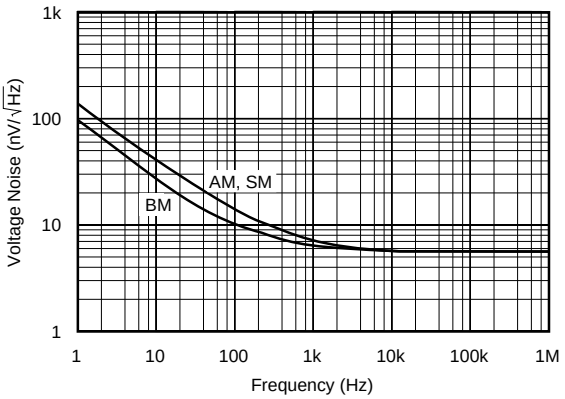
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

INPUT CURRENT NOISE SPECTRAL DENSITY



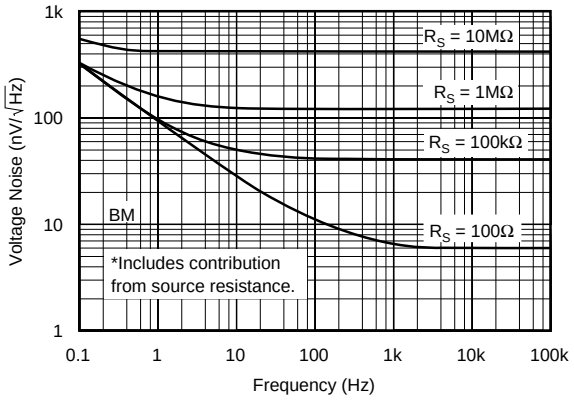
INPUT VOLTAGE NOISE SPECTRAL DENSITY



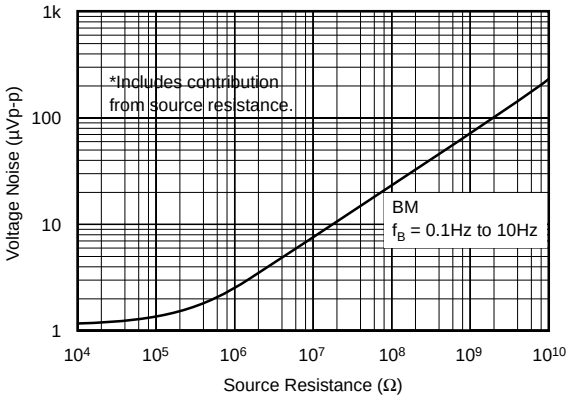
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

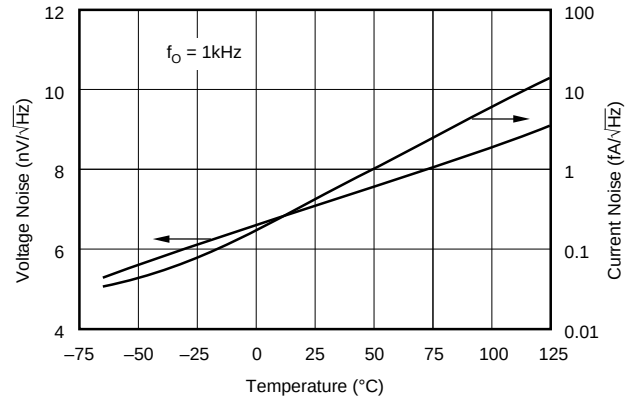
TOTAL* INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



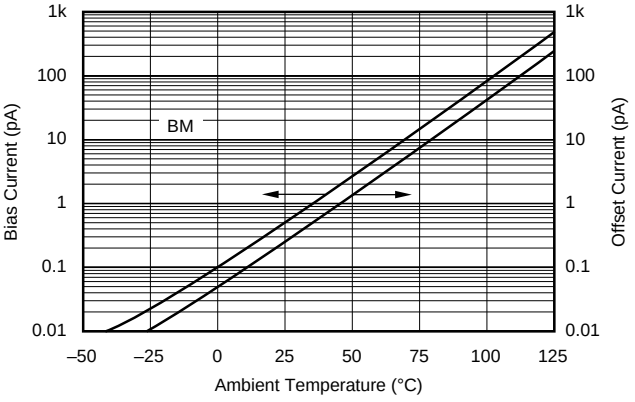
TOTAL* INPUT VOLTAGE NOISE (PEAK-TO-PEAK) vs SOURCE RESISTANCE



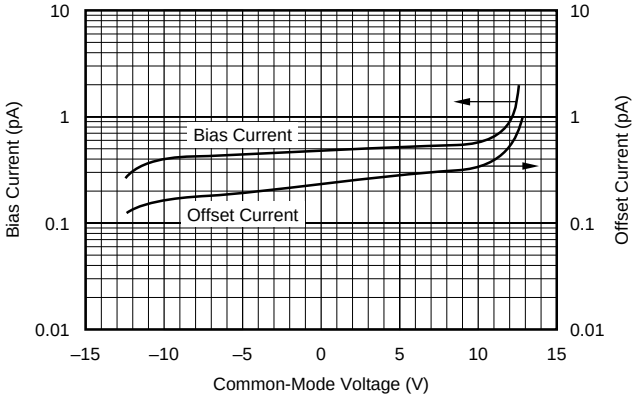
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



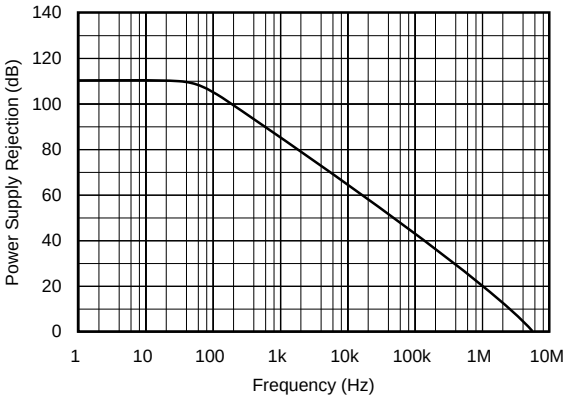
BIAS AND OFFSET CURRENT vs TEMPERATURE



BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



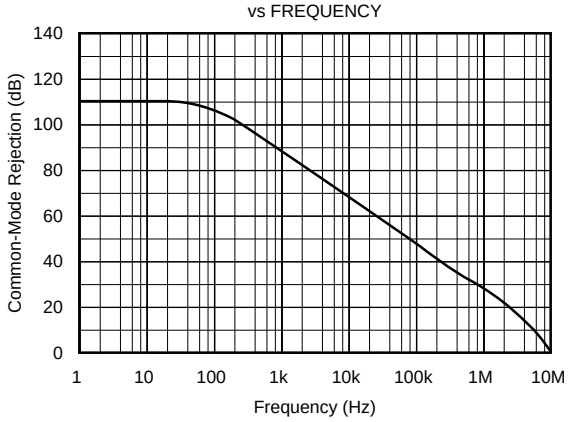
POWER SUPPLY REJECTION vs FREQUENCY



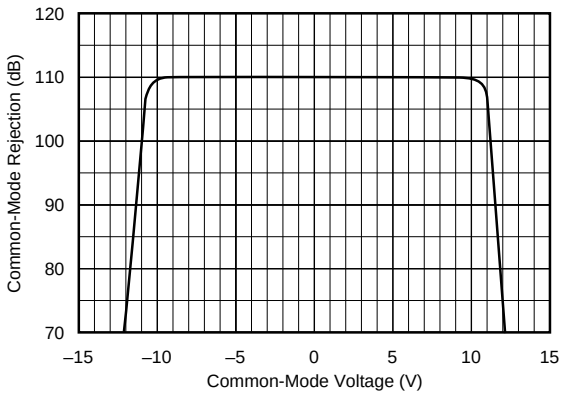
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

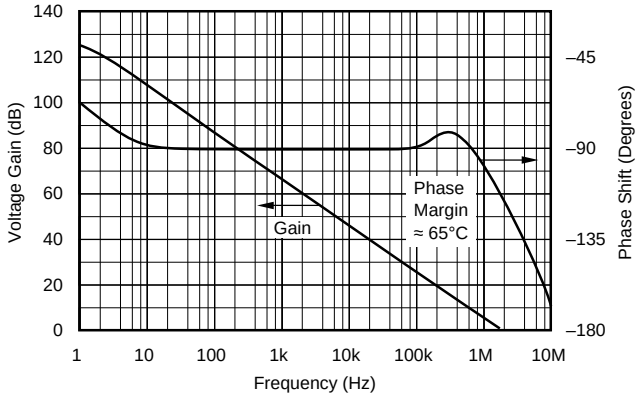
COMMON-MODE REJECTION
vs FREQUENCY



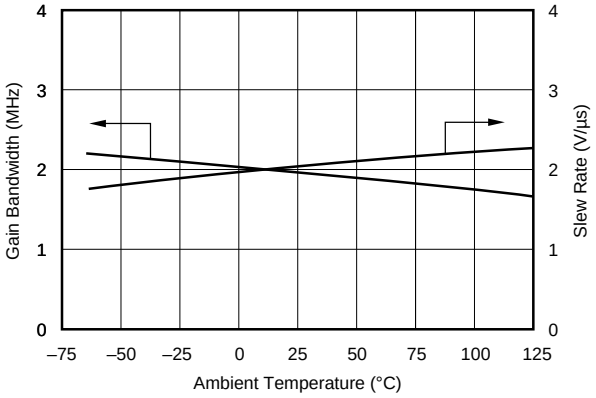
COMMON-MODE REJECTION
vs INPUT COMMON MODE VOLTAGE



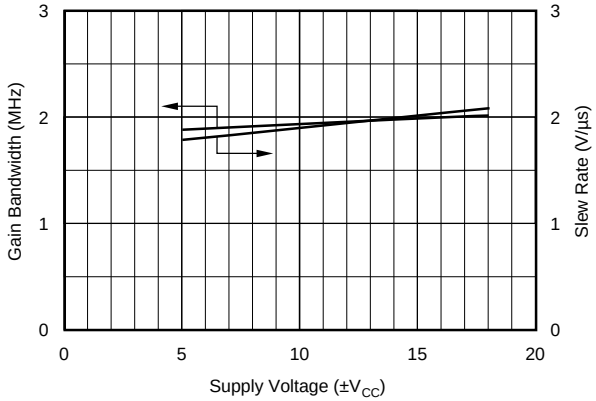
OPEN-LOOP FREQUENCY RESPONSE



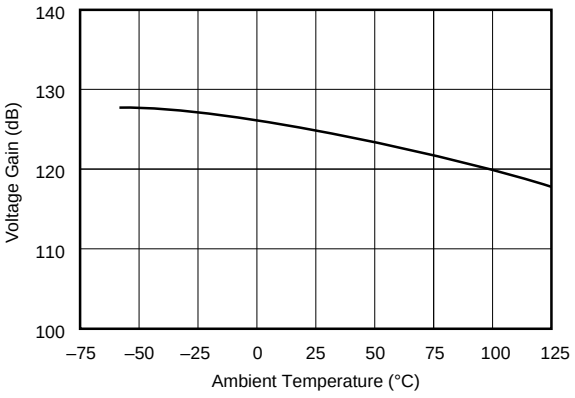
GAIN-BANDWIDTH AND SLEW RATE
vs TEMPERATURE



GAIN-BANDWIDTH AND SLEW RATE
vs SUPPLY VOLTAGE



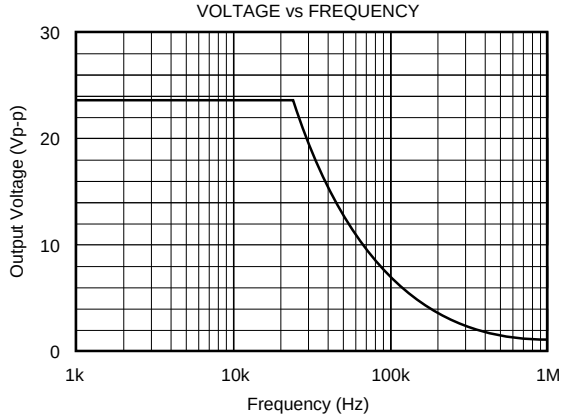
OPEN-LOOP GAIN vs TEMPERATURE



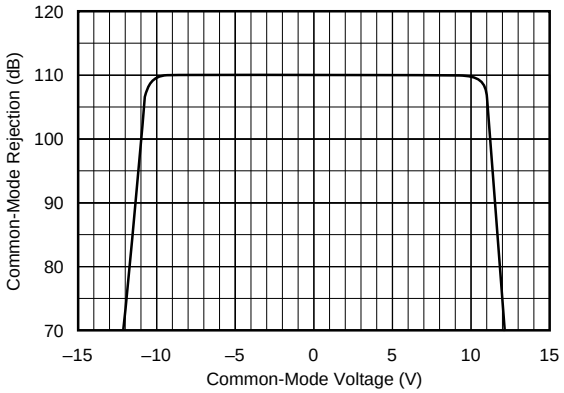
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

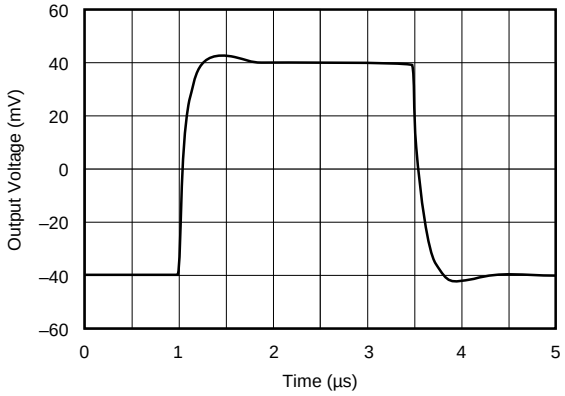
MAXIMUM UNDISTORTED OUTPUT VOLTAGE vs FREQUENCY



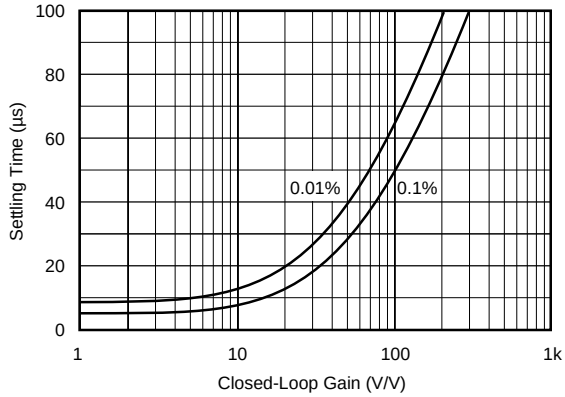
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



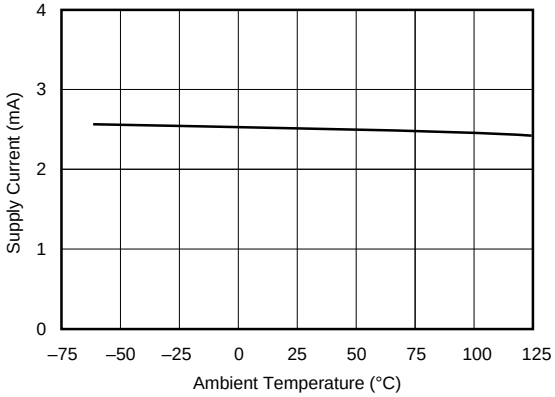
SMALL SIGNAL TRANSIENT RESPONSE



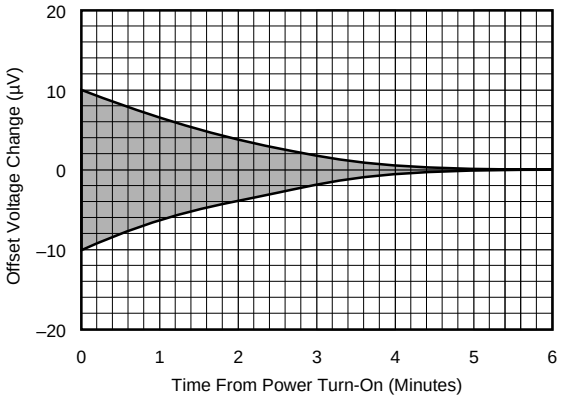
SETTLING TIME vs CLOSED-LOOP GAIN



SUPPLY CURRENT vs TEMPERATURE

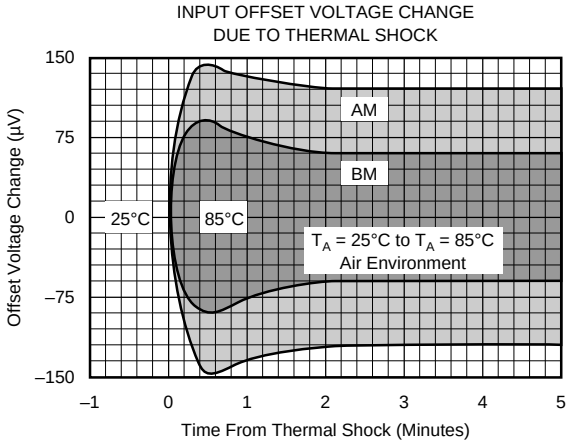


INPUT OFFSET VOLTAGE WARM-UP DRIFT



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA111 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3µV/°C for each 100µV of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as 741 and AD547. The OPA111 can replace most other amplifiers by leaving the external null circuit unconnected.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

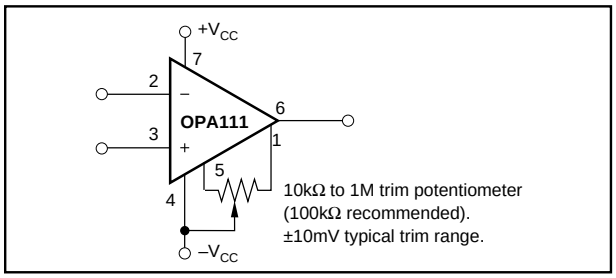


FIGURE 1. Offset Voltage Trim.

Unlike BIFET amplifiers, The ***Difet*** OPA111 requires input current limiting resistors only if its input voltage is greater than 6V more negative than $-V_{CC}$. A 10kΩ series resistor will limit input current to a safe level with up to ±15V input levels, even if both supply voltages are lost.

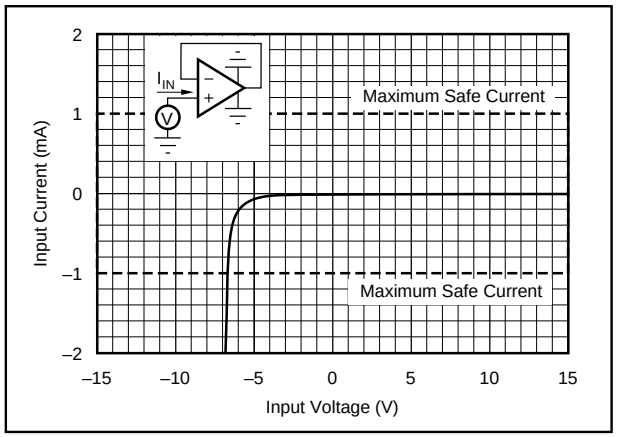


FIGURE 2. Input Current vs Input Voltage with ±V_{CC} Pins Grounded.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA111. To avoid leakage problems, it is recommended that the signal input lead of the OPA111 be wired to a Teflon standoff. If the OPA111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern

should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 3).

If guarding is not required, pin 8 (case) should be connected to ground.

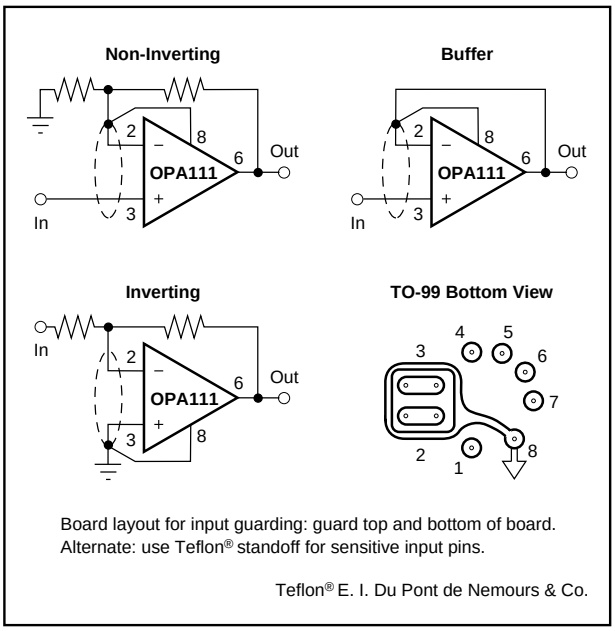


FIGURE 3. Connection of Input Guard.

NOISE: FET VERSUS BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ, the OPA111 will have a lower total noise than an OP-27 (see Figure 4).

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias current of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 5). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely low bias current of the OPA111 is not compromised by common-mode voltage.

APPLICATIONS CIRCUITS

Figures 6 through 18 are circuit diagrams of various applications for the OPA111.

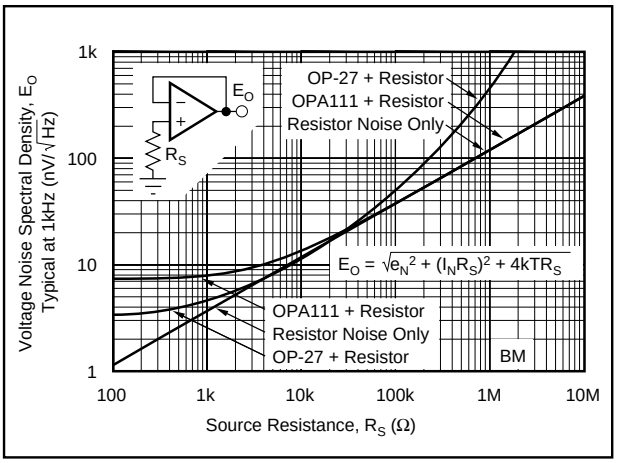


FIGURE 4. Voltage Noise Spectral Density vs Source Resistance.

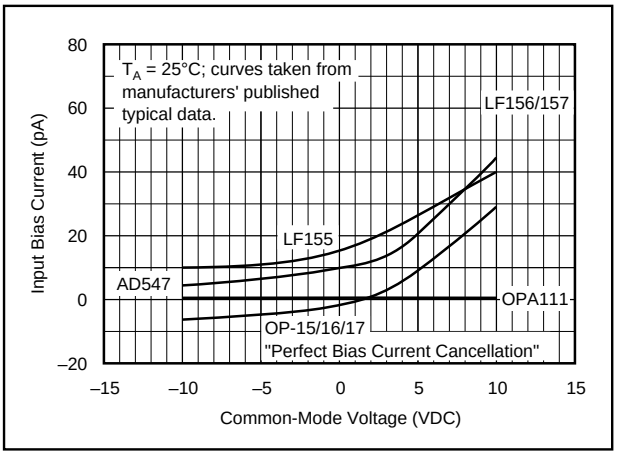


FIGURE 5. Input Bias Currrent vs Common-Mode Voltage.

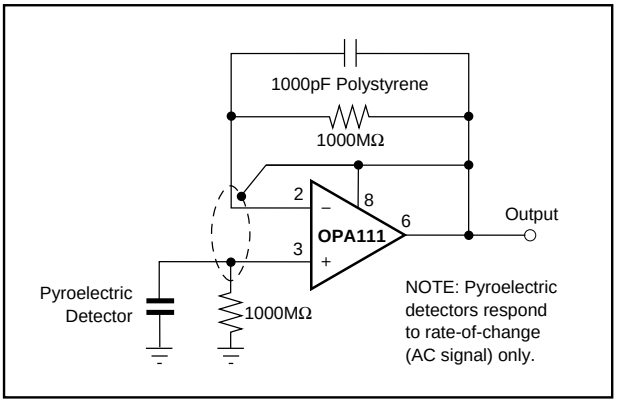


FIGURE 6. Pyroelectric Infrared Detector.

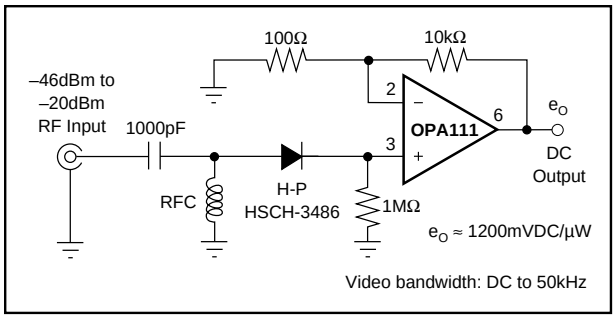


FIGURE 7. Zero-Bias Schottky Diode Square-Law RF Detector.

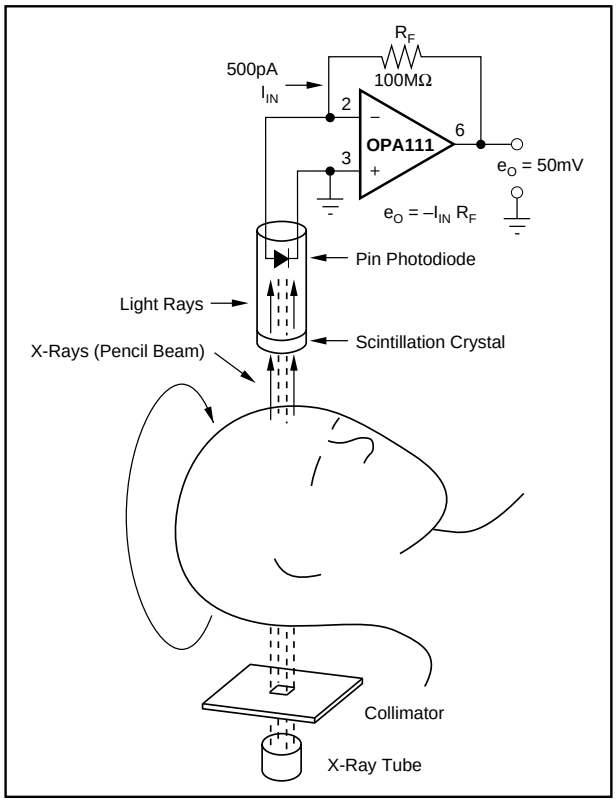


FIGURE 8. Computerized Axial Tomography (CAT) Scanner Channel Amplifier.

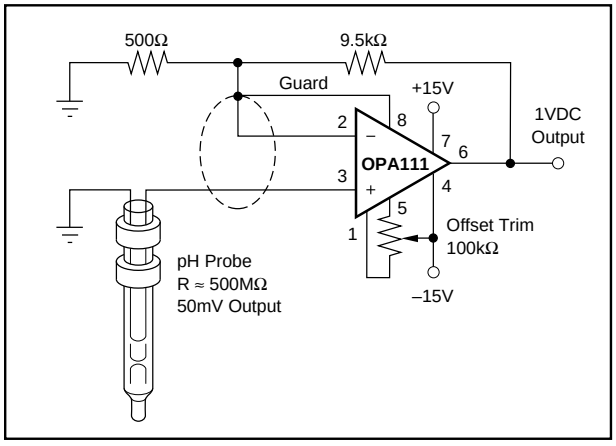


FIGURE 9. High Impedance ($10^{14}\Omega$) Amplifier.

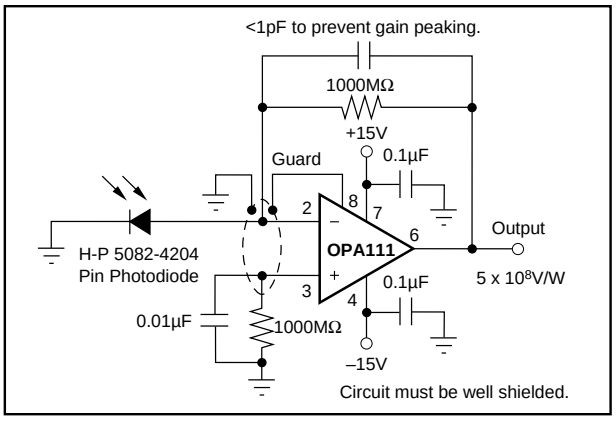


FIGURE 10. Sensitive Photodiode Amplifier.

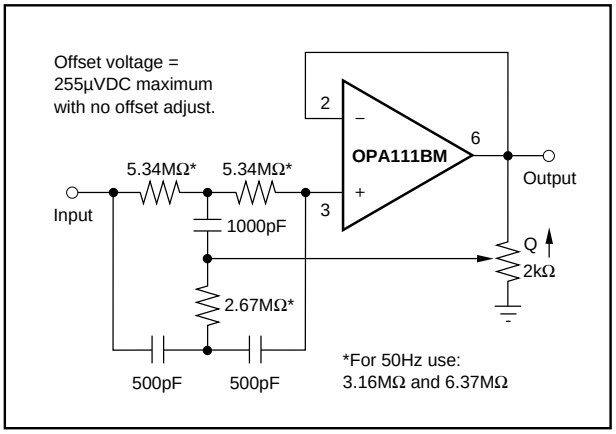


FIGURE 11. 60Hz Reject Filter.

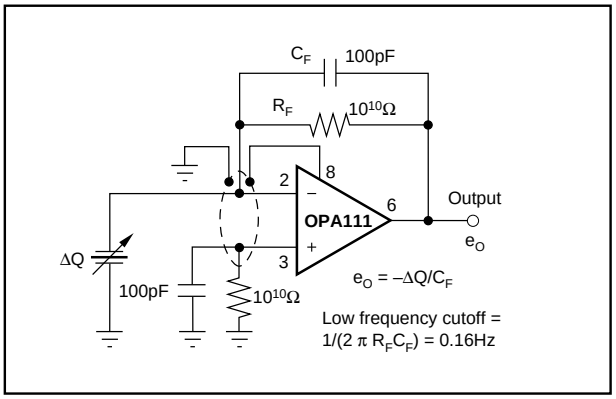


FIGURE 12. Piezoelectric Transducer Charge Amplifier.

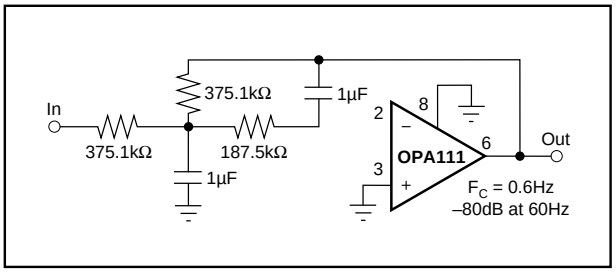


FIGURE 13. 0.6Hz Second-Order Low-Pass Filter.

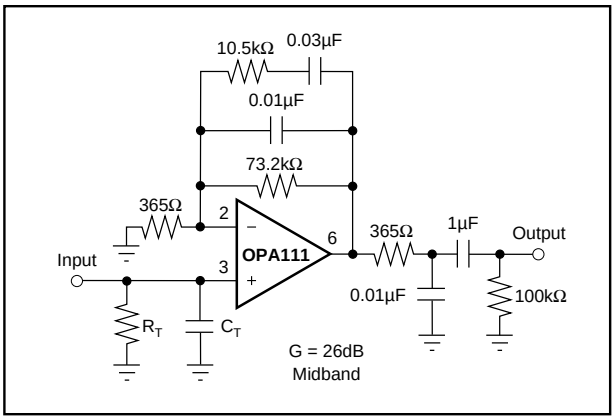


FIGURE 14. RIAA Equalized Phono Preamplifier.

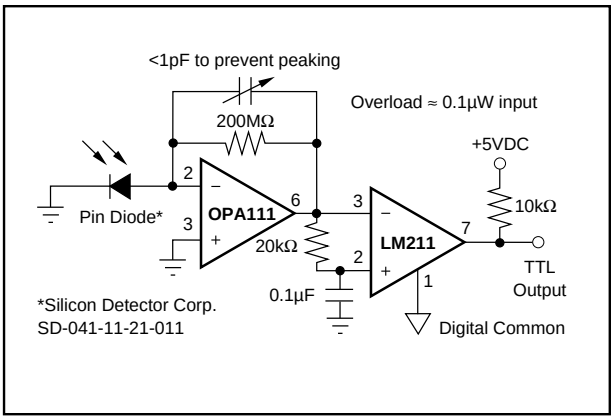


FIGURE 15. High Sensitivity (under 1nW) Fiber Optic Receiver for 9600 Baud Manchester Data.

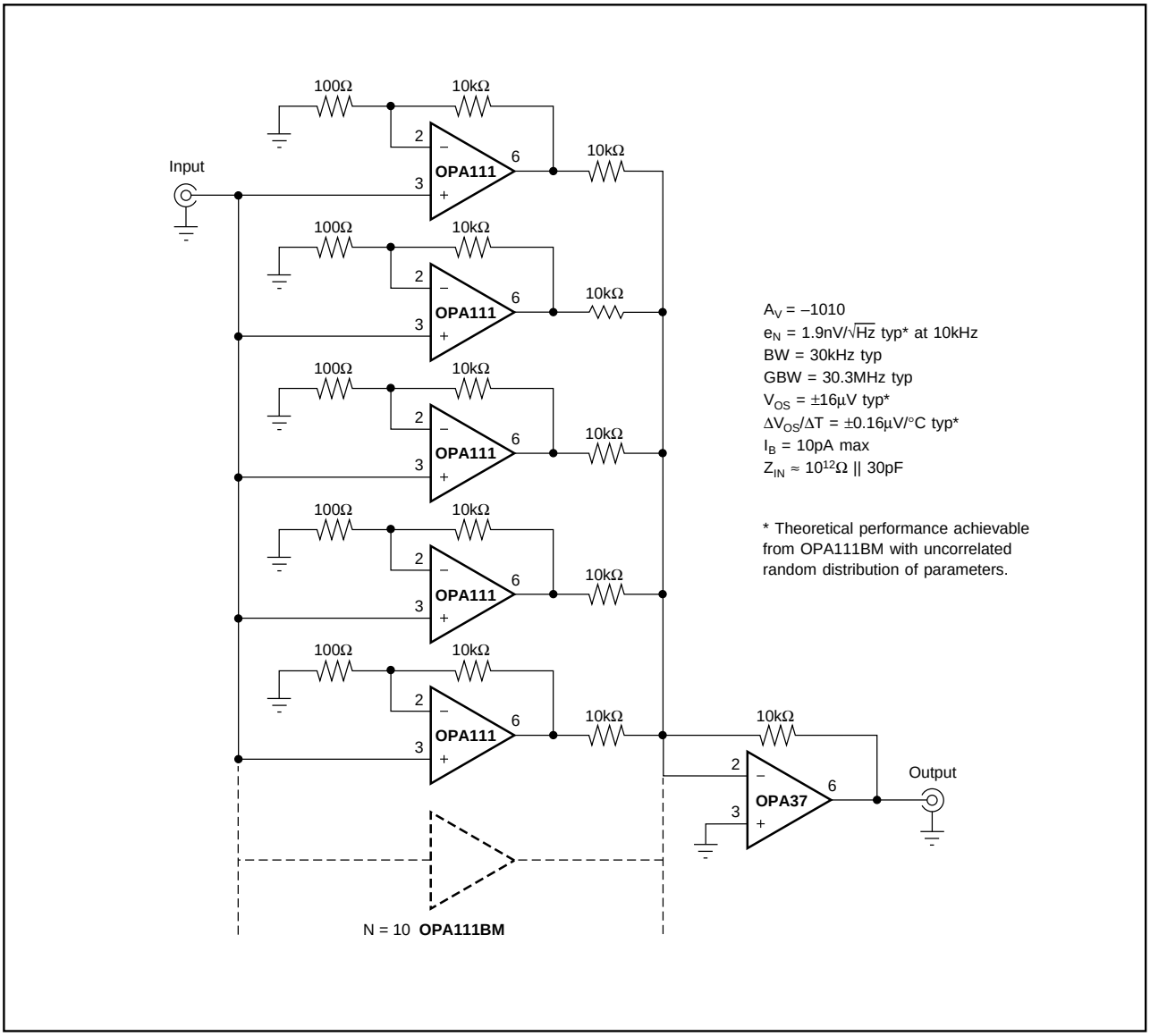


FIGURE 16. 'N' Stage Parallel-Input Amplifier for Reduced Relative Amplifier Noise at the Output.

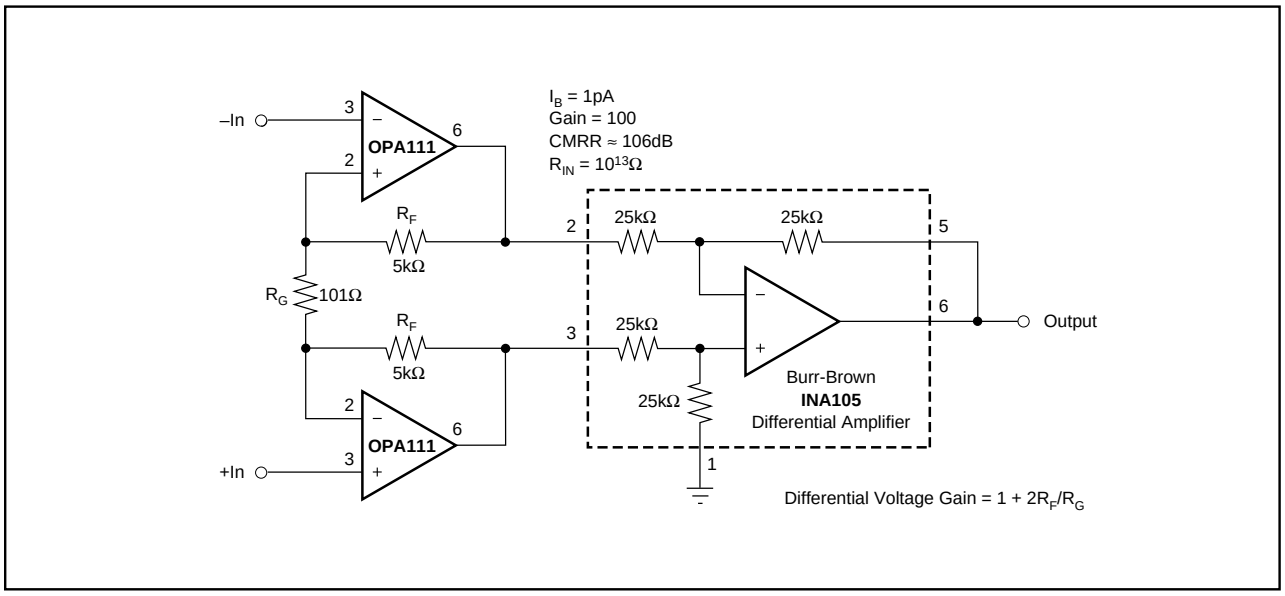


FIGURE 17. FET Input Instrumentation Amplifier.

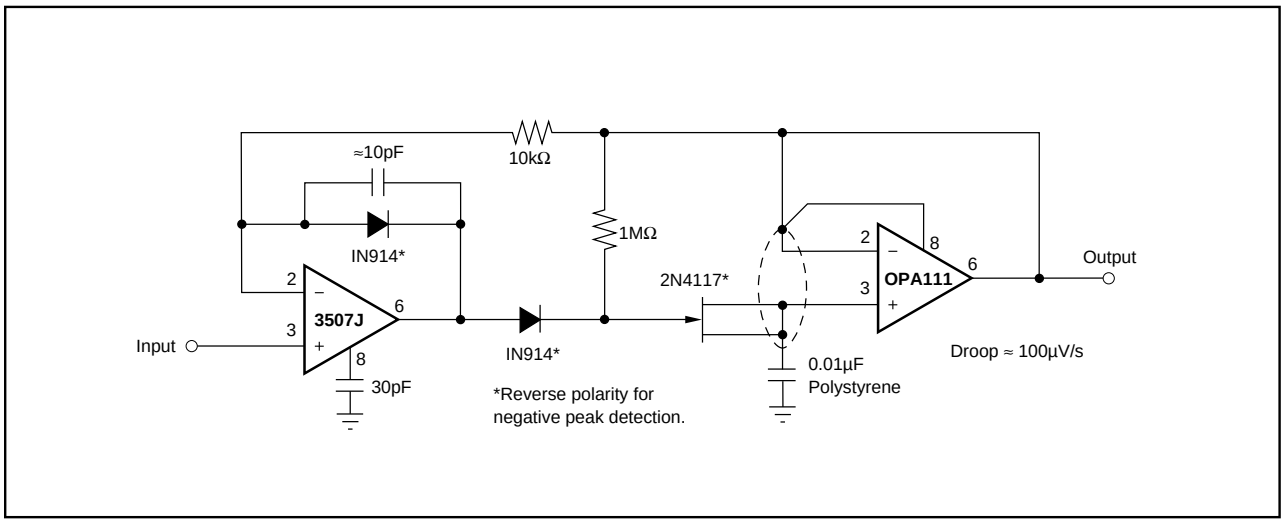


FIGURE 18. Low-Droop Positive Peak Detector.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA111AM	LIFEBUY	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		OPA111AM	
OPA111BM	LIFEBUY	TO-99	LMC	8	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		OPA111BM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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