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FCH104N60

June 2014

N-Channel SuperFET® II MOSFET

600 V, 37 A, 104 mΩ

Features

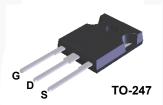
- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 96 m Ω
- Ultra Low Gate Charge (Typ. Q_g = 63 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 280 pF)
- 100% Avalanche Tested
- · RoHS Compliant

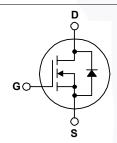
Applications

- · Telecom / Sever Power Supplies
- · Industrial Power Supplies

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FCH104N60	Unit
V _{DSS}	Drain to Source Voltage			600	V
	Cata ta Cauraa Valtana	- DC		±20	V
V_{GSS}	Gate to Source Voltage	- AC	(f > 1 Hz)	±30	- V
	Drain Current	- Continuous (T _C = 25°C)	/	37	Α
ID	Drain Current	- Continuous (T _C = 100°C)		24	- A
I _{DM}	Drain Current	- Pulsed	(Note 1)	111	Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		809	mJ	
I _{AR}	Avalanche Current		(Note 1)	6.8	Α
E _{AR}	Repetitive Avalanche Energy (Note 1)		3.57	mJ	
dv/dt	MOSFET dv/dt			100	V/ns
uv/ui	Peak Diode Recovery dv/dt		(Note 3)	20	V/IIS
D	Dawar Dissination	(T _C = 25°C)		357	W
P_{D}	Power Dissipation	- Derate Above 25°C		2.85	W/°C
T _J , T _{STG}	Operating and Storage Temperature	Operating and Storage Temperature Range			°C
T _L	Maximum Lead Temperature for S	oldering, 1/8" from Case for 5 Sec	conds	300	οС

Thermal Characteristics

Symbol	Parameter FCH104N		Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.35	°C/W
$R_{\theta,IA}$	Thermal Resistance, Junction to Ambient, Max. 40		30/00

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH104N60	FCH104N60	TO-247	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
D\/	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 25^{\circ}\text{C}$	600	-	-	V
BV _{DSS}	Dialii to Source Breakdowii voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 150^{\circ}\text{C}$	650	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	0.67	-	V/°C
1	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	-	-	1	μА
IDSS	Zero Gate voltage Drain Current	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	1.98	-	μΑ
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2.5	-	3.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 18.5 A	-	96	104	mΩ
g _{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 18.5 \text{ A}$	-	33	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 200 V V 0 V	-	3130	4165	pF
C _{oss}	Output Capacitance	V _{DS} = 380 V, V _{GS} = 0 V, f = 1 MHz		75	100	pF
C _{rss}	Reverse Transfer Capacitance	1 1 1 1 1 1 2	-\	3.66	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	280	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 380 V, I _D = 18.5 A,	- \	63	82	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	14	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	15	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.97	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time			-	26	62	ns
t _r	Turn-On Rise Time	$V_{DD} = 380 \text{ V}, I_D = 18.5 \text{ A},$		- /	18	46	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_g = 4.7 \Omega$		-/	72	154	ns
t _f	Turn-Off Fall Time		(Note 4)	-	3.3	17	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	37	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	114	Α
V_{SD}	Drain to Source Diode Forward Voltage V ₀	_{GS} = 0 V, I _{SD} = 18.5 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time V	_{GS} = 0 V, I _{SD} = 18.5 A,	-	414	-	ns
Q _{rr}	Reverse Recovery Charge dl	_F /dt = 100 A/μs	-	8.8	-	μC

Notes:

- 1. Repetitive Rating: pulse width limited by maximum junction temperature.
- 2. I_{AS} = 6.8 A, R_{G} = 25 Ω , Starting T_{J} = 25°C
- 3. I $_{SD} \leq$ 18.5 A, di/dt \leq 200 A/ μ s, V $_{DD} \leq$ 380 V, Starting T $_{J}$ = 25°C
- 4. Essentially Independent of Operating Temperature.

Typical Characteristics

Figure 1. On-Region Characteristics

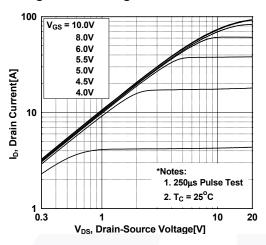


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

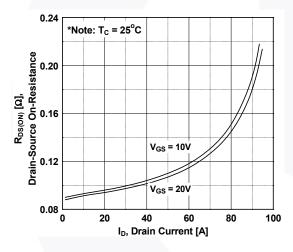


Figure 5. Capacitance Characteristics

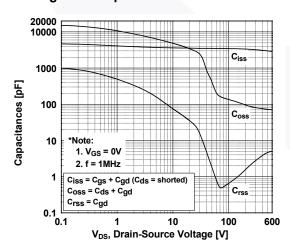


Figure 2. Transfer Characteristics

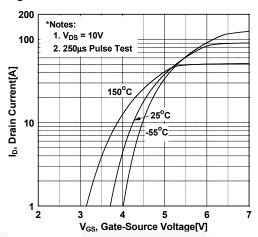


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

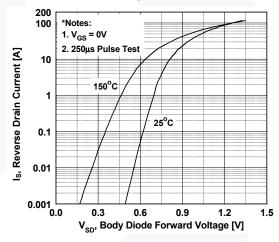
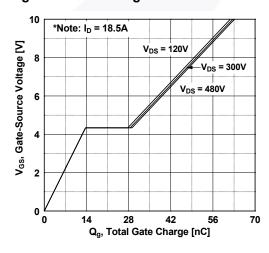


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

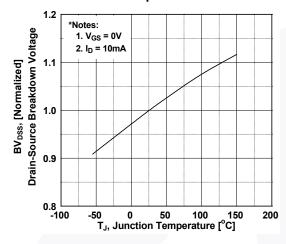


Figure 9. Maximum Safe Operating Area

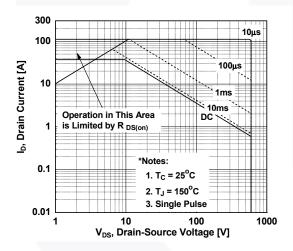


Figure 11. Eoss vs. Drain to Source Voltage

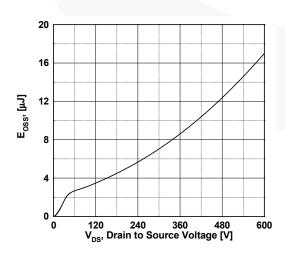


Figure 8. On-Resistance Variation vs. Temperature

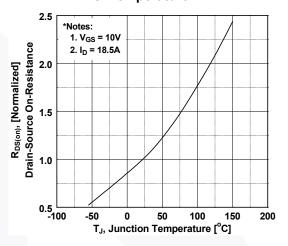
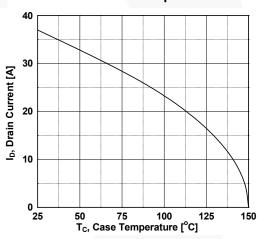


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Characteristics (Continued)

Figure 12. Transient Thermal Response Curve

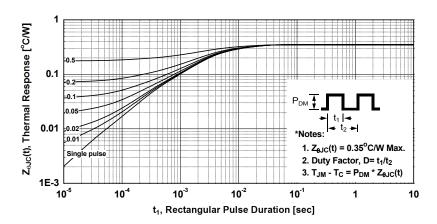


Figure 13. Gate Charge Test Circuit & Waveform

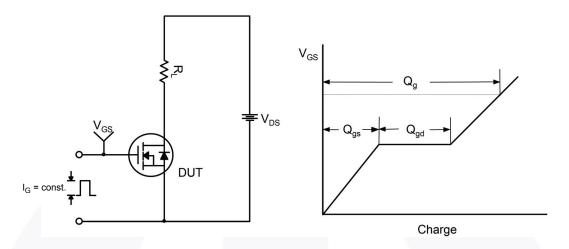


Figure 14. Resistive Switching Test Circuit & Waveforms

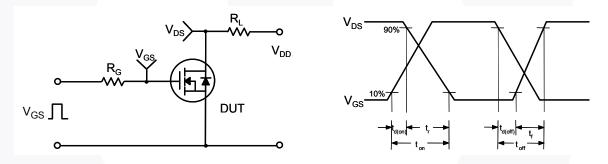
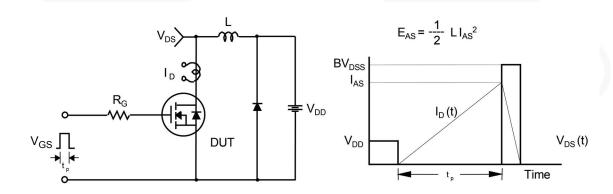


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms



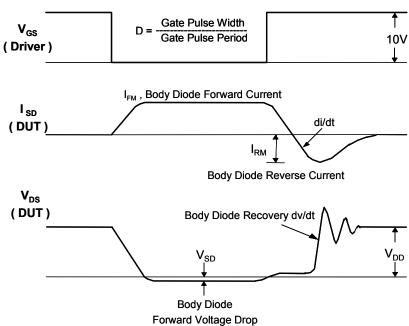
Dut

VDS

Same Type
as Dut

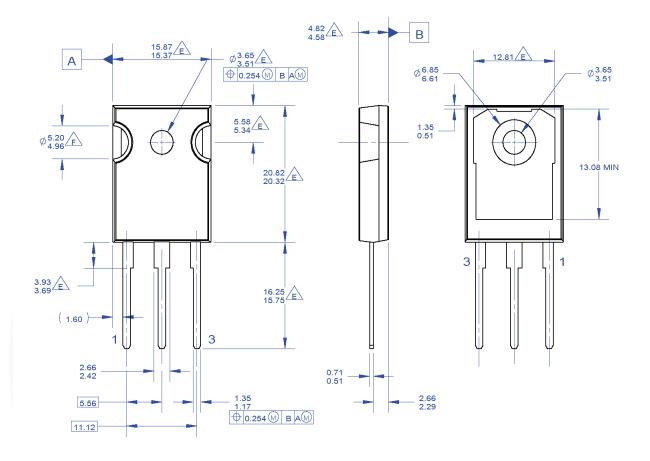
• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-247 3L



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
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Figure 17. TO-247, Molded, 3 Lead, Jedec Variation AB

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